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MODELING AND ANALYSIS OF TUNED POWER AMPLIFIERS

by
Ned Eugene Abbott

A dissertation submitted in partial fulfillment
of the requirements for the degree of
Doctor of Philosophy
(Electrical Engineering)
in The University of Michigan
1971

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CHAPTER 1

INTRODUCTION

1.1 Purpose

The desire to understand and design circuits for efficient conversion of electrical energy over a wide frequency range has prompted this study of large-signal high-frequency transistor amplifiers. The problems associated with the design of RF power amplifiers to achieve various performance criteria have received considerable attention in the past. Due to the nonlinear behavior often associated with such large-signal amplifiers, there are very few specific design rules that can be used in their development. At the present time, large-signal RF power amplifiers are typically designed by laboratory determination of "average" large-signal device characteristics, design of simple linear matching circuitry to fit these "average" characteristics, and laboratory cut-and-try procedures to optimize the circuit performance. Unfortunately, the cut-and-try approach is only useful for relatively simple circuits. In addition, such approaches do not allow the engineer to determine what circuit performance could be obtainable if a different device were chosen as a gain element for the circuit.

The rapid development of new devices by the semiconductor industry adds to the design problem. Even as the designer selects an appropriate device for a particular task, he is aware of possible

circuit improvements as new devices become available. When considering complex tuning networks, multiple power stages, strip-line networks and integrated high frequency power stages, the designer needs more analytical methods for predicting, studying and optimizing circuit performance. The use of a high-speed digital computer for analyzing complex nonlinear circuits offers one possible method for aiding the solution of these design problems.

Computer-aided circuit design and analysis is well-developed in problem areas involving linear circuit models for transistors and other active devices. Many automated analysis programs even provide nonlinear device models for determining transient behavior of nonlinear circuits. There is, however, no general nonlinear transistor model stemming from device measurements that adequately incorporates the high-frequency large-signal characteristics of most RF power transistors. It is therefore desirable to develop models and techniques for determining the model parameters that may subsequently be used for computer analysis of high-frequency large-signal circuits.

The main purpose of this research is to further the understanding of high frequency transistorized power amplifiers. This objective involves development of related models and computer analysis techniques. The work is concerned mainly with the behavior

of class C amplifiers operating in the VHF frequency range. Previous analyses of class C amplifiers have been limited by certain assumptions introduced to make hand analysis tractable. The analyses to be presented here are numerical in nature, allowing the power of high speed digital computation to aid in removal of many of the standard assumptions.

Previous analyses typically assume that the operating frequency is low in comparison to the transistor limitations, and low frequency models of the transistor are used (Refs. S3, H5, S2, E3). The Q's of the output tuning networks are normally assumed to be high so that output waveforms can be assumed to be purely sinusoidal. Many analyses make the further assumption that the emitter-base and collector-base junction potentials are sinusoidal (Refs. H5, S3, S4, W1, S2, E3, P1). In addition, the waveshapes of transistor output current are often assumed to be of some known shape, and the corresponding base currents are calculated by assuming linear or very simple relationships between the two currents (Refs. S2, S3, P1). In keeping with the assumed current waveshapes, the device is assumed always to operate in cut-off or the active region of operation. The device is allowed to approach the edge of saturation but not allowed to enter the saturation region (Refs. H5, S2, S3). For further simplification, extrinsic device resistances and inductances are usually neglected, and depletion capacitances are assumed to be constant or nonexistent (Refs. H5, S2, S3, P1).

Depending on the intended purpose of the amplifier the standard assumptions may or may not be justified. In the class C amplifier design problems to be stressed in this work none of the above assumptions are truly justified. The basic problem to be considered is one of making use of the given device to obtain maximum fundamental output power or maximum efficiency of energy conversion at frequencies near the gain bandwidth limitation of the device. Power gain is of secondary importance, and in general, power gain will be sacrificed to provide operating efficiency and to increase the output power. With such operation in mind the high-frequency characteristics of the transistor must be included in the description of amplifier behavior. Typical values of operating Q lie in the range of 1 to 10, and as a result, considerable amounts of harmonic content will appear in the output voltage waveforms. The harmonic powers must be included for complete characterization of amplifier performance. The relationships between the terminal currents and voltages of a transistor can be expressed in terms of nonlinear differential equations, and the application of digital computation methods allows a rather complete description to be used instead of relying on linearizing assumptions. By using this more complete description, the current waveshapes need not be assumed but can be determined from input excitation and linear network constraints. A standard method of operation of class C power stages is to provide an excess of input power so that the output power

attains a saturation level. Such operation improves the efficiency of operation of the output circuitry and stabilizes the output power with respect to slight variations in input power (Ref. S4). In this mode of operation the transistor is periodically driven into the saturation region,and saturation effects must be included if an accurate analysis is desired. The large signals encountered in tuned power amplifiers can cause avalanche breakdown of the semiconductor junctions, and this effect is also easily included in computer simulations.

1.2 Statement of Problem

As an introduction to the types of problems to be studied, consider the general circuit configuration for a single stage tuned power amplifier shown in Fig. 1.1. In a strict sense, the concept of admittance does not apply to the nonlinear behavior of the input and output characteristics of the transistor under large signal excitation, but artificial admittances $Y_{i_{Equiv}}$ and $Y_{0_{Equiv}}$ are introduced here in a manner consistent with that currently in use by most manufacturers of VHF power transistors (Refs. C5, H7, H9, L2). That is, with the input and output matching networks of a given configuration adjusted[1] for maximizing a given performance criteria (i.e., max power output, max efficiency, etc.) with given bias conditions, signal levels, and frequency; the transistor large-signal equivalent admittances are

[1] These adjustments are normally accomplished with low-loss LC networks or double-stub tuners.

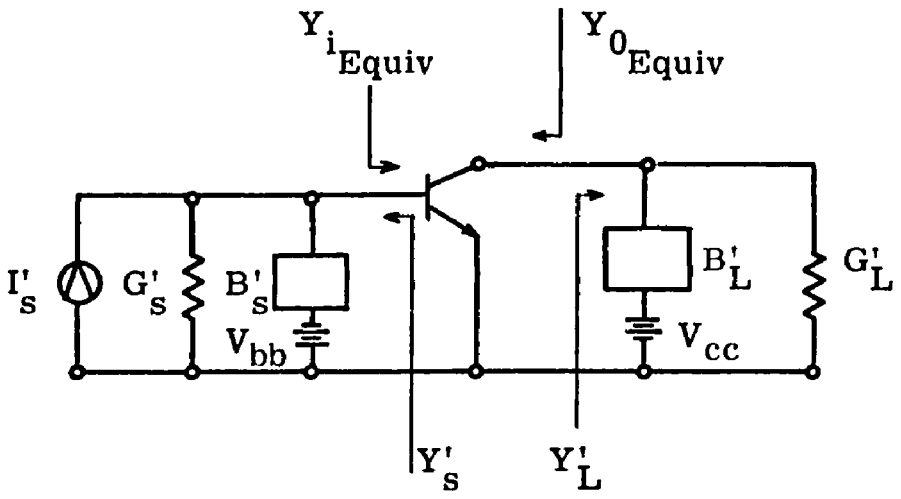

Fig. 1.1. Circuit configuration for tuned power amplifier

defined in terms of the linear matching networks as:

$$Y_{i_{Equiv}} = Y_s'^*$$

$$Y_{0_{Equiv}} = Y_L'^*$$

Information about $Y_{i_{Equiv}}$ and $Y_{0_{Equiv}}$ as functions of frequency and signal level is useful in the practical sense of designing passive circuitry for obtaining a maximum output power over a selected frequency range; however, there are definite limitations to this information. Since the transistor is operating in a nonlinear mode, the overall behavior depends on the effects of the tuning networks on the harmonic components of the signals as well as the fundamental. Hence it is not possible to predict accurately the behavior of the transistor

when it is imbedded in a network that differs from the networks used for determining $Y_{i_{Equiv}}$ and $Y_{0_{Equiv}}$. In addition, this equivalent admittance technique does not provide the designer with sufficient information to estimate such characteristics as amplifier bandwidth in wideband situations or the effects of bias conditions on the circuit behavior. It is difficult for the designer to analytically determine the trade-offs possible in power output, bandwidth, and efficiency; and as a result he is often forced into trial-and-error laboratory procedures to determine the level of performance he can expect from a given device in a specified application.

Our objective is to increase the understanding of some of the basic characteristics of class C and class D amplifiers, to develop modeling techniques suitable for describing the large-signal high-frequency effects encountered in VHF power transistors, and to develop computer analysis programs for predicting the performance of class C and D amplifiers. Before analyses of the amplifiers are begun, transistor models are selected to provide descriptions of the major dynamic and nonlinear transistor characteristics. Figure 1.2 provides a brief indication of the progression of the model and circuit forms considered by this study.

The transistor models to be used in the numerical analyses of tuned power amplifiers are presented in Chapter 2. Each of the model forms presented is then used separately in Chapters 3, 4, and 5 to

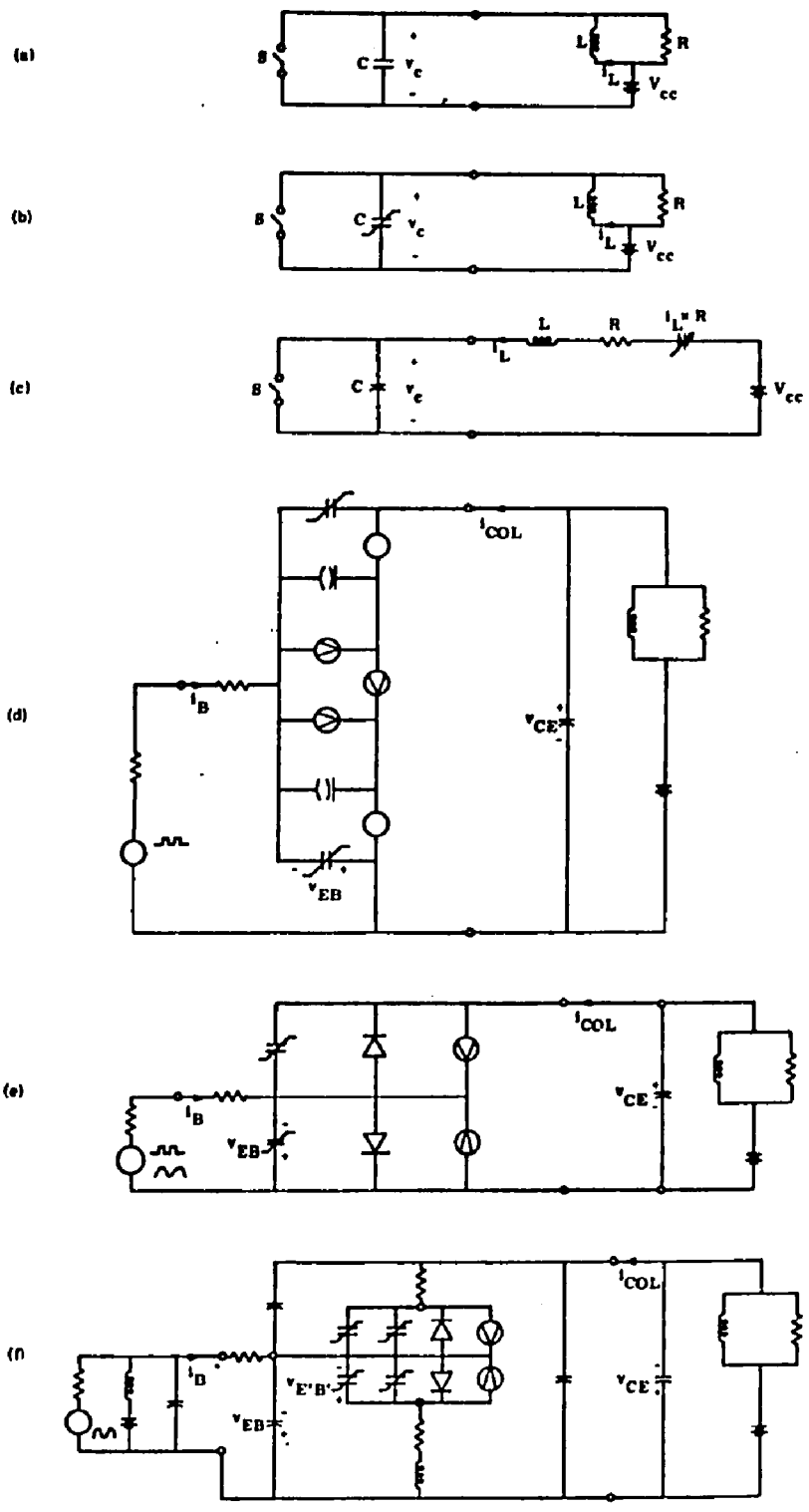

Fig. 1.2. Progression of device and circuit models

study amplifier behavior. Comparisons of the models is provided in Chapter 6 where they are each used to predict the performance features of a common amplifier. Chapter 7 presents the general conclusions of the study and suggests related areas for further consideration.

The simplest modeling of class C/D output circuits is shown on Fig. 1.2a where the transistor is modeled as a simple controlled switch with a fixed shunt capacitance, and the output tuning and matching network is taken to be a parallel RL network. As discussed in Section 3.2 a computer analysis program is used to study the effects of switch duty factor, supply voltage, and frequency in determining the $Y_{0_{Equiv}}$'s for obtaining maximum fundamental output power and for obtaining maximum efficiency. The relationships among output power, efficiency, bandwidth, and harmonic content are also investigated with the ideal switch transistor representation (Section 3.2).

By replacing the fixed shunt capacitance with a nonlinear voltage dependent capacity characteristic of semiconductor junction depletion layers as shown in Fig. 1.2b, the effects of a first order nonlinearity are investigated. In Section 3.3 the results of this investigation are contrasted to those of the fixed capacitance case which forms a reference standard used throughout this study.

The effect of the configuration of the tuning network in determining the equivalent admittances is investigated by changing the

output tuning and matching network to a series RL connection again using the ideal switch with fixed capacitance to represent the output characteristics of the transistor (Section 3.4). The ideal switch representation is also used to investigate the effects of harmonic tuning in the output circuits of RF power amplifiers (Section 3.5). This investigation considers both fixed and nonlinear switch capacitances to determine the significance of a nonlinear element to harmonic energy conversion.

With the insight gained through the idealized studies of class C amplifiers, emphasis is directed to predicting behavior of real VHF amplifiers. An intrinsic voltage controlled transistor model (Section 2.4.3) is used to predict the behavior of a low frequency, tuned output, pulsed input amplifier (Section 4.2). This model is also used to analyze a 100 MHz class C amplifier (Section 4.5). Experimental circuits are constructed, and their measured behaviors are used as comparisons to the behaviors predicted with the computed analyses (Sections 4.3 and 4.4).

Another 100 MHz amplifier experiment is performed to add the effects of input circuit tuning (Section 5.2), and this amplifier is modeled (Section 5.3) using an extended voltage controlled transistor model (Section 2.5). Again computed behavior is compared and contrasted to experimentally measured behavior.

A summary of the computational advantages and limitations of

each of the models is presented (Chapter 7). This includes cost-accuracy comparisons and computed results for one tuned amplifier example (Chapter 6).

CHAPTER 2

MODELING

2.1 Introduction

Several models used in the computer-aided analysis of VHF power amplifiers will be presented in this chapter together with experimental techniques useful for obtaining the model parameters. Many of the elements present in the models were suggested by observations of experimental amplifier behavior and by computer analysis of tuned power amplifiers. Although the models and modeling procedures will be presented here in a self-contained fashion, it was the interactions with the experimental and computed behaviors that prompted the inclusion of many of the model elements and the experimental techniques that are used for obtaining their quantitative descriptions.

2.2 Introduction of Model

Quantitative analyses of physical processes require mathematical descriptions of the processes. The circuit models and corresponding mathematical expressions chosen for representing the physical behavior of VHF power amplifiers determine the facility with which an analysis can be performed as well as the accuracy of the analysis. Generally, we can expect to improve analytical accuracy by increasing the size of our circuit and mathematical models. The anticipated

price to be paid for improved accuracy is one of increased complexity and time required for the analysis. An apparent practical limit to the maximum size appropriate for a model occurs when further size increases are found to produce insignificant changes in the analytical results, or as a final size limit, when results of further model expansions are lost in computational and measurement noises.

There are several popular large-signal circuit descriptions of intrinsic transistor properties. Notable among these are the classical Ebers-Moll voltage-controlled model (Ref. E1), the physics oriented Linvill voltage-controlled model (Ref. L3), and the mathematical charge-controlled description of Beaufoy-Sparkes (Ref. B1). For a consistent set of approximations, these models can be shown to be mathematically equivalent (Ref. K1); however, because of the different choices in the controlling independent variables, computational differences in dynamic ranges and severities of nonlinearity in various operating regions can affect the computational advantages of one model relative to another (Ref. M1). Neglecting these computational differences between the models, a lumped charge-controlled time-domain model is selected initially because it closely resembles the physical process and also lends itself to a succinct circuit representation. This model can be considered as the basis for the formulation of all the other model forms to be presented. The notation used for the

charge-controlled model[1] (Fig. 2.1) of an intrinsic NPN transistor and its defining equations (Eqs. 2.1 - 2.4) are basically those of Ref. P2.

$$i'_B = \frac{q_F}{\tau_{BF}} + \dot{q}_F + \frac{q_R}{\tau_{BR}} + \dot{q}_R - C_{EDEP}\,\dot{v}_{E'B'} - C_{CDEP}\,\dot{v}_{C'B'} \tag{2.1}$$

$$i'_{COL} = \frac{q_F}{\tau_F} - q_R\left(\frac{1}{\tau_R} + \frac{1}{\tau_{BR}}\right) - \dot{q}_R + C_{CDEP}\,\dot{v}_{C'B'} \tag{2.2}$$

$$q_F = Q_{FS}\left(e^{-\lambda v_{E'B'}} - 1\right) \tag{2.3}$$

$$q_R = Q_{RS}\left(e^{-\lambda v_{C'B'}} - 1\right) \tag{2.4}$$

These equations result from the solution of a lumped representation of a one-dimensional, field-free, diffusion equation approximating minority carrier motion in a narrow base region of a junction transistor. Approximations of space charge neutrality, no carrier recombination or generation in the space charge region, and no potential drops except at the junctions have also been made in the derivation of these charge-controlled equations.

The junction depletion layer capacitances, C_{EDEP} and

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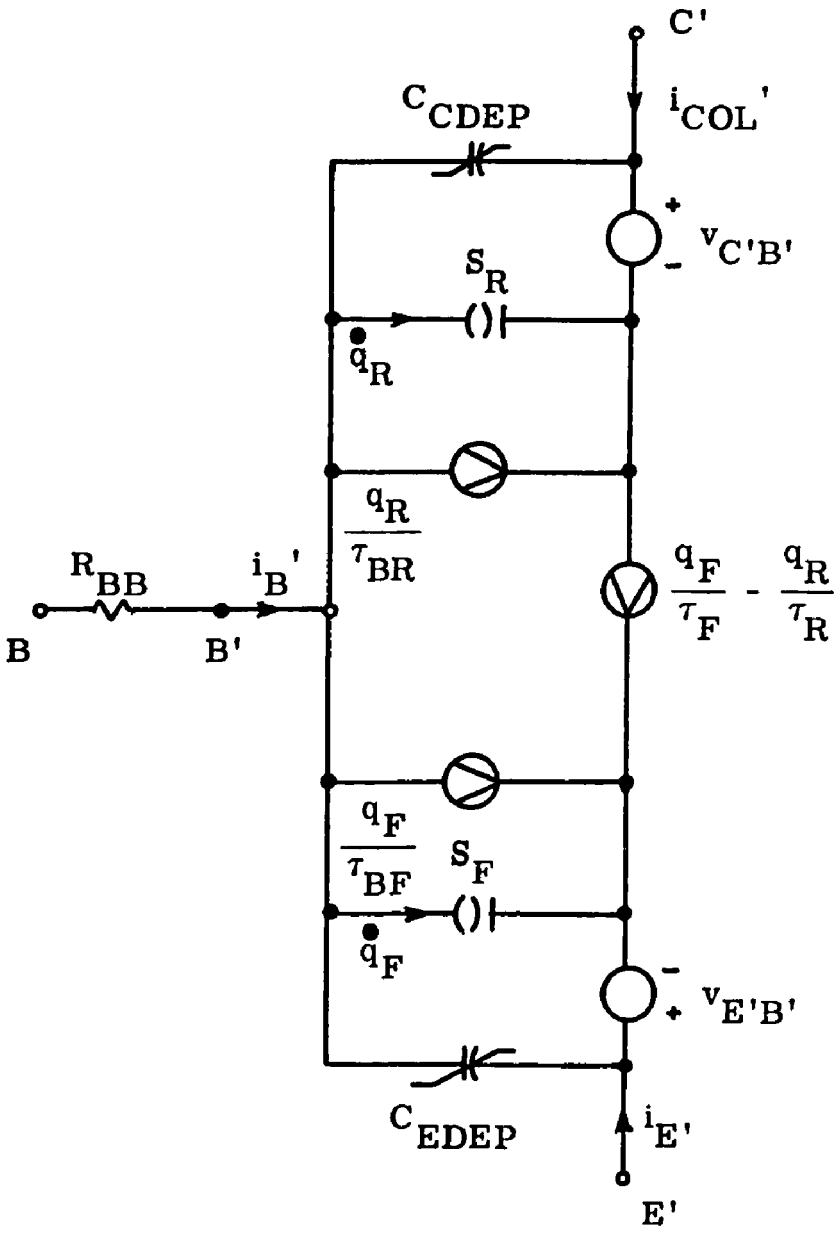
[1] The elements S_F and S_R are termed the forward and reverse charge stores respectively. A charge store is defined as an electrical element with the property that the store potential is always zero and the current through the store is equal to the time rate of change of the stored charge.



$$i_B' = \frac{q_F}{\tau_{BF}} + \dot{q}_F + \frac{q_R}{\tau_{BR}} + \dot{q}_R - C_{EDEP}\dot{v}_{E'B'} - C_{CDEP}\dot{v}_{C'B'}$$

$$i_{COL}' = \frac{q_F}{\tau_F} - q_R\left(\frac{1}{\tau_R} + \frac{1}{\tau_{BR}}\right) - \dot{q}_R + C_{CDEP}\dot{v}_{C'B'}$$

$$q_F = Q_{FS}\left(e^{-\lambda v_{E'B'}} - 1\right)$$

$$q_R = Q_{RS}\left(e^{-\lambda v_{C'B'}} - 1\right)$$

Fig. 2.1. Intrinsic charge-controlled model of NPN transistor

C_{CDEP} are appended to the intrinsic model after the solution of the diffusion equation to account for the energy stored in immobile charges in the space charge regions (Ref. P2). A base spreading resistance R_{BB} is often added also to simulate ohmic potential drops that result from transverse majority carrier motion in the base region (Ref. P2).

2.3 Determination of Model Parameters

In order to make the model useful for numerical computations relating to a given transistor type, experimental methods can be employed to determine the numerical values and behaviors of the model parameters to describe the specific device. The parameters required for completing the intrinsic charge-controlled model description are:

α_F, α_R:	common base dc forward and reverse current transport factors
τ_F, τ_R:	recombination time constants for emitter-base and collector-base junctions
Q_{FS}, Q_{RS}:	saturation charge constants for the emitter-base and collector-base junction behaviors
C_{EDEP}, C_{CDEP}:	emitter-base and collector-base depletion layer capacitances
λ:	exponential constant $\frac{mq}{KT}$
R_{BB}:	base spreading resistance

with

$$\tau_{BF} \triangleq \frac{\alpha_F}{1 - \alpha_F} \cdot \tau_F$$

$$\tau_{BR} \triangleq \frac{\alpha_R}{1 - \alpha_R} \cdot \tau_R$$

There are various methods that can be used to determine the required parameter values from experimental measurements of device behavior. The following techniques have been used to establish parameter values for a type 2N3866 VHF transistor.

2.3.1 α_F and α_R From Curve Tracer Measurements. The device forward and inverse current gains β_F and β_R can be determined over a wide range of current-voltage operating conditions with conventional curve tracer measurements (Ref. H3, Chapter 7). The common-base current gains are then obtained by applying the simple relationship $\alpha = \frac{\beta}{\beta+1} = 1 - \frac{1}{\beta+1}$. Quite often, however, problems with oscillations, excessive power dissipations, junction temperature variations, and accuracy preclude the use of this simple measurement. In such instances more specialized direct or pulsed measurements may be required, but for present purposes the curve tracer measurements are adequate. Figures 2.2 and 2.3 show the results of forward and inverse beta measurements of three 2N3866 transistors over a wide range of collector and emitter currents. Figures 2.4 and 2.5 illustrate the effects of junction potential variations for one of the transistors.

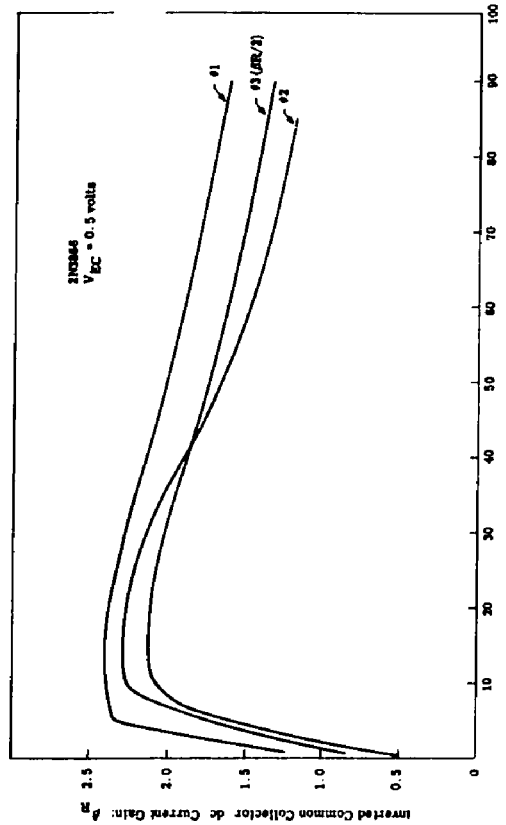


Fig. 2.3. Inverse current gain

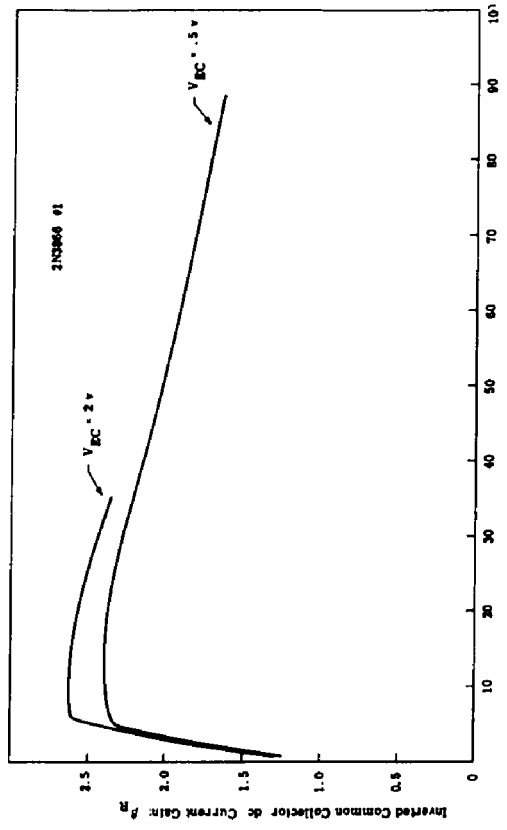


Fig. 2.5. Effect of junction potential on inverse gain

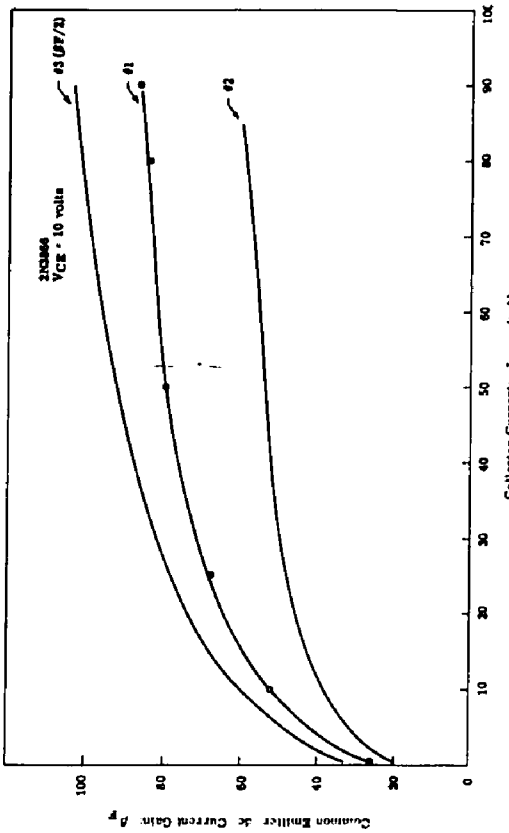


Fig. 2.2 Forward current gain

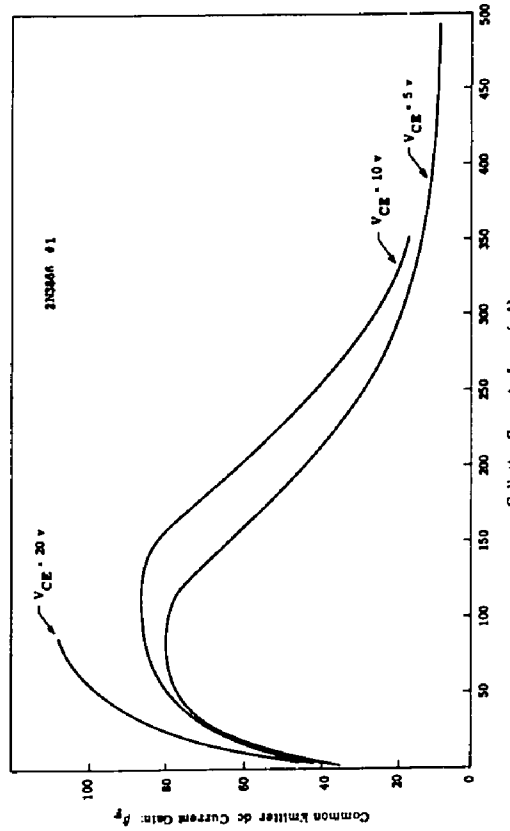


Fig. 2.4. Effect of junction potential on forward gain

For transistor #1 in the relatively large region 20 ma $< I_{COL} <$ 150 ma, 5 volts $< V_{CE} <$ 15 volts; we find $70 \lesssim \beta_F \lesssim 90$. Approximating β_F as a constant, 80, in this region leads to the value $\alpha_F = 0.988$ which will be used in the computer simulation studies. Similarly for 20 ma $< I_E <$ 150 ma, 0.5 volts $< V_{EC}$ $<$ 2.0 volts, we find $1.5 \lesssim \beta_R \lesssim 2.0$ and approximate $\alpha_R \approx 0.667$.

2.3.2 Charge Parameters Determined with Pulse Transient Measurements. A useful method for determining the time constants of a charge-control model has been proposed by Hegedus (Ref. H6). This method employs pulse transient techniques to identify the time constants of the model and to determine how they vary with regard to terminal voltages and currents. Basically, the technique separates the effects of the two junctions by selectively forward biasing one of them while reverse biasing the other. For example, if the emitter-base junction is forward biased and the collector-base junction is reverse biased, the predominant charge stored in the base region is q_F, and q_R and $\dot{q}_R$ may be neglected. Thus, the charge-control equations can be approximated by

$$i_B' = \frac{q_F}{\tau_{BF}} + \dot{q}_F + \frac{q_R}{\tau_{BR}} + \dot{q}_R - i_{C_{EDEP}} - i_{C_{CDEP}}$$

$$\approx \frac{q_F}{\tau_{BF}} + \dot{q}_F - i_{C_{EDEP}} - i_{C_{CDEP}} \qquad (2.5)$$

$$i'_{COL} = \frac{q_F}{\tau_F} - q_R\left(\frac{1}{\tau_R} + \frac{1}{\tau_{BR}}\right) - \dot{q}_R + i_{C_{CDEP}}$$

$$\approx \frac{q_F}{\tau_F} + i_{C_{CDEP}} \qquad (2.6)$$

where

$$i_{C_{EDEP}}(t) = C_{EDEP}(v_{E'B'}) \frac{dv_{E'B'}(t)}{dt}$$

$$i_{C_{CDEP}}(t) = C_{CDEP}(v_{C'B'}) \frac{dv_{C'B'}(t)}{dt}$$

If a pulse of collector current is stimulated by an emitter excitation as indicated in Fig. 2.6, the resulting base current (i'_B) will be composed of a static term which is the recombination current (q_F/τ_{BF}), and two transient terms: one to build up the stored base charge (q_F) and a second to charge the depletion layer capacitances ($i_{C_{EDEP}}$, $i_{C_{CDEP}}$). Integration of the base current transient terms yields the base charge stored in the base and depletion layer regions, viz.

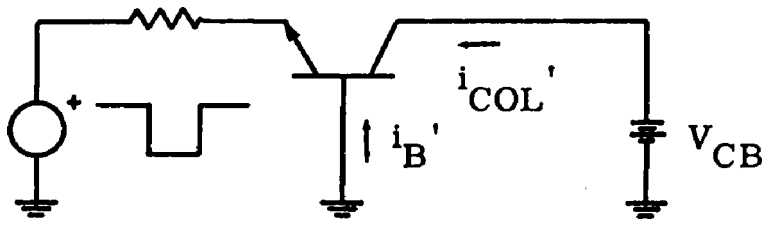


Fig. 2.6. Charge storage measurement

$$Q_{B_{stored}} = \int_{transient} i'_B \, dt \quad [1]$$

$$= \int \dot{q}_F \, dt - \int i_{C_{EDEP}} \, dt - \int i_{C_{CDEP}} \, dt \qquad (2.7)$$

With the measurement technique used, the collector-base voltage ($v_{C'B'}$) is held constant so that the $i_{C_{CDEP}}$ term can be neglected. As a result

$$Q_{B_{stored}} \approx q_F + Q_{C_{EDEP}} \qquad (2.8)$$

with

$$Q_{C_{EDEP}} \triangleq - \int_{transient} i_{C_{EDEP}} \, dt$$

Combining Eqs. 2.6 and 2.8 results in an expression that relates the stored charge linearly to the collector current.

$$Q_{B_{stored}} \approx \tau_F i'_{COL} + Q_{C_{EDEP}} \qquad (2.9)$$

(forward region)

Similarly by reverse biasing the emitter-base junction and exciting a known pulse amplitude of emitter current we get:

---

[1] $\int_{transient} i'_B \, dt$ means integrating the two transient terms of the total base current and excluding the static term. Refer to Appendix A for details of the related experimental technique.

$$Q_{B_{stored}} \approx \tau_R i'_E + Q_{C_{CDEP}} \quad \text{(inverse region)} \tag{2.10}$$

The experimental procedure for determining Q_B involves electronic integration of the transient base current waveform for various levels of steady state collector current (Appendix A). A plot of this stored charge versus the collector current (Eq. 2.9) will then reveal the time constant (τ_F) as the slope and the depletion capacitance charge $\left(Q_{C_{EDEP}}\right)$ as the intercept.

Experimental measurements of stored charge have been taken at various values of current and junction potentials for the three 2N3866 transistors. The results are shown in Figs. 2.7 and 2.8. For the forward bias measurement the straight-line relationship predicted theoretically is seen to occur experimentally in the region of collector currents from 10 to 200 milliamperes. In this region the slope, τ_F, is found to be 1.1×10^{-10} second. In the region of higher collector currents the value for τ_F increases rapidly whenever the current exceeds a threshold value dependent on the external collector-base bias potential. This rapid increase in time constant can be attributed to saturation of the intrinsic collector-base junction due to a resistive potential drop in the bulk collector region. For example, the knee of the stored charge curve for transistor #1 with a bias voltage of 10.0 volts occurs at a collector current of approximately 200.00 milliamperes. From this behavior we might infer an effective collector

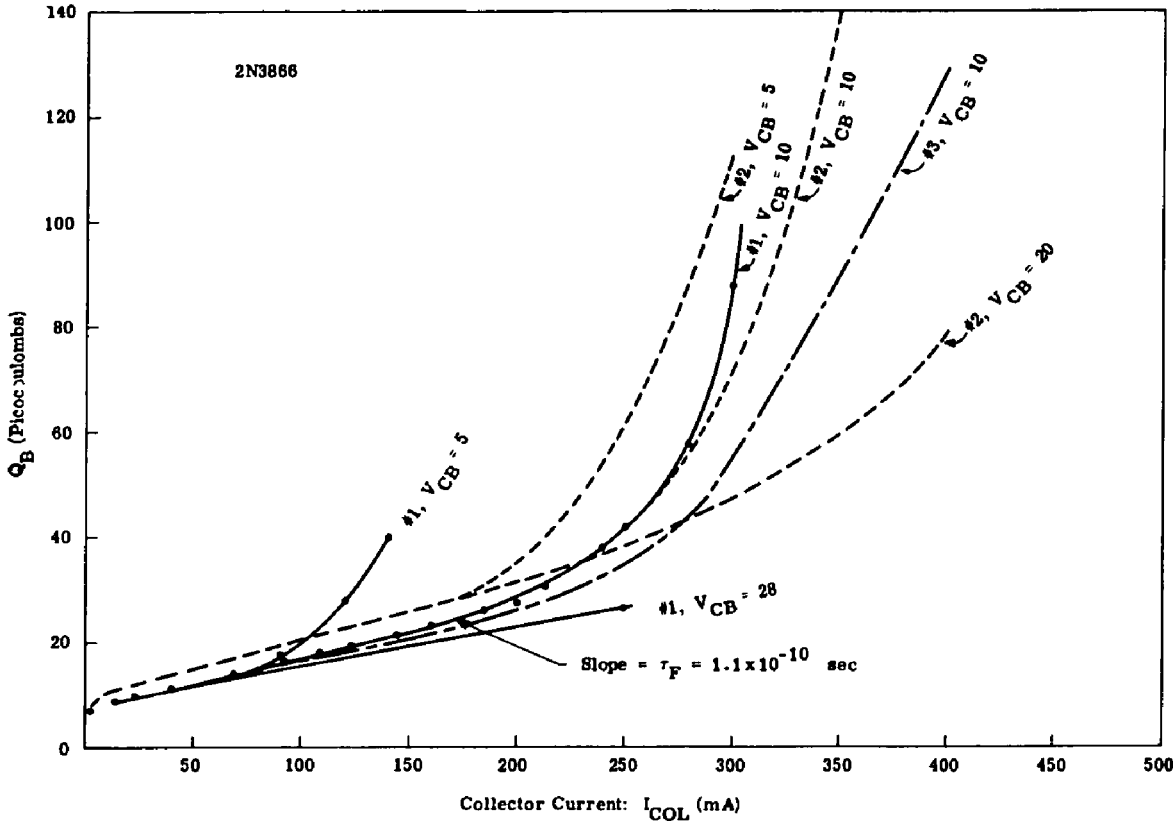


Fig. 2.7. Forward charge storage

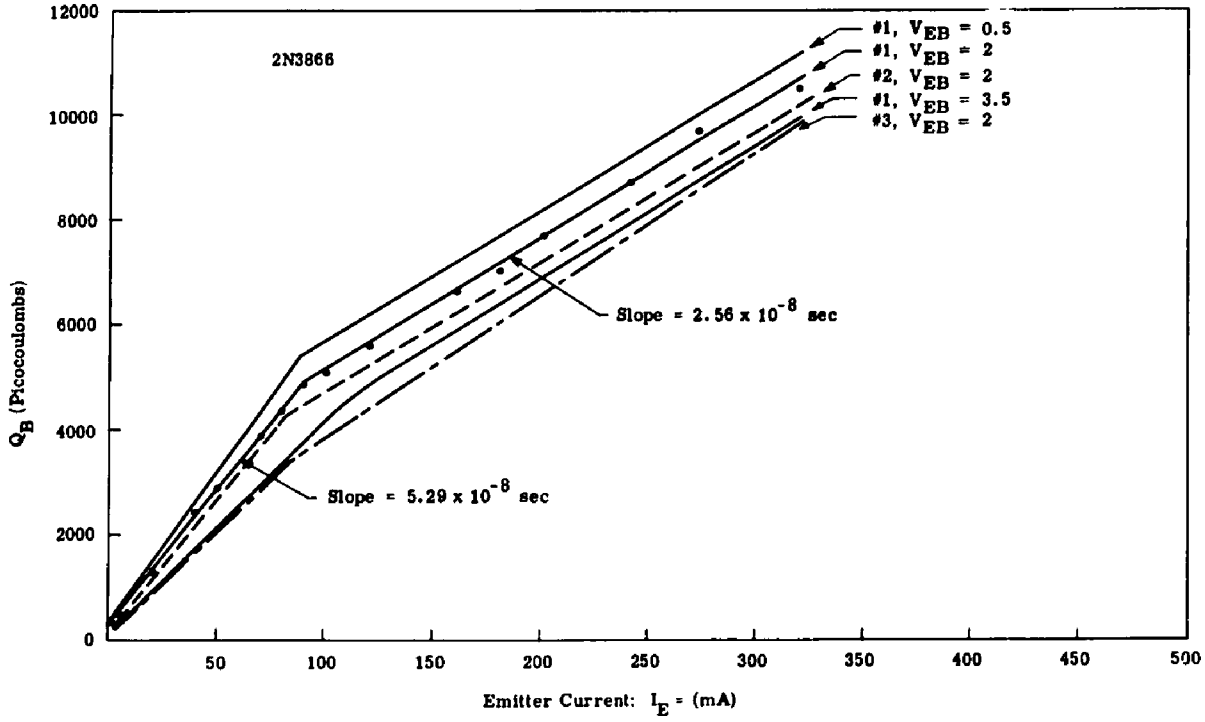


Fig. 2.8. Inverse charge storage

bulk resistance of 50.0 ohms. Conversely, the absence of such saturation effects in the inverse measurement implies that the emitter bulk resistance is less than 0.5 volts/350. mA or 1.4 ohm. Further consideration of these bulk resistances will be given in Section 2.5.3.

From the measurements in the inverse region of transistor operation the reverse charge time constant, τ_R, appears to be 5.29×10^{-8} second for emitter currents less than 80.0 milliamperes and decreases to 2.56×10^{-8} second when the emitter current exceeds 100.0 milliamperes. For convenience single values ($\tau_F = 1.1 \times 10^{-10}$ and $\tau_R = 2.56 \times 10^{-8}$) will be taken as representative of the 2N3866 device behavior in the operating regions anticipated for the large signal simulations.

2.3.3 λ, Q_{FS}, and Q_{RS} from DC Behavior of Junctions.

The steady-state base current $I_{b'c'}$ resulting from an applied base-collector potential $V_{b'c'}$ with an emitter current of zero can be expressed from Eqs. 2.1 - 2.4 as

$$I_{b'c'}\Big|_{I'_e=0} = \frac{(1 - \alpha_F\alpha_R)\, Q_{RS}}{\alpha_R\, \tau_R} \left(e^{\lambda V_{b'c'}} - 1\right) \qquad (2.11)$$

Similarly, for the base-emitter junction

$$I_{b'e'}\Big|_{I'_{COL}=0} = \frac{(1 - \alpha_F\alpha_R)\, Q_{FS}}{\alpha_F\, \tau_F} \left(e^{\lambda V_{b'e'}} - 1\right) \qquad (2.12)$$

For forward bias junction potentials greater than 100 millivolts, $e^{\lambda V} >> 1$. In this region, for example,

$$\ell n\left[\frac{I_{b'c'}\,\alpha_R\,\tau_R}{(1-\alpha_F\alpha_R)\,Q_{RS}}\right] \approx \lambda V_{b'c'} \qquad (2.13)$$

and semi-logarithmic plots of the characteristics for the emitter-base and collector-base junctions are expected to be straight lines with slopes of λ.

Experimental data[1] for a 2N3866 transistor are plotted in Fig. 2.9 and the slopes of both the base-collector and the base-emitter characteristics indicate a λ value of 21.3 (volts^{-1}) suitable for base currents greater than 500 microamperes. For base currents less than 500 microamperes, the slope changes to suggest λ = 29.3 (volts^{-1}).

Evaluation of Q_{RS} and Q_{FS} can be made by substitution of experimental I-V data points into Eqs. 2.11 and 2.12.

$$Q_{RS} \approx \frac{I_{b'c'}\alpha_R\tau_R}{(1-\alpha_F\alpha_R)}\, e^{-\lambda V_{b'c'}}\Bigg|_{\substack{V_{b'c'}=0.796\text{ volt}\\ I_{b'c'}=10\text{ mA}}} = 1.16\times10^{-18}\text{ coulomb}$$

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[1] For this data it is assumed that the junction potentials were the same as the potentials applied to the device terminals; i.e., for the low current levels involved, ohmic potential drops in the bulk semiconductor material can be neglected.

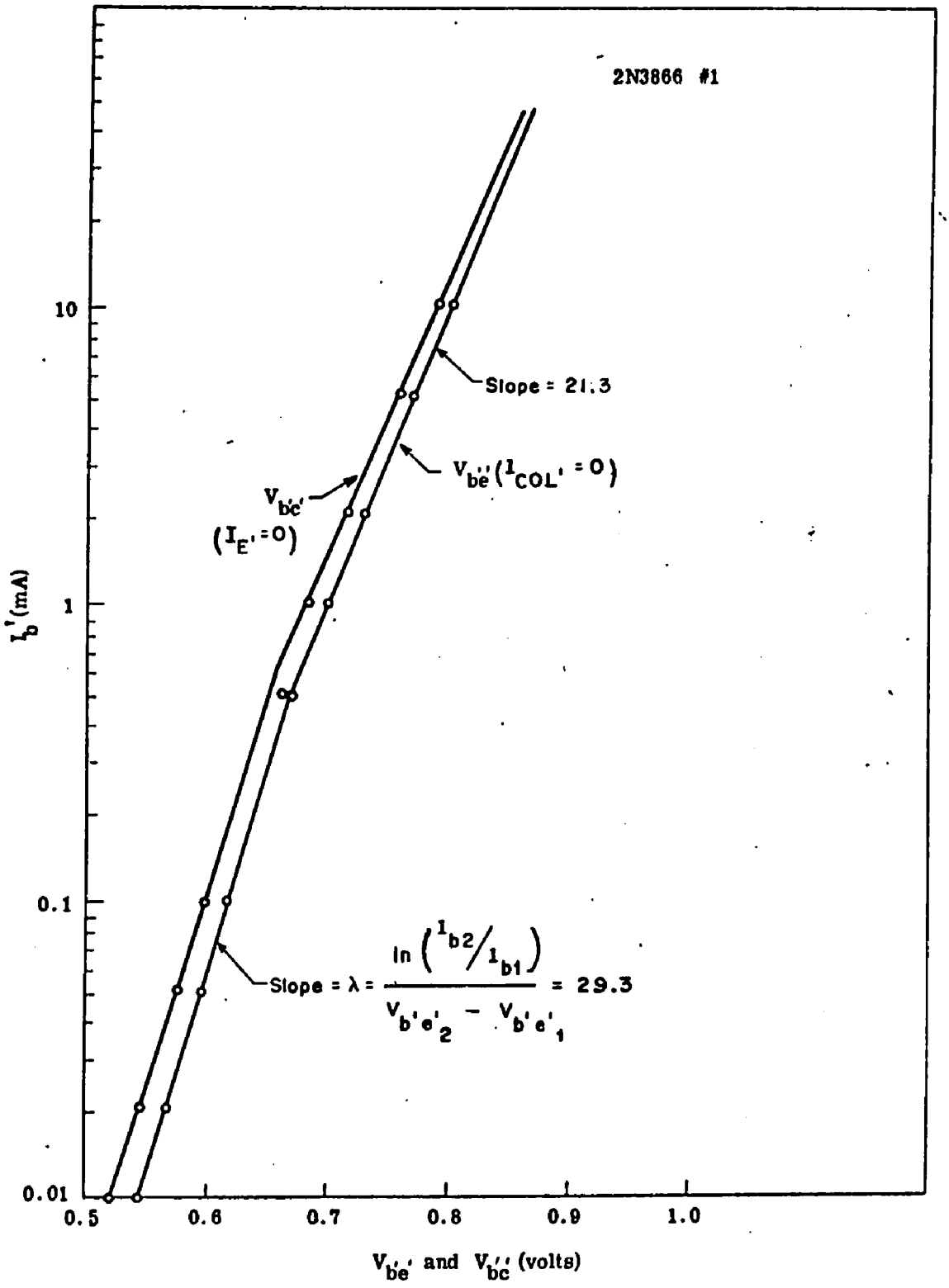


Fig. 2.9. Static behavior of junctions

$$Q_{FS} \approx \frac{I_{b'c'}\alpha_F\tau_F}{(1-\alpha_F\alpha_R)} e^{-\lambda V_{b'e'}} \Bigg|_{\substack{V_{b'e'}=0.808 \text{ volt} \\ I_{b'e'}=10 \text{ mA}}} = 4.66\times10^{-21} \text{ coulomb}$$

with $\alpha_F = 0.988$, $\alpha_R = 0.667$, $\tau_F = 1.1\times10^{-10}$, $\tau_R = 2.56\times10^{-8}$, $\lambda = 21.3$.

2.4 Numerical Difficulty with Charge Controlled Model

Computer analysis using the charge controlled transistor model of Fig. 2.1 is subject to a numerical difficulty--the dynamic range of the charge variables can exceed the dynamic range of the computer. This difficulty is easily illustrated by a simple example.

For the IBM 360/67 machine the smallest argument permissible for computing natural logarithms is on the order of 10^{-70}. Recalling the form of an equation for one of the junction potentials, e.g., $v_{E'B'} = -(1/\lambda)\,\ell n\left(1 + \frac{q_F}{Q_{FS}}\right)$, we see that the largest reverse bias potential that can be computed is limited by the argument of the natural logarithm. In this example, the machine limit of 10^{-70} for the argument corresponds to the largest reverse bias potential that can be handled directly. This limit on the potential would be

$$v_{E'B'_{\substack{\max \\ \text{reverse}}}} = \frac{\ell n(10^{-70})}{-\lambda} = 4.025 \text{ volts}$$

For typical class C amplifiers we expect to encounter reverse

junction potentials well in excess of this 4 volt limit, and some technique must be employed to overcome this limitation. Several circuit modifications and the related numerical modifications to extend the dynamic range of the charge control model are suggested in the following three sections.

2.4.1 Numerical Approximation with Shunt Resistance. As one possibility for overcoming the numerical limit to the reverse bias potential, consider shunting each semiconductor junction with a large resistance as the numerical logarithmic limit is approached. Using a single diode junction for an example (Fig. 2.10), the equations to be solved under forward bias and small reverse bias conditions would be

$$\left[1 + \frac{C_{DEP}(v)}{\lambda Q_S(1 + q/Q_S)}\right] \dot{q} = -\frac{q}{\tau} + i \qquad (2.14)$$

$$v = (1/\lambda)\, \ell n \left(1 + \frac{q}{Q_S}\right) \qquad (2.15)$$

$$i = \frac{v_S - v}{R_S} \qquad (2.16)$$

Now suppose we choose a small limiting value of the logarithmic argument, ϵ, which is slightly larger than the machine limit.

$$\epsilon = 1 + \frac{q_{LIM}}{Q_S} > 10^{-70}$$

This corresponds to determining a limiting value for reverse bias potential.

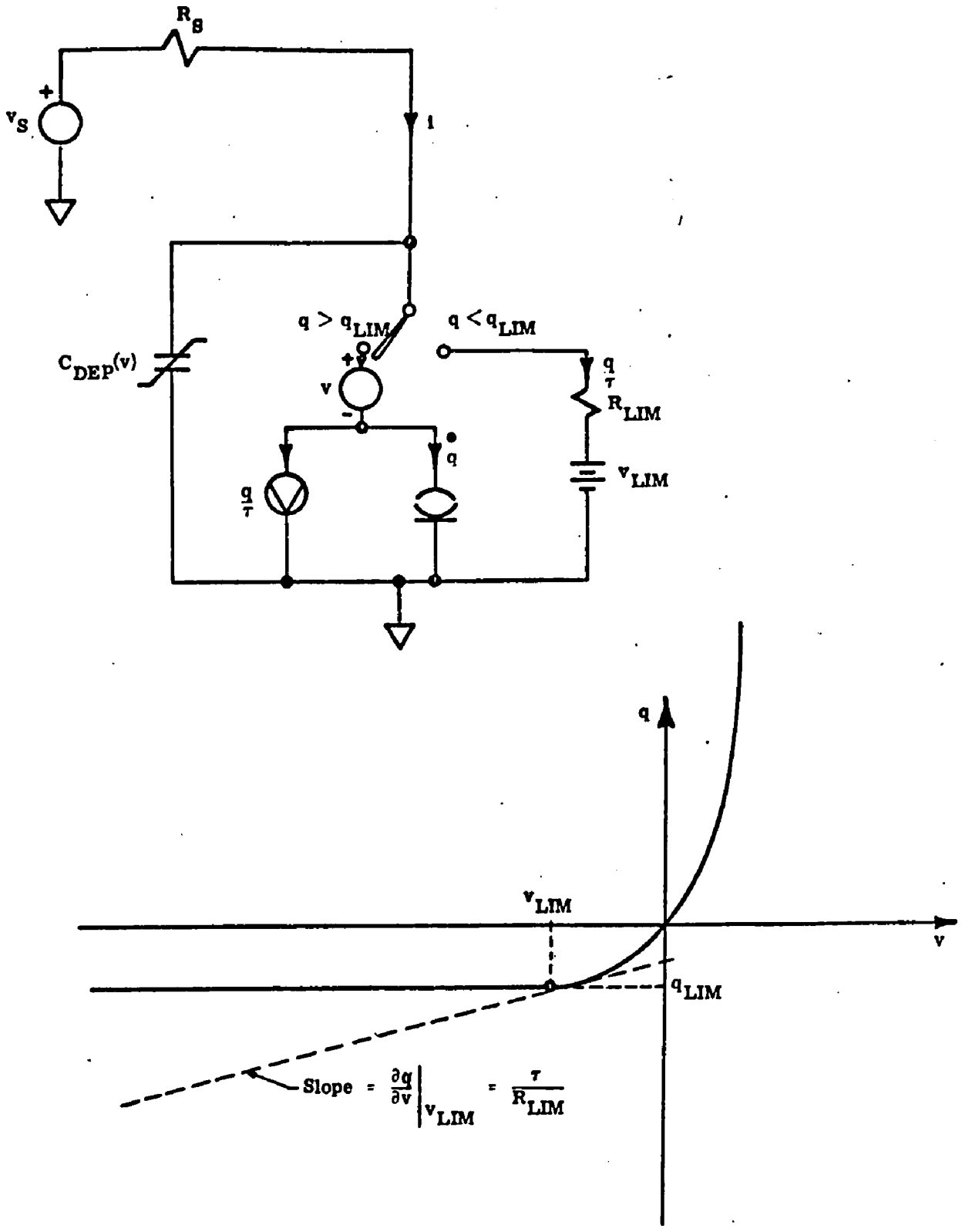


Fig. 2.10. Diode with shunt resistance to avoid numerical limit

$$v_{LIM} = -\frac{1}{\lambda} \ell n(\epsilon)$$

When this limiting potential is exceeded in the computation, the diode equations can be approximated as:

$$\left(\frac{C_{DEP}(v) \cdot R_{LIM}}{\tau}\right) \dot{q} = -\frac{q}{\tau} + i \tag{2.18}$$

$$v = \frac{R_{LIM}}{\tau} q + v_{LIM} \tag{2.19}$$

$$i = \frac{v_S - v}{R_S} \tag{2.20}$$

where

$$R_{LIM} = \left.\frac{\partial v}{\partial \frac{q}{\tau}}\right|_{v_{LIM}} = \frac{\lambda Q_S}{\tau} \left(1 + \frac{q_{LIM}}{Q_S}\right) \tag{2.21}$$

and

$$q_{LIM} \triangleq Q_S(\epsilon - 1)$$

This procedure is illustrated graphically in Fig. 2.10 and provides an effective method for extending the computational dynamic range of the charge control model.

2.4.2 Numerical Approximation with Shunt Capacitance. As an alternate procedure we could switch in a limiting value of shunt capacitance instead of the shunt resistance (Fig. 2.11). In a manner similar to that used for the shunt resistance, we define a capacitance

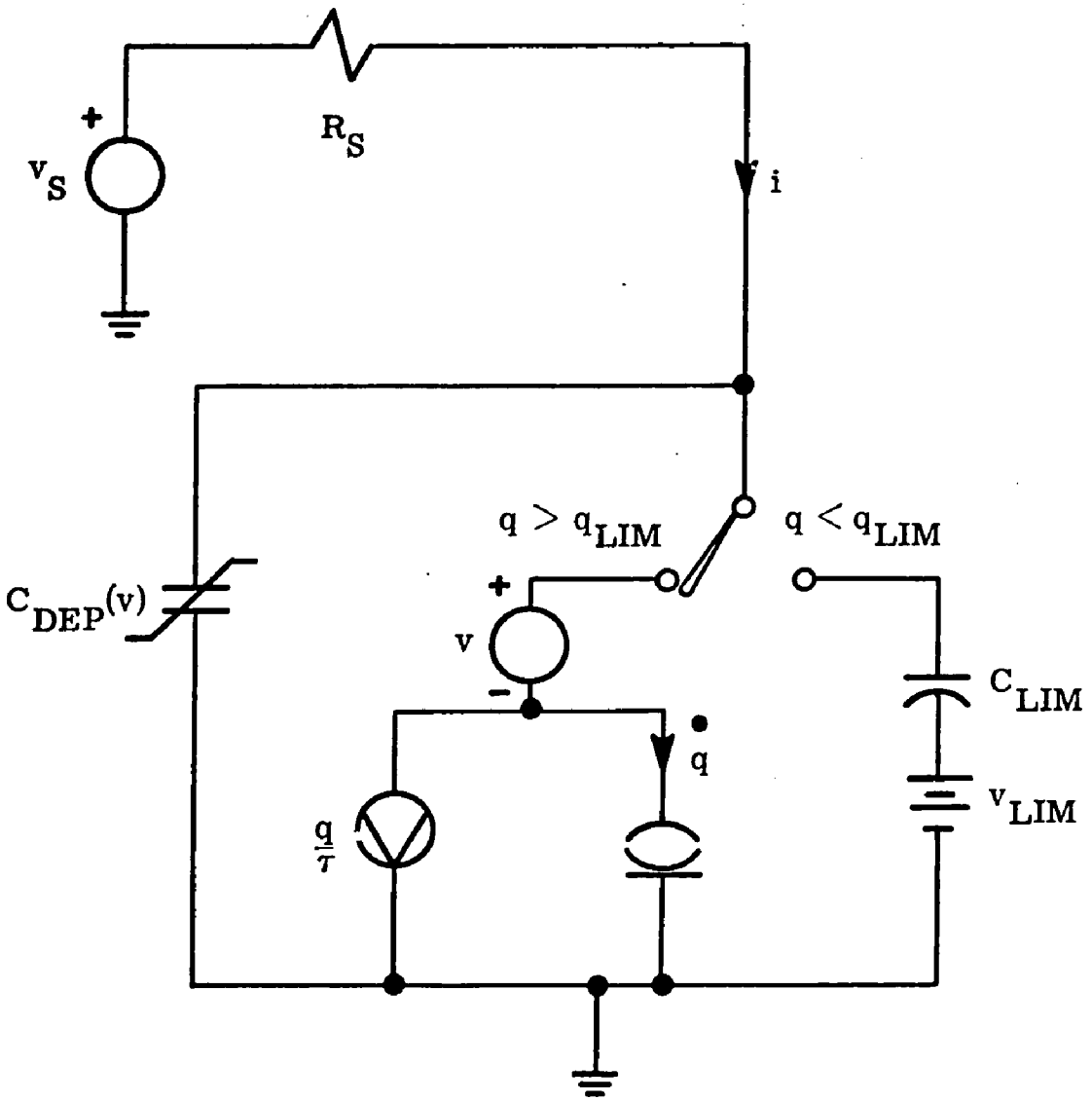


Fig. 2.11. Diode with shunt capacitance to avoid numerical limit

$$C_{LIM} = \frac{q_{LIM}}{v_{LIM}} \tag{2.22}$$

and when the limiting potential is exceeded, we are left with the equations

$$\left[\frac{C_{LIM} + C_{DEP}(v)}{\lambda Q_S\left(1 + \frac{q}{Q_S}\right)}\right] \dot{q} = i \tag{2.23}$$

$$v = \frac{q}{C_{LIM}} + V_{LIM} \tag{2.24}$$

$$i = \frac{v_S - v}{R_S} \tag{2.25}$$

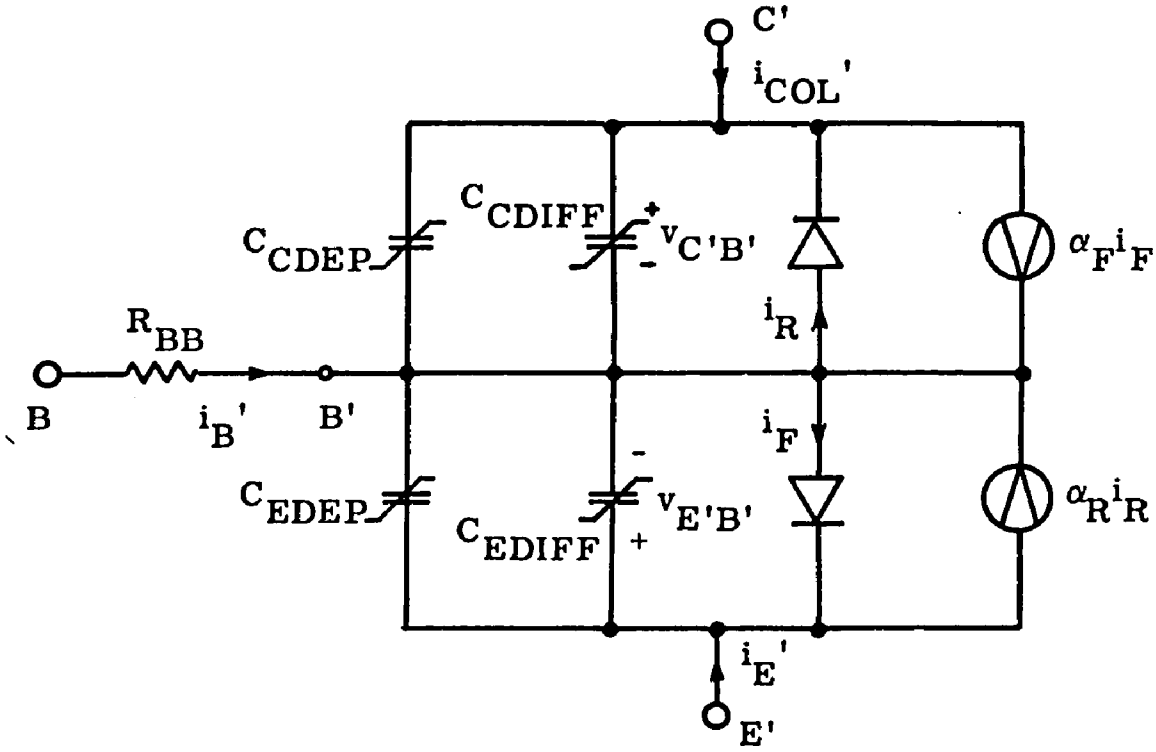
2.4.3 Transformation to Voltage-Control Model. A third approach that can be used to circumvent the numerical difficulties involved in dealing with large reverse-bias potentials with the charge-control model is to transform the charge-control equations to an equivalent set of voltage-control equations and to shift the state variables from charge to voltage. This change of controlling variable from charge to voltage is demonstrated in Appendix B and results in the intrinsic voltage controlled transistor model described by Eqs. 2.26 - 2.31 and illustrated in Fig. 2.12.

$$i'_B = (1 - \alpha_F)\, i_F - C_{E_{DIFF}}\, \dot{v}_{E'B'} + (1 - \alpha_R)\, i_R - C_{CDIFF}\, \dot{v}_{C'B'} - C_{EDEP}\, \dot{v}_{E'B'} - C_{CDEP}\, \dot{v}_{C'B'} \tag{2.26}$$

$$i'_{COL} = \alpha_F\, i_F - i_R + C_{CDIFF}\, \dot{v}_{C'B'} + C_{CDEP}\, \dot{v}_{C'B'} \tag{2.27}$$

$$i_F = \frac{Q_{FS}}{\alpha_F\, \tau_F} \left(e^{-\lambda v_{E'B'}} - 1 \right) \tag{2.28}$$

$$i_R = \frac{Q_{RS}}{\alpha_R\, \tau_R} \left(e^{-\lambda v_{C'B'}} - 1 \right) \tag{2.29}$$



$$i_B' = (1-\alpha_F)\, i_F - C_{EDIFF}\, \dot{v}_{E'B'} + (1-\alpha_R)\, i_R - C_{CDIFF}\, \dot{v}_{C'B'} - C_{EDEP}\, \dot{v}_{E'B'} - C_{CDEP}\, \dot{v}_{C'B'}$$

$$i_{COL}' = \alpha_F i_F - i_R + C_{CDIFF}\, \dot{v}_{C'B'} + C_{CDEP}\, \dot{v}_{C'B'}$$

$$i_F = \frac{Q_{FS}}{\alpha_F \tau_F}\left(e^{-\lambda v_{E'B'}} - 1\right)$$

$$i_R = \frac{Q_{RS}}{\alpha_R \tau_R}\left(e^{-\lambda v_{C'B'}} - 1\right)$$

$$C_{EDIFF} = \lambda Q_{FS}\, e^{-\lambda v_{E'B'}}$$

$$C_{CDIFF} = \lambda Q_{RS}\, e^{-\lambda v_{C'B'}}$$

Fig. 2.12. Intrinsic voltage controlled model of NPN transistor

$$C_{EDIFF} = \lambda Q_{FS} e^{-\lambda v_{E'B'}} \tag{2.30}$$

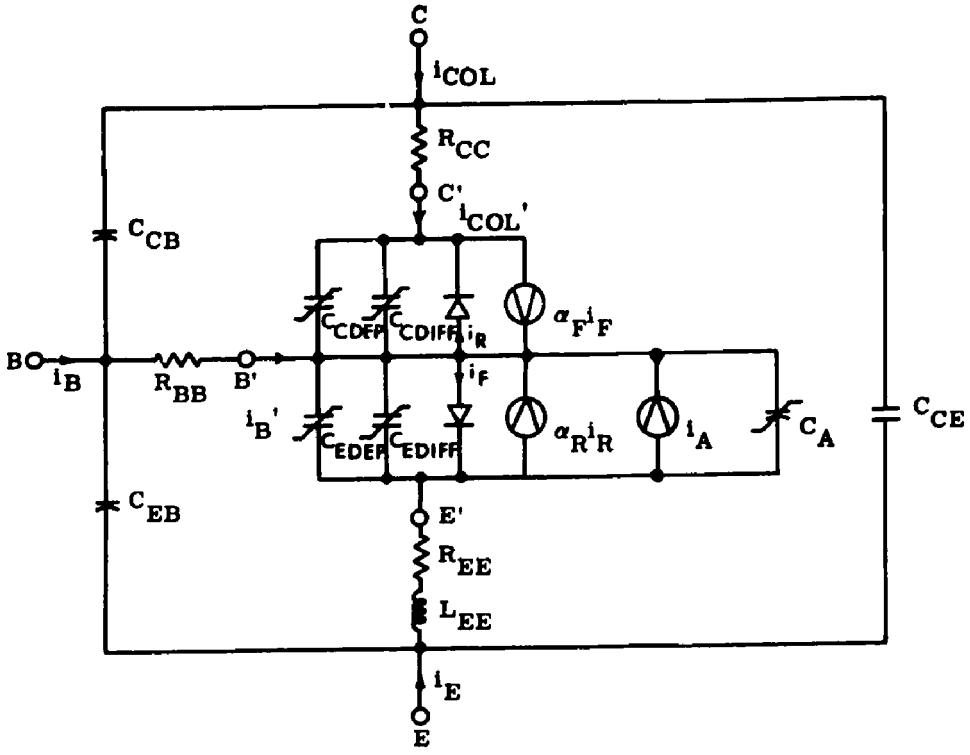
$$C_{CDIFF} = \lambda Q_{RS} e^{-\lambda v_{C'B'}} \tag{2.31}$$

This model is essentially a dynamic Ebers-Moll model and as mentioned previously is mathematically (but not computationally) identical to the charge controlled model. The parameters have been left in the form of the charge parameters to enhance the relationship between the two models. This transformation from charge control variables to voltage control variables for the transistor model provides a useful method for achieving the numerical range required for analyses of large signal amplifiers and will be used for the analyses considered in this study.

2.5 Extended Voltage Controlled Transistor Model

In order to account for several important large-signal and high-frequency characteristics of VHF power transistors not contained in the intrinsic transistor models, the intrinsic model has been extended by the addition of fixed extrinsic elements (R_{BB}, R_{CC}, R_{EE}, L_{EE}, C_{EB}, C_{CB}, C_{CE}) and controlled avalanche current elements (i_A, C_A). The resultant extended voltage controlled transistor model (Eqs. 2.26 - 2.35 and Fig. 2.13) is a nonlinear wideband description of a NPN transistor.

$$C_{EDEP} = \frac{C_{JE}}{(VZE + v_{E'B'})^{\gamma_E}} + C_{FE} \tag{2.32}$$



$$i_B' = (1 - \alpha_F)\, i_F - C_{E_{DIFF}}\, \dot{v}_{E'B'} + (1 - \alpha_R)\, i_R$$

$$- C_{CDIFF}\, \dot{v}_{C'B'} - C_{EDEP}\, \dot{v}_{E'B'} - C_{CDEP}\, \dot{v}_{C'B'}$$

$$i_{COL}' = \alpha_F i_F - i_R + C_{CDIFF}\, \dot{v}_{C'B'} + C_{CDEP}\, \dot{v}_{C'B'}$$

$$i_F = \frac{Q_{FS}}{\alpha_F \tau_F} \left(e^{-\lambda v_{E'B'}} - 1 \right)$$

$$i_R = \frac{Q_{RS}}{\alpha_R \tau_R} \left(e^{-\lambda v_{C'B'}} - 1 \right)$$

$$C_{EDIFF} = \lambda Q_{FS}\, e^{-\lambda v_{E'B'}}$$

$$C_{CDIFF} = \lambda Q_{RS}\, e^{-\lambda v_{C'B'}}$$

$$C_{EDEP} = \frac{C_{JE}}{(VZE + v_{E'B'})^{\gamma_E}} + C_{FE}$$

$$C_{CDEP} = \frac{C_{JC}}{(VZC + v_{C'B'})^{\gamma_C}} + C_{FC}$$

$$i_A = \frac{Q_{FS}}{\alpha_F \tau_F} \left[\frac{1}{1 - (v_{E'B'}/V_A)^{N_A}} - 1 \right], \quad C_A = \frac{\tau_F\, i_A}{V_A - v_{E'B'}}$$

Fig. 2.13. Extended voltage controlled model of NPN transistor

$$C_{CDEP} = \frac{C_{JC}}{(VZC + v_{C'B'})^{\gamma_C}} + C_{FC} \tag{2.33}$$

$$i_A = \frac{Q_{FS}}{\alpha_F \tau_F} \left[\frac{1}{1 - (v_{E'B'}/V_A)^{N_A}} - 1 \right] \tag{2.34}$$

$$C_A = \frac{\tau_F i_A}{V_A - v_{E'B'}} \tag{2.35}$$

The expressions for the depletion capacitances (Eqs. 2.32 and 2.33) apply to the intrinsic model as well as this extended model. Experimental determination of the depletion capacitance and the extrinsic element parameters is considered in the following sections.

2.5.1 Model Capacitances. Neglecting the avalanche capacitance,[1] the emitter-base and collector-base capacitances each consist of three components:

$$C_E = C_{EDIFF} + C_{EDEP} + C_{ECASE} \tag{2.36}$$

$$C_C = C_{CDIFF} + C_{CDEP} + C_{CCASE} \tag{2.37}$$

diffusion components, depletion layer components, and fixed mounting or case components. Small-signal low-frequency measurements of

[1]The avalanche capacitance, C_A, is an artificially introduced element to be discussed in Section 2.5.2, and as such it has no effect on the device capacitances under consideration here.

these total capacitances of a 2N3866 transistor as functions of the junction potentials led to the behaviors illustrated in Figs. 2.14 and 2.15.

2.5.1.1 Package Capacitances. The capacitances C_{EB}, C_{CB}, and C_{CE} represent the fixed interelectrode capacities of the transistor package. Their values can be determined directly by opening the device package, disconnecting the internal bonds to the chip, and making low frequency measurements of the remaining package capacitances. A set of package capacitance measurements of a 2N3866 type TO-5 case made with a General Radio 1215A Capacitance Bridge yielded the values

$$C_{EB} = 0.16\ \text{pF}$$

$$C_{CB} = 0.26\ \text{pF}$$

$$C_{CE} = 0.26\ \text{pF}$$

With the interelectrode capacities determined, equivalent case capacities can be subtracted from the total capacitances as indicated in Figs. 2.14 and 2.15. For this subtraction we have defined

$$C_{ECASE} \triangleq C_{EB} + \frac{C_{CE}\,C_{CB}}{C_{CE} + C_{CB}} = 0.29\ \text{pF}$$

$$C_{CCASE} \triangleq C_{CB} + \frac{C_{CE}\,C_{EB}}{C_{CE} + C_{EB}} = 0.27\ \text{pF}$$

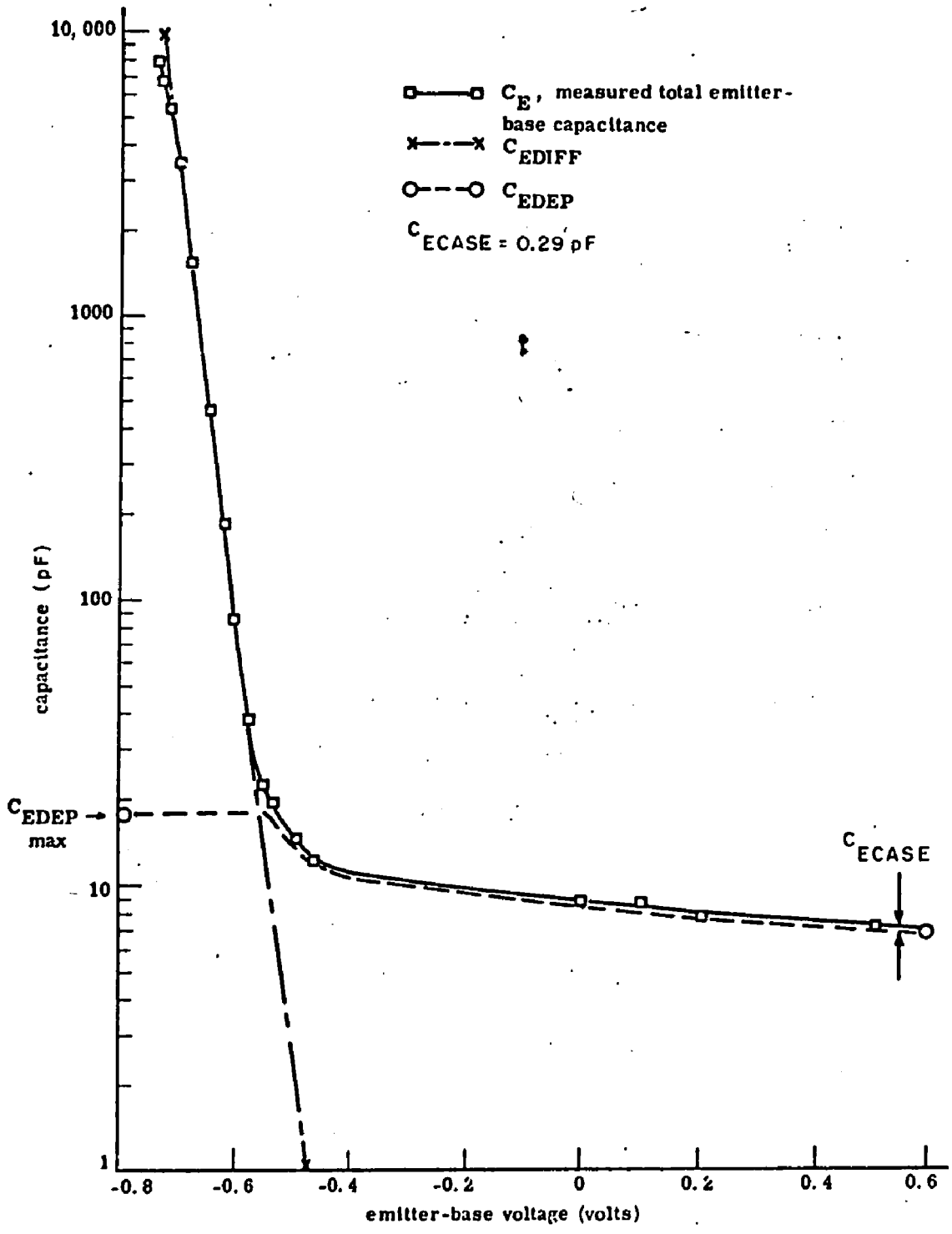


Fig. 2.14. Components of emitter-base capacitance of 2N3866

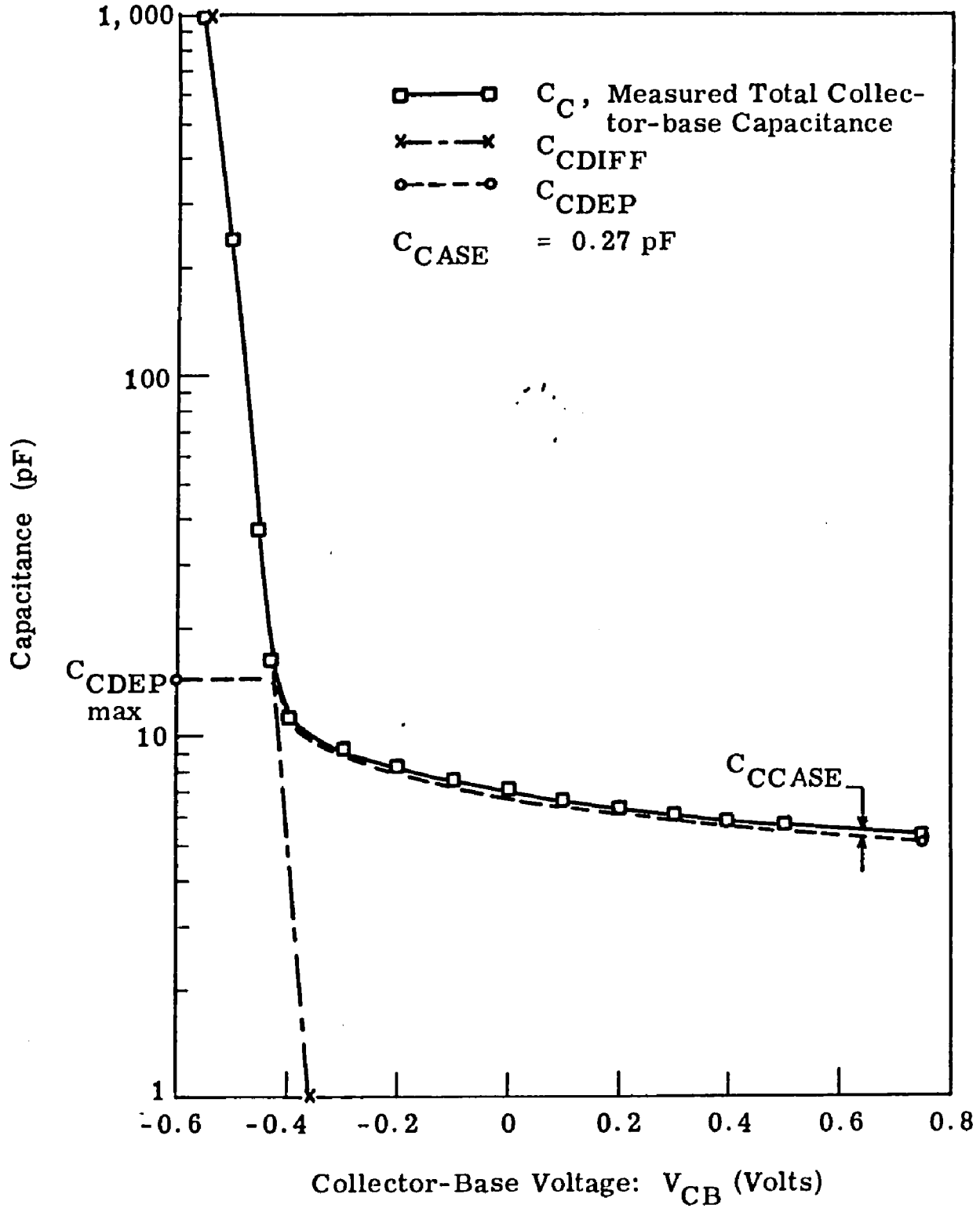


Fig. 2.15. Components of collector-base capacitance of 2N3866

The remaining capacitances in Figs. 2.14 and 2.15 are attributed to the junction diffusion and depletion capacitances.

2.5.1.2 Diffusion and Depletion Capacitances. Analytically the diffusion capacitances have been modeled with exponential voltage dependencies,

$$C_{EDIFF} = \lambda Q_{FS} e^{-\lambda v_{E'B'}} \tag{2.30}$$

$$C_{CDIFF} = \lambda Q_{RS} e^{-\lambda v_{C'B'}} \tag{2.31}$$

and the depletion layer capacitances are usually modeled by fractional power inverse voltage dependencies.

$$C_{EDEP} = \frac{C_{JE}}{(V_{ZE} + v_{E'B'})^{\gamma_E}} + C_{FE} \tag{2.32}$$

$$C_{CDEP} = \frac{C_{JC}}{(V_{ZC} + v_{C'B'})^{\gamma_C}} + C_{FE} \tag{2.33}$$

The parameters of the diffusion capacitances: λ, Q_{FS}, and Q_{RS} (Eqs. 2.30 and 2.31), have been determined in Section 2.3.3.

2.5.1.3 Limiting of Depletion Capacitances. Before establishing the parameter values for the depletion capacitance expressions (Eqs. 2.32 and 2.33) we find that they must be modified slightly to model the behavior under forward bias conditions. Using Eqs. 2.32

and 2.33 directly for transistor simulation would reveal that the depletion layer capacities are modeled very well for reverse and small forward bias conditions, but they are not valid as $v_{E'B'}$ approaches $-V_{ZE}$ or as $v_{C'B'}$ approaches $-V_{ZC}$ in the forward bias regions.

The measurements of C_E and C_C (Figs. 2.14 and 2.15) for both forward and reverse bias show that C_{EDEP} does not become very large as $v_{E'B'}$ approaches $-V_{ZE}$ nor does C_{CDEP} increase without limit as $v_{C'B'}$ approaches $-V_{ZC}$, but on the contrary, the depletion capacitances "limit" at values which are rather low relative to the diffusion capacitances in these regions. Using the semi-logarithmic plots of the junction capacitance data (Figs. 2.14 and 2.15) we can identify linear capacitance components in the forward bias region attributable to the diffusion capacitance terms. These components (and the TO-5 package portion of the total capacitances) can be subtracted leaving the capacitances due to the depletion layers. The maximum values of these components (Figs. 2.14 and 2.15) are used to establish limiting values, A_{ELIM} and A_{CLIM}, for numerical computations involving the arguments, $(V_{ZE} + v_{E'B'})$ and $(V_{ZC} + v_{C'B'})$, in Eqs. 2.32 and 2.33. E.g.,

$$A_{ELIM} = \left(\frac{C_{JE}}{C_{\substack{EDEP \\ max}} - C_{FE}} \right)^{1/\gamma_E} \qquad (2.38)$$

$$A_{CLIM} = \left(\frac{C_{JC}}{C_{\substack{CDEP \\ max}} - C_{FC}} \right)^{1/\gamma_C} \tag{2.39}$$

Adding the "limiting" requirements to the emitter-base and collector-base depletion capacitances has led to the following expressions for computer simulation of the depletion capacitances:

$$C_{EDEP}(v_{E'B'}) = \frac{C_{JE}}{[A_E(v_{E'B'})]^{\gamma_E}} + C_{FE} \tag{2.40}$$

where

$$A_E(v_{E'B'}) \triangleq \text{Supremum} \left\{ \begin{matrix} v_{E'B'} + V_{ZE} \\ A_{ELIM} \end{matrix} \right\}$$

$$C_{CDEP}(v_{C'B'}) = \frac{C_{JC}}{[A_C(v_{C'B'})]^{\gamma_C}} + C_{FC} \tag{2.41}$$

where

$$A_C(v_{C'B'}) \triangleq \text{Supremum} \left\{ \begin{matrix} v_{C'B'} + V_{ZC} \\ A_{CLIM} \end{matrix} \right\}$$

2.5.1.4 Determination of Depletion Capacitance Parameters.

Since the diffusion capacitances rapidly become negligibly small for $v_{E'B'} > -0.4$ volts and $v_{C'B'} > -0.4$ volts; it is natural to measure

the junction capacitances under reverse bias conditions in order to determine the parameters for the depletion layer capacitances. Characterization of the emitter-base and collector-base depletion capacitances are thus provided conveniently by low-frequency junction capacitance measurements under the desired reverse bias conditions. Experimentally measured characteristics of the transition capacitances of three 2N3866 transistors are plotted in Figs. 2.16 and 2.17. The problem that remains is to extract the constants (C_J, V_Z, γ, C_F) from these experimental curves.

If the capacitance relationship is reorganized as

$$C(v) - C_F = \frac{C_J}{(VZ + v)^{\gamma}}$$

and the logarithm is taken

$$\ell n[C(v) - C_F] = -\gamma\, \ell n[VZ + v] + \ell n\, C_J \ ,$$

the result is in slope-intercept form as illustrated in Fig. 2.18a. With the assumptions that VZ is small compared with the largest reverse bias voltage, v, and that C_F is small compared with the largest $C(v)$ measured, a logarithmic plot of experimental $C - v$ data will appear as indicated in Fig. 2.18b. Thus, if a logarithmic plot of the experimental data is made, VZ and C_F values can be determined graphically as those values that shift the experimental data to a straight-line plot on log-log graph paper.

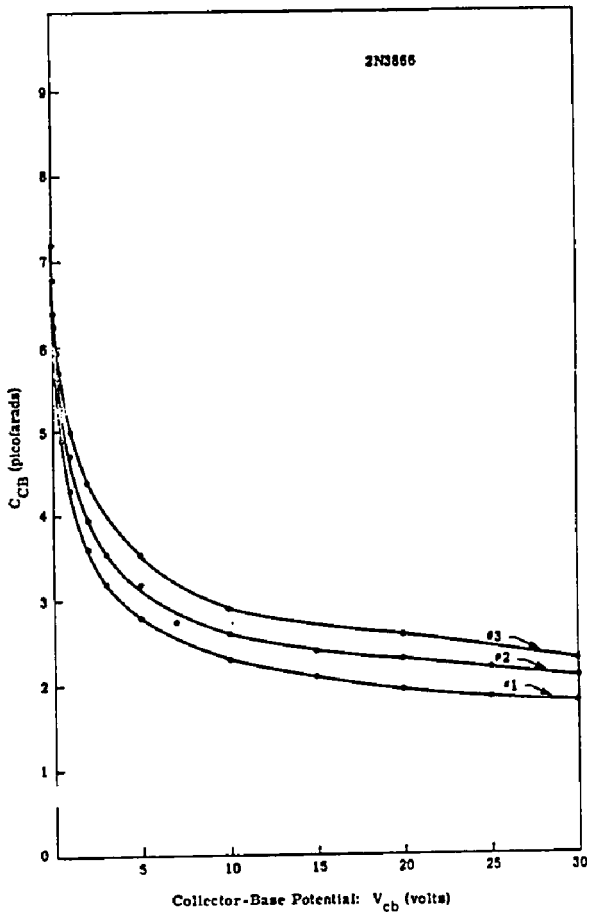


Fig. 2.16. Collector-base depletion and case capacitance

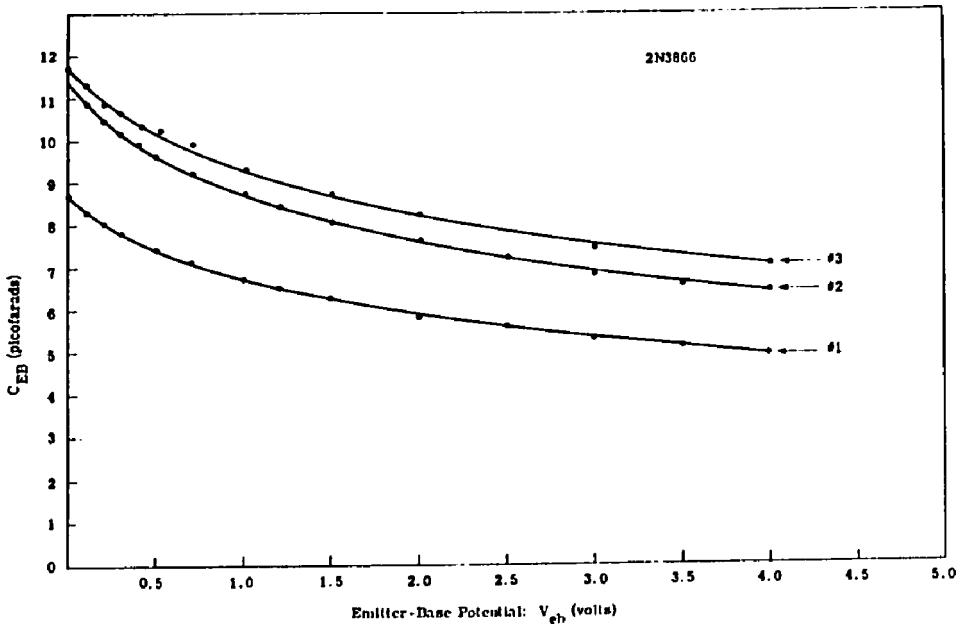
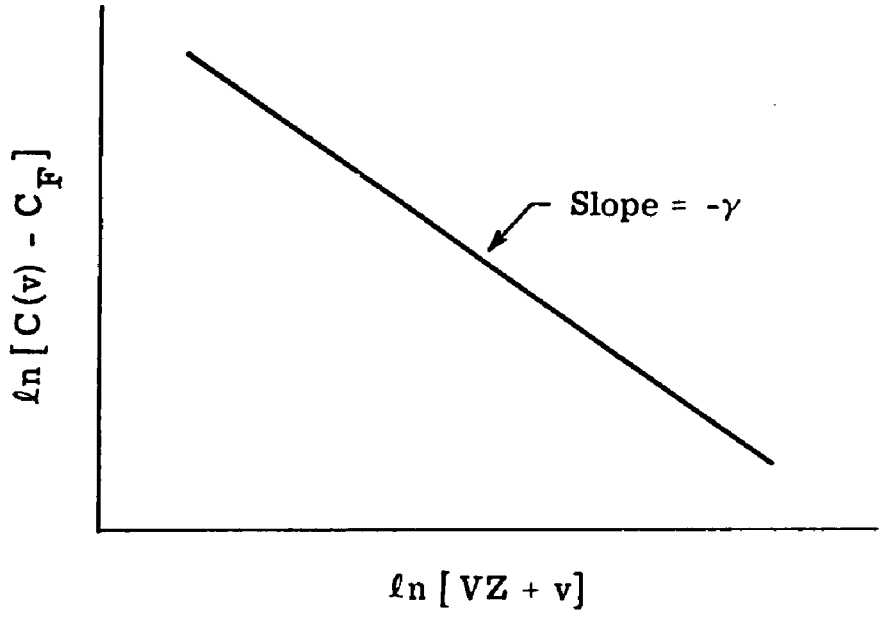
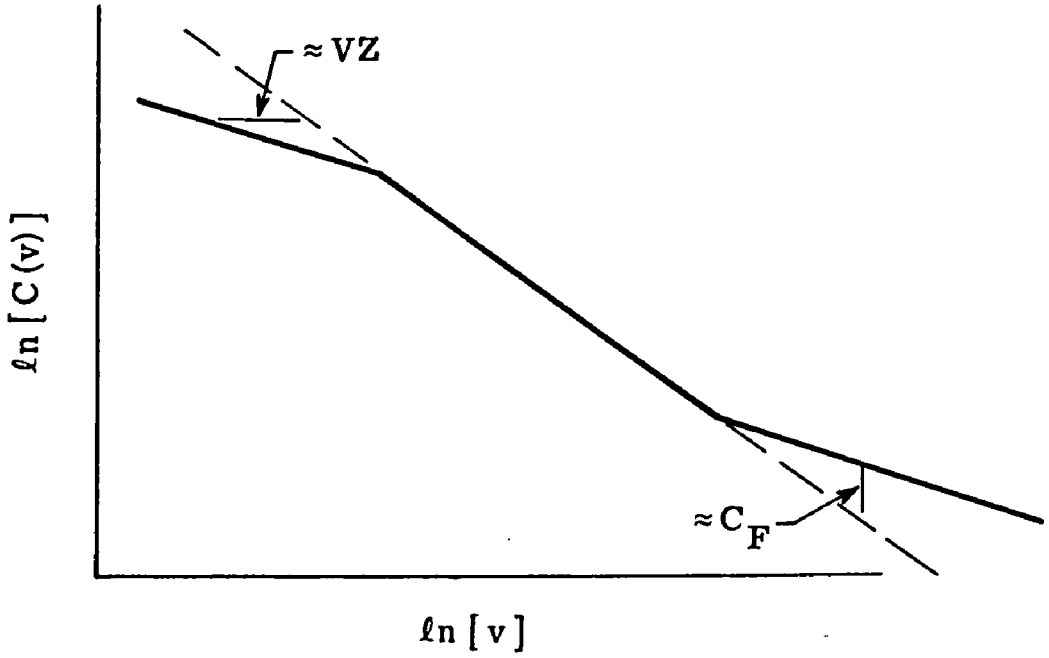


Fig. 2.17. Emitter-base depletion and case capacitance



(a)



(b)

Fig. 2.18. Logarithmic C-v behavior

This graphical procedure is illustrated in Fig. 2.19 where the experimental collector-base capacitance data were first shifted to the right by an amount VZC = 0.5, and then shifted downward by an amount $C_{FC} = 1.7$ pF. The resulting plot is a straight line whose slope gives a value of $\gamma_C = 0.474$. The value of C_{JC} is read from the final straight-line plot as the value of C_{CDEP} when v_{CB} is 1.0 volt, and, in this example, $C_{JC} = 3.41$ pF. Returning to Fig. 2.15 we find

$$C_{CDEP_{max}} = 14.5 \text{ pF}$$

and from Eq. 2.39 we determine the limiting argument for the collector-base junction to be

$$A_{CLIM} = 0.0625$$

Summarizing the results for the collector-base depletion capacitance, we have

$$C_{JC} = 3.41 \text{ pF}$$

$$C_{FC} = 1.7 \text{ pF}$$

$$\gamma_C = 0.474$$

$$V_{ZC} = 0.5 \text{ volt}$$

$$A_{CLIM} = 0.0625 \text{ volt}$$

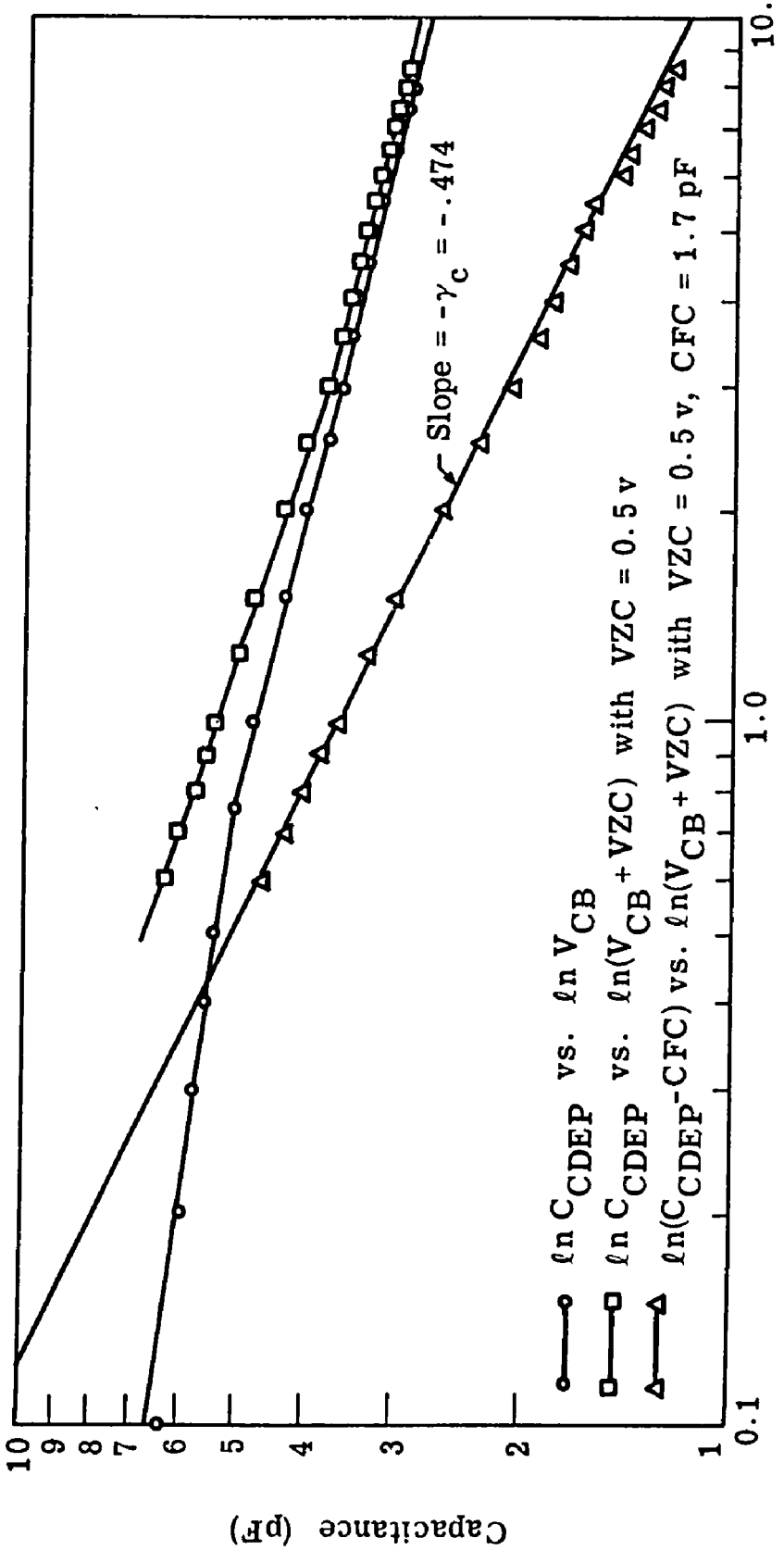


Fig. 2.19. Graphical determination of collector depletion capacitance parameters

Repeating this graphical procedure for determining the emitter-base transition capacitance parameters yields

$$C_{JE} = 10.4 \text{ pF}$$

$$C_{FE} = 0.1 \text{ pF}$$

$$\gamma_E = 0.314$$

$$V_{ZE} = 0.8 \text{ volt}$$

$$A_{ELIM} = 0.06 \text{ volt}$$

2.5.2 Emitter-Base Avalanche Description. The controlled avalanche breakdown source and the associated avalanche capacitance are additions to the intrinsic portion of the usual transistor model. Their inclusion in the model has been prompted by measurements of an experimental class-C amplifier. It was observed that under conditions of static reverse bias emitter-base potential and large signal excitation, the average base current can be in a direction opposite to the normal direction for forward bias. An explanation for this reversal of the average base current direction at large signal excitation amplitudes is the occurrence of avalanche breakdown of the emitter-base junction whenever the total emitter-base potential exceeds the transistor's emitter-base breakdown voltage. The additions of the avalanche current source, i_A, and an avalanche capacitance, C_A, were made to the intrinsic model to account for these avalanche effects. It has been assumed that the majority carriers injected into the base region during

avalanche conduction recombine sufficiently fast so that their associated storage effects may be neglected. This assumption has been supported by small signal measurements of avalanching junctions. Measured emitter-base impedances in the avalanche region were found to be slightly inductive with Q's of less than unity for frequencies up to 100 MHz. In addition, it is assumed that avalanche carriers injected into the base are not coupled to the collector, i.e., the collector-base junction will be assumed to be reverse biased when the emitter-base junction is avalanching. Thus the majority carriers (holes) injected into the base region by emitter-base avalanche will be repelled by the electric field at the reverse biased collector-base junction.

The voltage dependent forms for these avalanche elements are chosen to be

$$i_A = \frac{Q_{FS}}{\alpha_F \tau_F}\left[\frac{1}{1 - (v_{E'B'}/VA)^{N_A}} - 1\right] \tag{2.42}$$

$$C_A = \frac{K_A \tau_F i_A}{V_A - v_{E'B'}} \tag{2.43}$$

The form of Eq. 2.42 is often used to describe the behavior of avalanching junctions (Ref. P3). The capacitance C_A does not model an experimentally observed effect; it was introduced artificially to overcome excessive integration times in the numerical simulation program. The capacitance C_A is given a voltage dependency to make the time

constant of the avalanching junction large enough to avoid numerical difficulties (excessive computation times) without changing the computed results.

Experimental observation of several 2N3866 transistors has indicated unit-to-unit variations and departures from the analytical form of Eq. 2.42 for small avalanche currents (less than 1 mA). For larger currents, however, the characteristics of all the devices are well modeled by Eq. 2.42. The only significant variation from unit to unit is the value of the avalanche voltage, V_A. This value is easily established from static measurements in the avalanche region; a typical value for a 2N3866 is 6.2 volts.

Computer analyses of a class C amplifier, using the extended model for a 2N3866 transistor, showed the amplifier behavior to be relatively insensitive to the value chosen for the exponent N_A. Values of N_A from 2.0 to 6.0 have no perceptible effect on the computation times or the computed results, and a value of $N_A = 4.0$ was chosen as the representative value for a 2N3866.

Several values of the avalanche capacitance weighting constant, K_A, were tried in numerical analyses of the class C amplifier. K_A controls the time constant of the emitter-base junction during avalanche. If this time constant during avalanche, τ_A, is allowed to become much less than the recombination time constant for emitter-base minority carriers, τ_F, computation times for the numerical integration become excessive. It has been found that constraining the avalanche time

constant such that $\tau_F \leq \tau_A \leq 2\tau_F$ will prevent the integration difficulties associated with widely separated time constants; at the same time τ_A will be small enough that the computed results will be unaffected. As τ_A is increased toward $2\tau_F$, the computation time approaches a limiting minimum. Hence τ_A values greater than $2\tau_F$ were not tried as these larger time constants are not expected to reduce computation times, and such large artificial time constants would reduce the accuracy of the simulation. In conclusion, as long as the avalanche time constant does not alter the dynamic behavior of the amplifier, its value can be increased to avoid the numerical difficulties associated with very small nondominant time constants (Refs. G1, C2, C3, R3).

The values chosen for the bulk of the computer simulations of the emitter-base avalanche behavior are summarized below.

$$V_A = 6.2 \text{ volts}$$

$$N_A = 4.0$$

$$K_A = 1.0$$

2.5.3 Extrinsic Resistances.

2.5.3.1 Initial Estimates of R_{BB}. The extrinsic resistances R_{BB}, R_{CC}, and R_{EE} (Fig. 2.13) were added to the intrinsic transistor model (Fig. 2.12) to approximate the resistive potential drops in the bulk semiconductor regions of the transistor. Values for

the base spreading resistance, R_{BB}, can be estimated from small signal y_{ie} data and collector-base time constant data. A standard technique for estimating the value of the extrinsic base resistance is to measure the transistor input admittance y_{ie} at high frequencies (Ref. E2, p. 118). Then

$$R_{BB} = \left. \frac{1}{Re[y_{ie}]} \right|_{f_M}$$

where f_M is the frequency at which $Im[y_{ie}] = 0$.

From published technical data for a typical 2N3866 (Ref. S1) we find

$$R_{BB} = \left. \frac{1}{Re[y_{ie}]} \right|_{\substack{f = 250 \text{ MHz} \\ V_{ce} = 15 \text{ volts} \\ I_{COL} = 80 \text{ mA}}} \approx 20.0\ \Omega$$

The same reference source for the 2N3866 gives a typical high frequency figure of merit, $R_{BB}\, C_{CBO}$, as

$$R_{BB}\, C_{CBO} \Big|_{\substack{V_{ce} = 10 \text{ volts} \\ I_{COL} = 20 \text{ mA}}} = 8.0 \text{ pico second}$$

with

$$C_{CBO} \Big|_{V_{CB} = 10 \text{ volts}} = 2.0 \text{ picofarad}$$

This data implies

$$R_{BB} = 4.0\ \Omega$$

The wide disparity between these two values of R_{BB} (20.0 and 4.0 Ω) prompts additional measurements to establish a satisfactory value for the large signal model. Such measurements are considered in Sections 2.5.3.3 through 2.5.3.7.

2.5.3.2 Initial Estimates of R_{CC} and R_{EE}. In the pulsed, charge storage measurements to determine τ_F and τ_R (Section 2.3.2), abrupt changes in stored base charge were observed for large collector and emitter currents. This break in the stored charge characteristics was attributed to saturation of the intrinsic semiconductor junction. This saturation effect was found to be voltage dependent and was caused by potential drops in the extrinsic collector and emitter resistances. From the charge storage measurements the bulk resistances may be estimated as

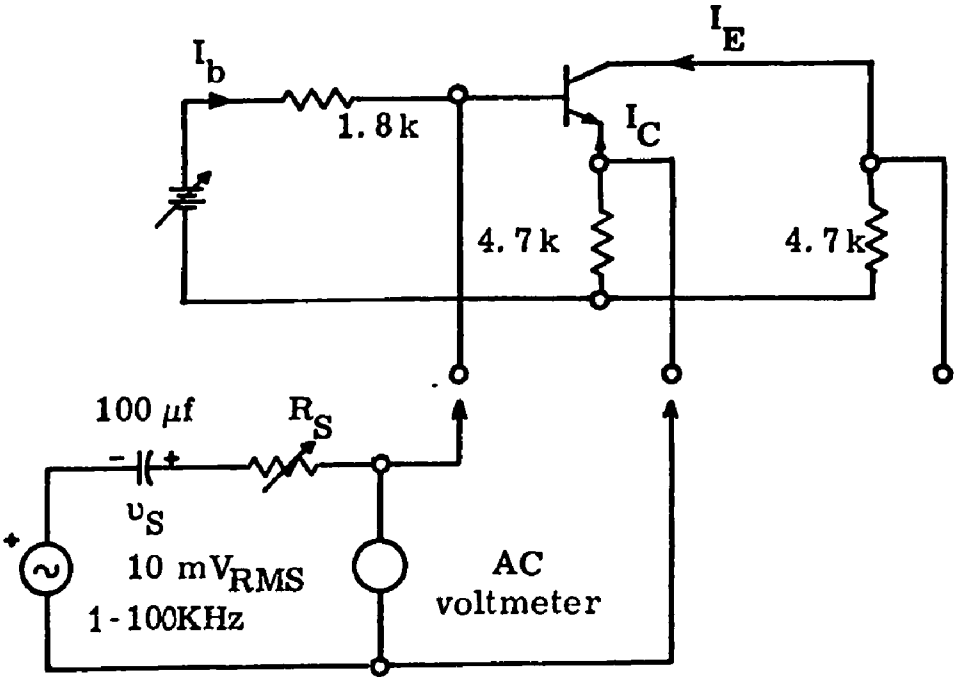
$$R_{CC} \approx 50.0\ \Omega$$

$$R_{EE} < 1.4\ \Omega$$

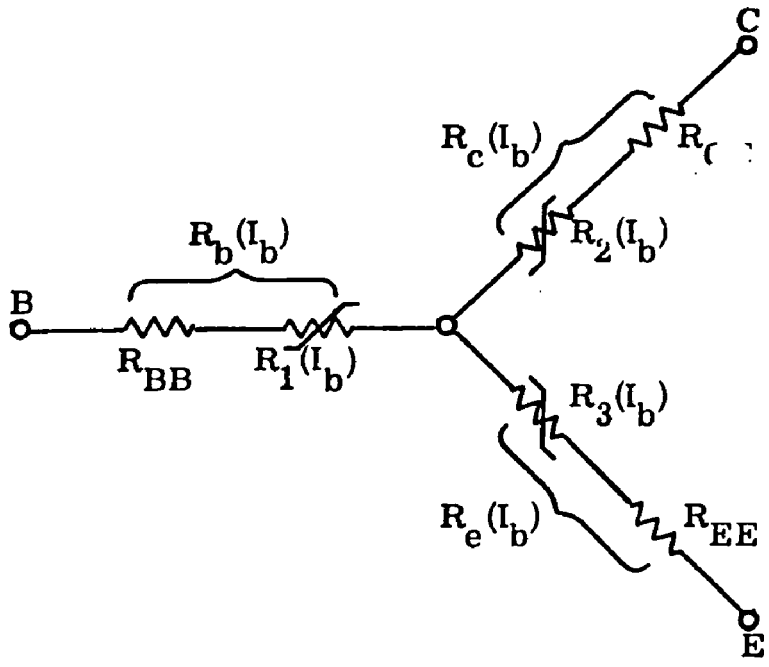
An additional guide to the value of R_{CC} was provided by observed waveforms of a 100 MHz amplifier (Section 5.2) and preliminary simulations of the amplifier (Section 5.3). These simulations indicated that approximately 10.0 Ω of extrinsic collector resistance

would be required to bring the experimental and computed collector voltage waveforms into agreement.

2.5.3.3 Saturated Resistance Measurements. In order to resolve the values of R_{BB}, R_{CC}, and R_{EE} further independent measurement techniques were considered. To the extent that the bulk resistances of the emitter, base and collector regions can be modeled adequately as single-lumped resistances, it should be feasible to isolate these resistance effects with low frequency measurements. By biasing the transistor in the saturation region as indicated in Fig. 2.20a, and considering the small signal behavior to be represented by a Y connection of resistors as in Fig. 2.20b, the bulk resistances R_{BB}, R_{CC}, and R_{EE} can be determined by measurements of terminal resistances at various levels of bias current. The results of this procedure for measurement frequencies of 1 kHz to 100 kHz are shown in Fig. 2.21. As expected the total branch resistances are found to vary inversely with current for small currents. At the higher current levels, the bulk resistances are expected to dominate the total branch resistances and thus can be separated from the total resistances. Values of $R_{BB} < 1.0\Omega$, $R_{CC} \leq 0.4\Omega$ and $R_{EE} \leq 0.55\Omega$ can be inferred from Fig. 2.21. These values are much smaller than expected on the basis of previous information. These low frequency measurements do not seem to be representative of the values that should be used to characterize the transistor at higher frequencies.



(a)



(b)

Fig. 2.20. (a) Measurement circuit - low frequency saturated resistance
(b) Y connection representation of saturated transistor small signal behavior

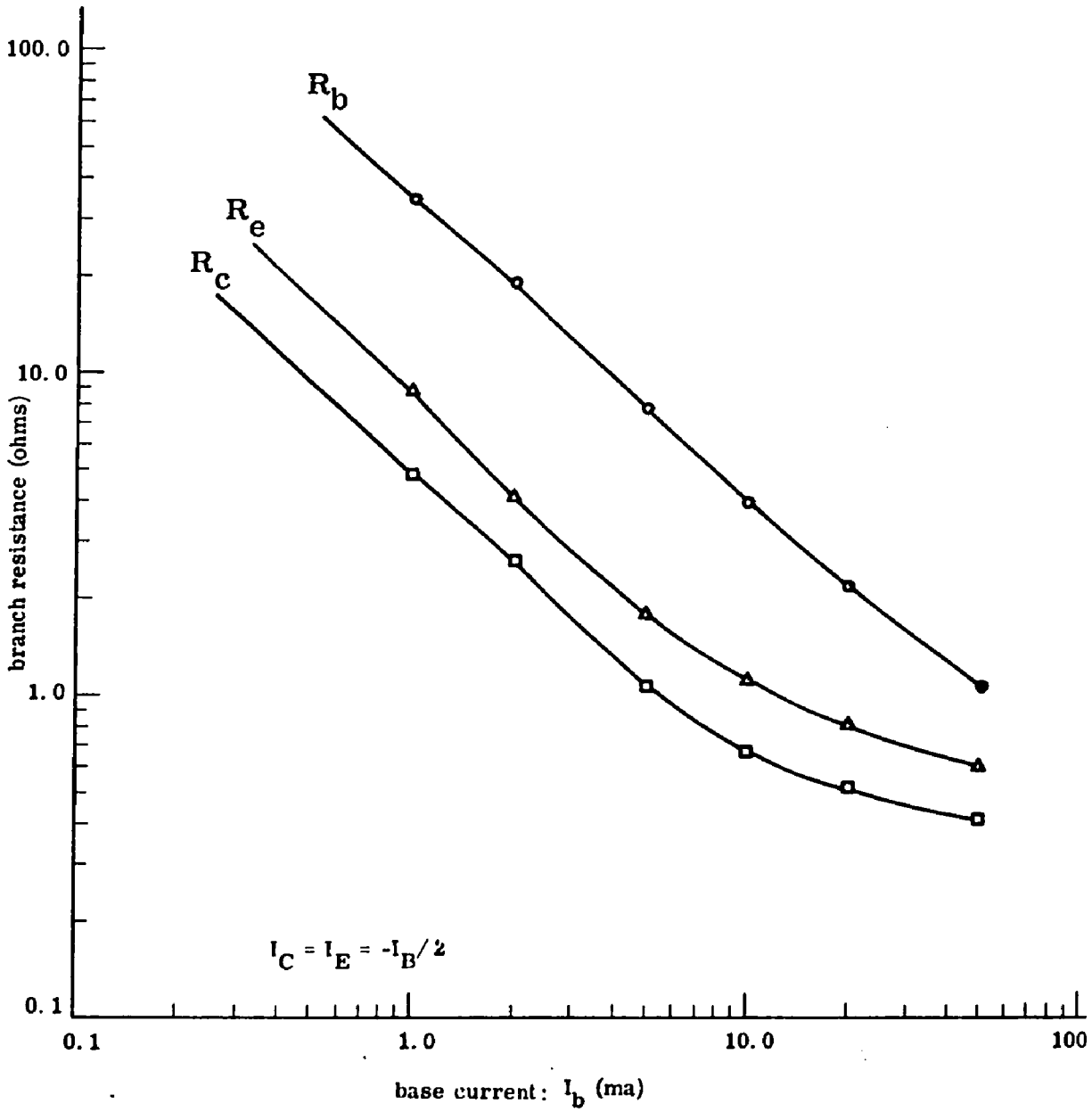


Fig. 2.21. Low frequency saturated resistance measurements

One possible reason for the surprising difference between resistance values measured at low frequencies and those inferred from the small-signal high-frequency data, charge storage results, and amplifier measurements might be that these resistance values are frequency dependent at the higher frequencies. For this reason an equivalent set of saturated resistance measurements were made in the VHF frequency band. For these measurements the transistor junctions were again forward biased, and the small signal terminal impedances were measured with a General Radio 1607A Transfer Function and Immittance Bridge (Fig. 2.22). The terminal impedances were separated into three equivalent Y-connected impedances Z_{BB}, Z_{CC}, and Z_{EE}. The real components of these impedances, for a 100 MHz measurement frequency, are plotted in Fig. 2.23. From these plots we might estimate saturated bulk resistance values of $R_{BB} = .42\,\Omega$, $R_{CC} = .24\,\Omega$, and $R_{EE} = .35\,\Omega$. These values are of the same order as those determined at low frequencies (Fig. 2.21) and again are too small to correctly predict the observed behavior of the VHF power amplifier as mentioned in Section 2.5.3.2.

2.5.3.4 Experimental Observation of Saturation Characteristics. The differences among the resistance values obtained by the preceding measurements (summarized in Table 2.1) led to supplementary investigations of the characteristics of the 2N3866 transistor operating as a high speed saturated switch. The nature of the turn-on

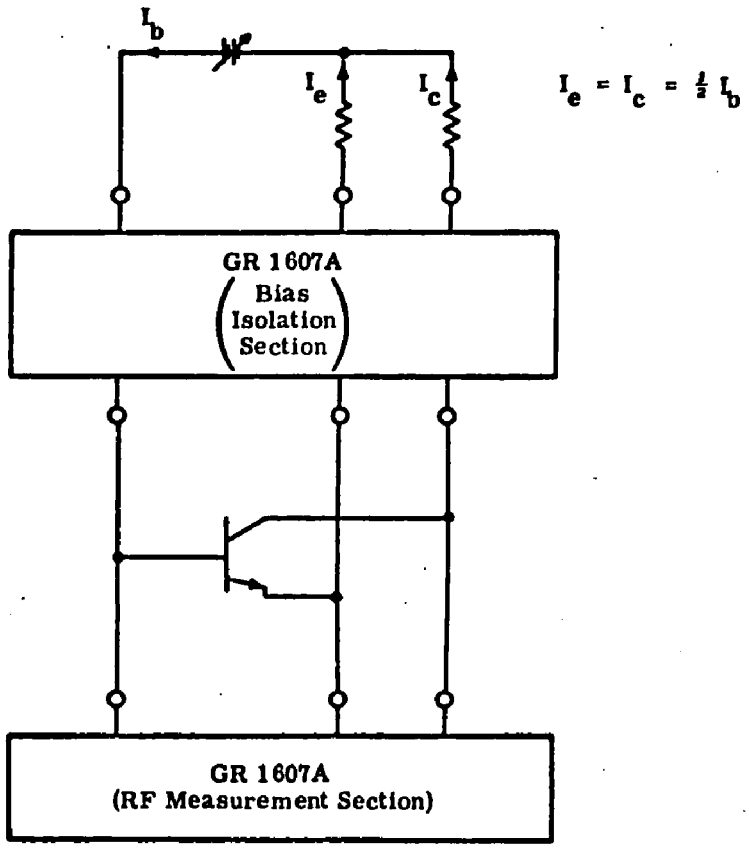


Fig. 2.22. Measurement circuit for VHF saturated impedances

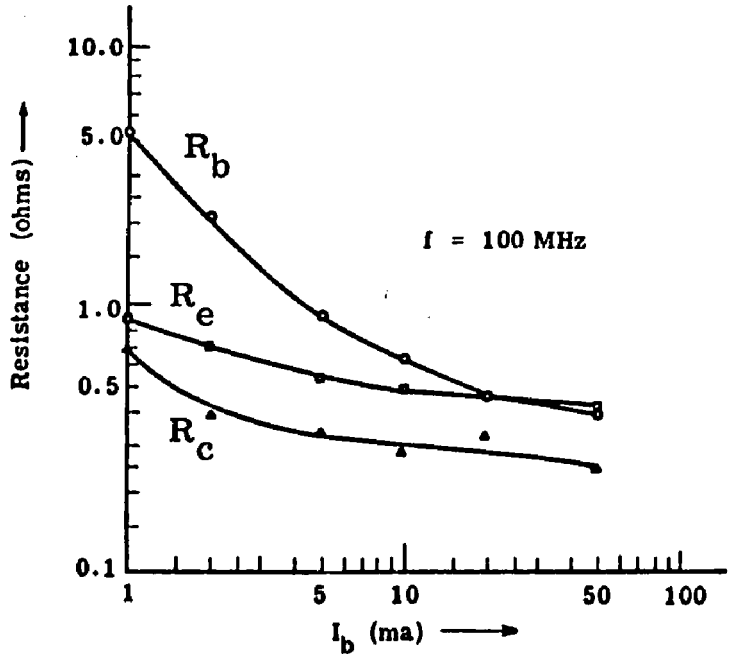


Fig. 2.23. Real parts of VHF saturated impedances

Description of Measurement	Element Values Determined
y_{ie} Data	$R_{BB} \approx 20.0\Omega$
Collector-Base Time Constant	$R_{BB} \approx 4.0\Omega$
Pulsed Charge Storage Measurement	$R_{CC} \approx 50.0\ \Omega$ $R_{EE} < 1.4\Omega$
100 MHz Class C Amplifier Waveforms	$R_{CC} \approx 10.0\Omega$
Low-Frequency Saturated Resistances	$R_{BB} < 1.0$, $R_{CC} \leq 0.4$, $R_{EE} \leq 0.55$
High-Frequency Saturated Impedances	$R_{BB} \approx 0.42$, $R_{CC} \approx 0.24$, $R_{EE} \approx 0.35$

Table 2.1. Summary of extrinsic resistance estimates

characteristics of several transistors was observed by utilizing the test circuit of Fig. 2.24. The saturation characteristics of several 2N3866 transistors all displayed a definite break in turn-on time constant as the device entered the edge of saturation (Fig. 2.25). The collector voltage at which the break in turn-on time constant occurred was found to vary rather linearly with changes in supply voltage, V_{CC}, indicating that the phenomena can be explained by a linear (resistive) effect. Thus the saturation characteristics may be used to establish

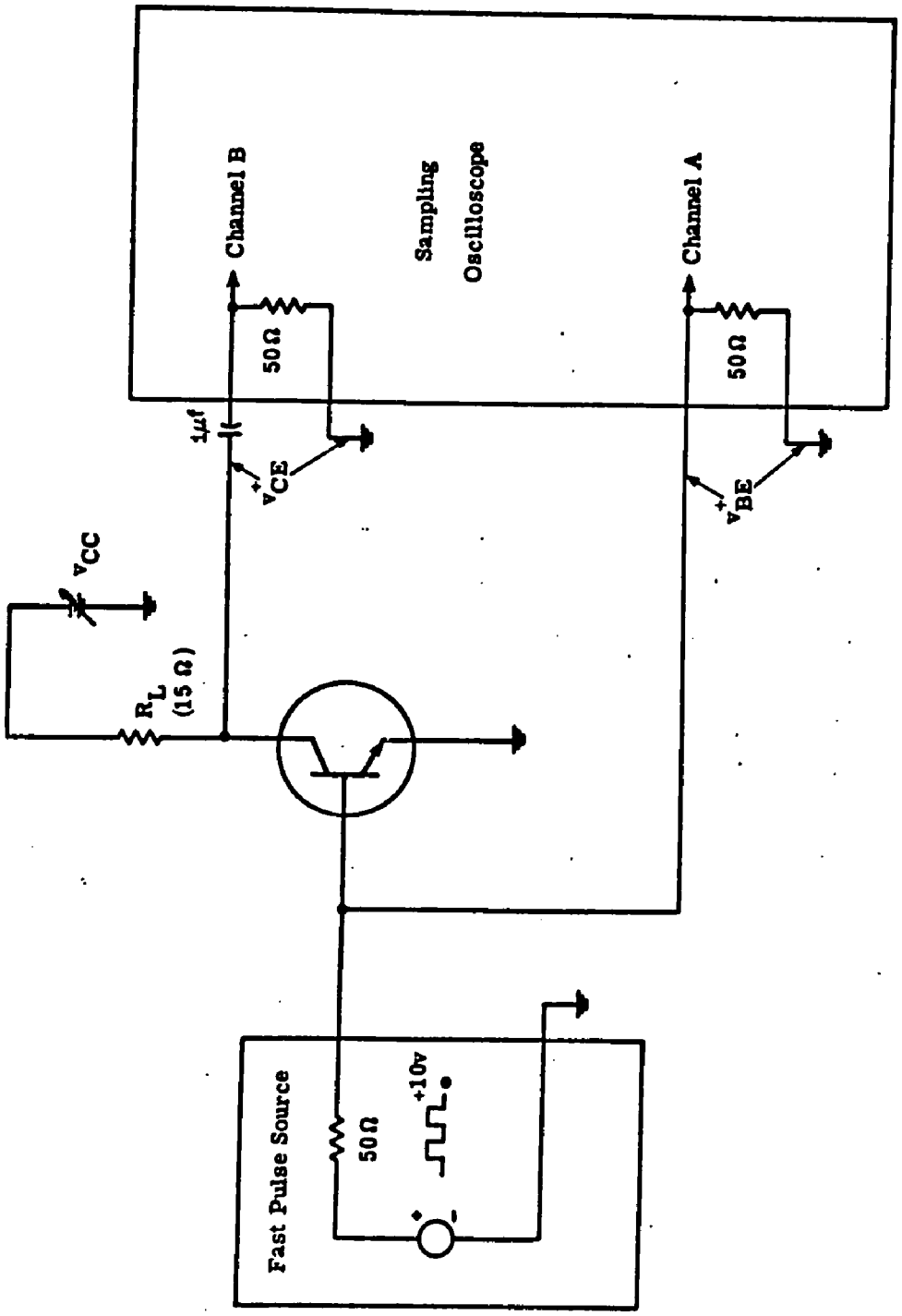


Fig. 2.24. Switching test circuit

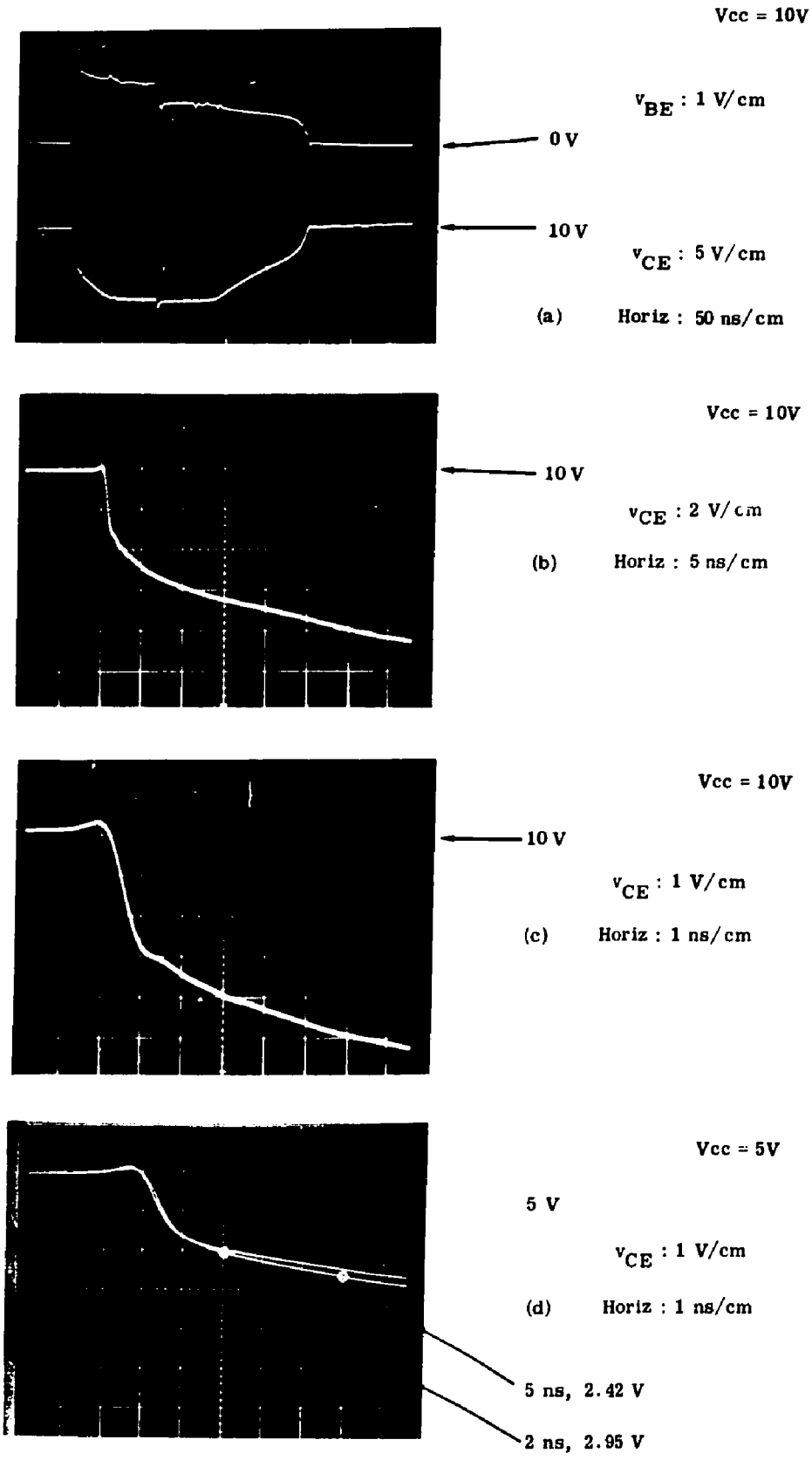


Fig. 2.25. Turn-on characteristics of 2N3866

effective resistance values, but these values should be dependent on the length of time the device is expected to be in saturation. For example, for a 100 MHz amplifier, the transistor switching duty factor can be expected to be about 40 percent or less; therefore, the transistor may be in saturation for approximately 4 nanoseconds. An average saturation resistance can be estimated from the results of the switching test using an average saturation voltage observed during the first 4 nanoseconds. For the transistor used in the RF power amplifiers discussed in Chapters 5 and 6

$$R_{sat} = \frac{V_{ce\ avg}}{V_{cc} - V_{ce\ avg}} \cdot R_L' = 13.27 \text{ ohms} \qquad (2.44)$$

where $V_{ce\ avg} = \frac{1}{2}(2.42V + 2.95V)$ From Fig. 2.25d

$R_L' = \frac{(15\,\Omega)(50\,\Omega)}{(15\,\Omega) + (50\,\Omega)}$ From Fig. 2.24

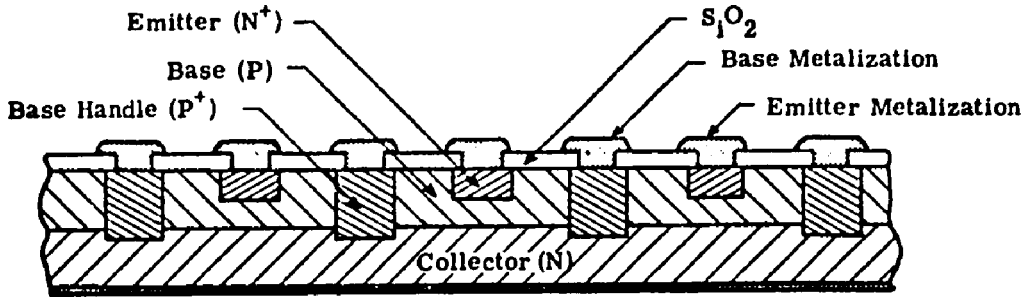
This saturation resistance is much larger than suggested by the saturated resistance values of Section 2.5.3.3. A discussion of the transient behavior of the 2N3866 transistor is given in the next section to resolve these differences in saturation resistance.

2.5.3.5 Effective Resistances Under Transient Conditions. The 2N3866 is an NPN planar overlay type transistor with 16 separate emitter sites. An illustrative cross sectional view of a portion of such a transistor structure is shown in Fig. 2.26a. For our purposes we may consider that the behavior of charge distribution is identical under each of the separate emitters, and we can concentrate on the characteristics of one such region remembering that the current flow through the total

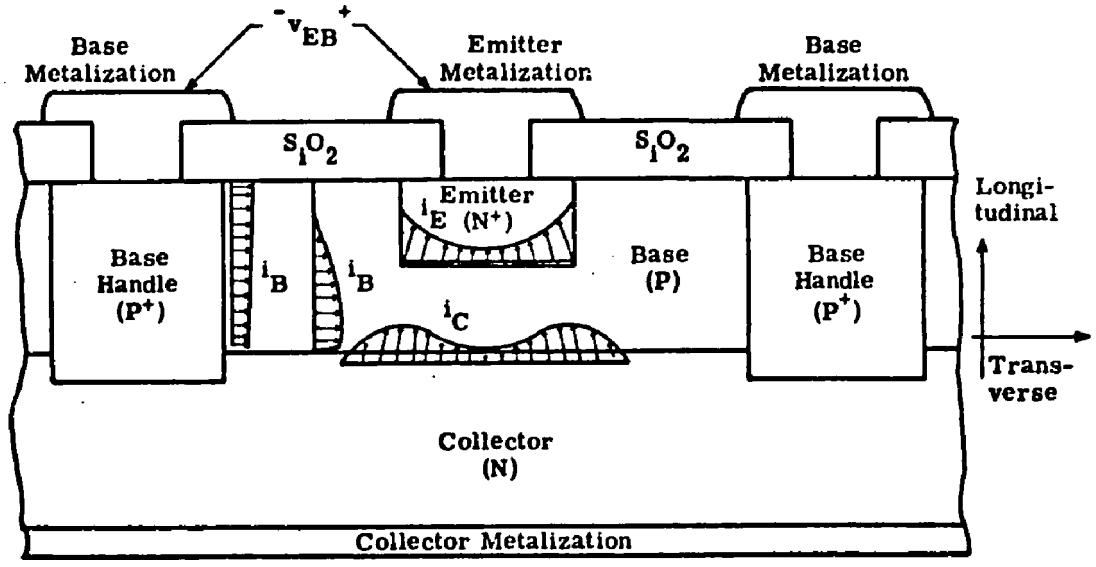
device will include a summed effect of the sixteen separate emitters.

The current distribution beneath any one emitter site is adumbrated in Fig. 2.26b. There are several reasons for the non-uniformity of the current distribution in the various regions of the transistor. The principal reasons for this non-uniform current flow are (a) current crowding at the periphery of the emitter-base junction due to the transverse ohmic potential drop along the emitter-base junction which results from large transverse flow of carriers in the base region under large signal conditions, and (b) the transverse potential drop due to the distributed R-C structure of the base region resistance and the emitter-base diffusion capacitance (Ref. C6, pp. 23-38). It is this second effect of requiring majority carrier motion in the base region to charge the diffusion capacitance (stored charge) that develops a non-uniform emitter-base bias whenever the emitter-base potential is required to change in a dynamic sense. As a result of this dynamic effect, the edges of the emitter-base junction provide the majority of the longitudinal carrier motion. As a net result it appears as though only a small portion of the total active transistor area is responsible for handling the majority of the current during transient conditions.

If we were to think of one emitter-base-collector portion of the transistor as a distributed structure, and then model this distributed structure as several discrete lumps, we would be led to an equivalent transistor model as illustrated in Fig. 2.27. This structure excludes any effects attributable to the package capacitances, inductances and



(a)



(b)

Fig. 2.26. (a) Cross sectional view of overlay transistor structure
(b) Expanded view of overlay transistor

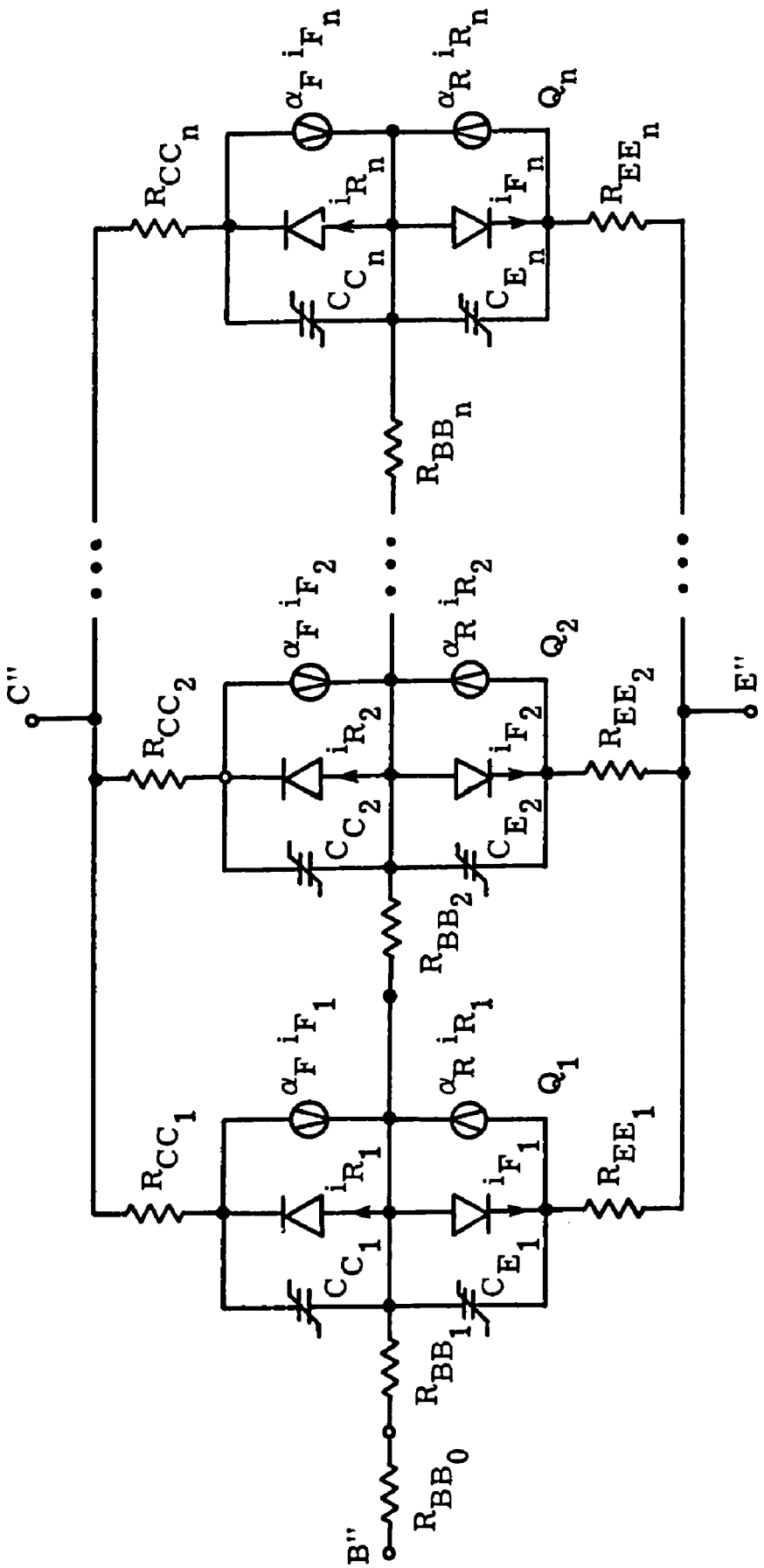


Fig. 2.27. Lumped equivalent transistor model

contact resistances. The initial part of the base resistance, R_{BB_0}, is a representation of the inactive portion of the base, that is, the portion not beneath the emitter and not participating in the useful transistor action. This resistance is normally small (10-50 ohms) for high frequency transistors and is subject to drastic reduction (100:1 ratio) due to conductivity modulation under conditions of high carrier concentrations associated with large static current levels. The lumped equivalent resistances of the distributed active portion of the base region, R_{BB_1}, R_{BB_2}, ... R_{BB_n}, also become reduced by conductivity modulation at high current levels and in addition can be expected to increase slightly at large reverse bias collector-base potentials due to base width modulation. The equivalent collector resistances and the equivalent emitter resistances are also current dependent due to conductivity modulation, but the emitter resistances are much smaller than those of the collector because of the relatively high emitter doping concentrations. For our present purposes, each section of the multi-lumped equivalent may be assumed to be identical.

If we now take our multi-lumped equivalent model for one emitter-base-collector region and reduce its impedance levels by sixteen, we can account for the total current through the sixteen emitter sites of the 2N3866 overlay transistor. In order to use this structure in a practical package, small values of contact resistance, lead inductance, and case capacitance are inevitable. A total representation of

a 2N3866 type device is finally depicted in Fig. 2.28. (Approximate values have been given by each element to indicate their relative magnitudes only and should not be construed as precise descriptions of the device.) This representation will form the basis for explaining the differences obtained in the saturated and transient measurements of the equivalent terminal resistances.

With conditions of static bias the multi-lumped transistor model behaves similarly to the single lump nonlinear model we have been using previously. However, if the multi-lumped model is operated in dynamic situations such as presented by the switching test circuit of Fig. 2.24, the effects of the individual lumps become more apparent. Consider operating the multi-lump model in the switching test circuit as the base drive conditions control the device from cut-off, through the active region, and then into saturation. As the device is brought into the active region a transverse potential drop occurs across resistors R_{BB_1}, R_{BB_2} ... R_{BB_n} because of the base current flow through them. Because of this transverse potential, the first lump of the model, Q1, is more heavily forward biased than succeeding lumps and thus is responsible for providing a disproportionate share of the total collector current. As the total collector current increases with a time constant τ_F, the collector potential is reduced at this same rate until the collector-base junction of the first section is brought into saturation. At this point the base charge time constant of this first section changes from approximately τ_F to

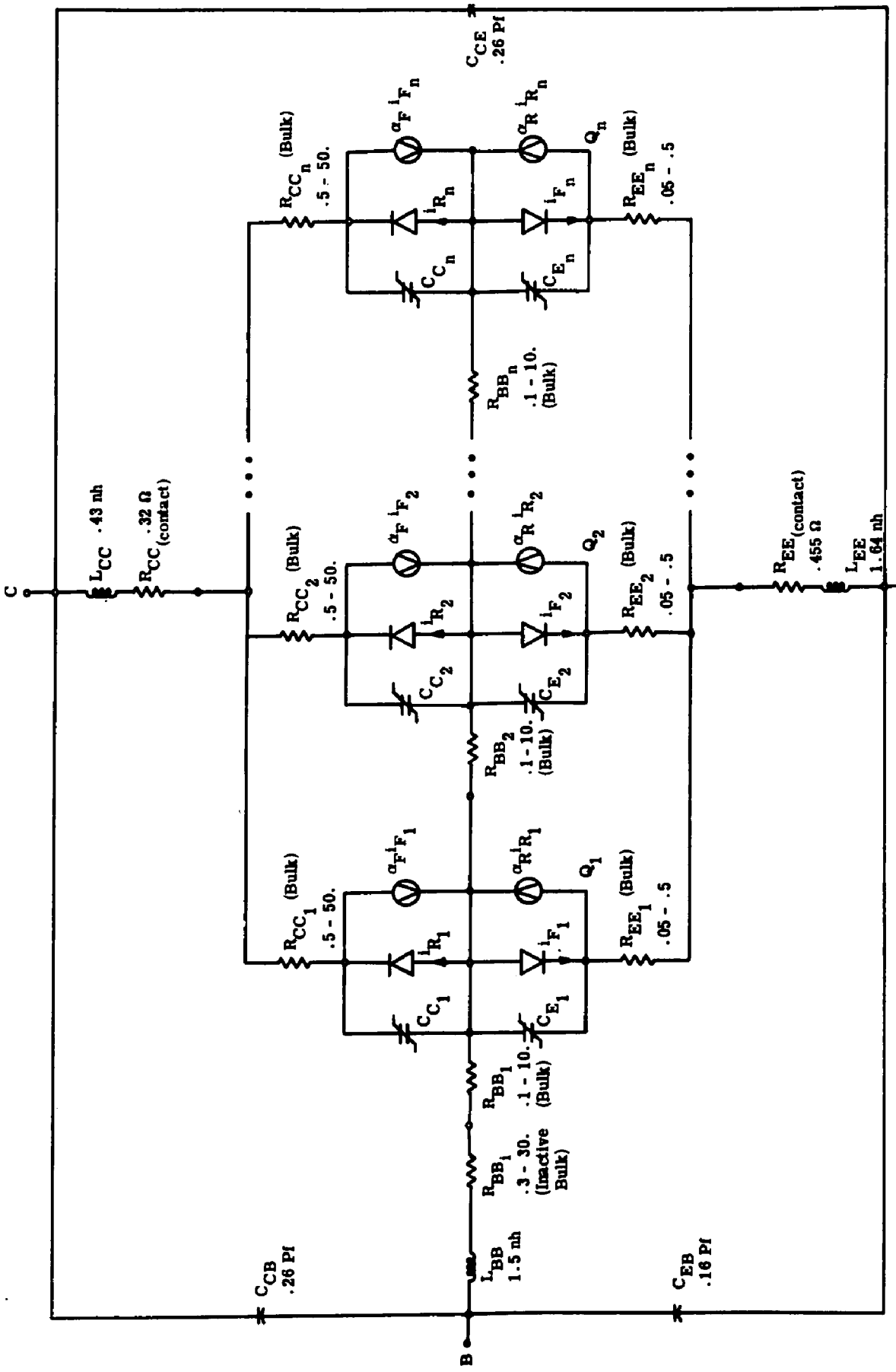


Fig. 2.28. Total 2N3866 representation

$$\tau_S \approx \frac{\alpha_F(\tau_F + \alpha_R \tau_R)}{1 - \alpha_F \alpha_R}$$

In effect, further increases in base potential for this first section must then be accompanied by large increases in charge stored in its collector-base diffusion capacitance in addition to the charges stored in the emitter-base diffusion capacitance. Hence, the rate at which the base transverse carrier flow can spread to the inner lumps is retarded by saturation of the first lump. For the model chosen, this change in time constant would occur at an approximate collector potential of

$$V_{\substack{ce \\ sat\ first\ lump}} \approx V_{CC} \cdot \frac{R_{CC_1} + R_{EE_1}}{R_L + R_{CC_1} + R_{EE_1}}$$

As the supplied base charge spreads from the outermost lump to the innermost or last lump of the model, additional sections reach saturation, reducing even more the rate at which remaining lumps can reach saturation.

As viewed from the device terminals this spread of saturation from the periphery to the inner portion of the active transistor would appear as a continual monotonic reduction in collector saturation resistance from the time the first portion of the transistor reaches saturation until the entire device has obtained a steady state saturation condition. It seems reasonable that it is this distributed saturation

phenomena that has led many designers of high frequency class C amplifiers to state that saturation voltage for RF transistors increases with frequency (Refs. L2, T1).

2.5.3.6 Validation of Multi-Lump Model Transient Behavior. Measurements of the turn-on characteristics of several other types of transistors were performed with the same test circuit as used for the 2N3866 (Fig. 2.24). For the devices observed, overlay and non-overlay planar types, not all displayed a pronounced time constant change at these current levels, and it is not clear as to what geometries and construction techniques will produce devices with the pronounced change in time constant as saturation is approached. In particular, a type 2N918 transistor did not exhibit a double time constant in its turn on characteristics (Fig. 2.29), and this type device was chosen to generate an artificial break in time constant by constructing a two-lump equivalent circuit (Fig. 2.30). This equivalent circuit was used to demonstrate the ability of the chosen lumped model form to predict a double time constant turn-on characteristic similar to that observed for the 2N3866 (Fig. 2.25). The results of the test with the equivalent two-lump transistor formed from two 2N918's are shown in Fig. 2.31, and as can be seen, a clear break in time constant was produced by the circuit.

Returning to the multi-lump representation for the 2N3866 (Fig. 2.28) we can consider the effects of applying a static forward bias to

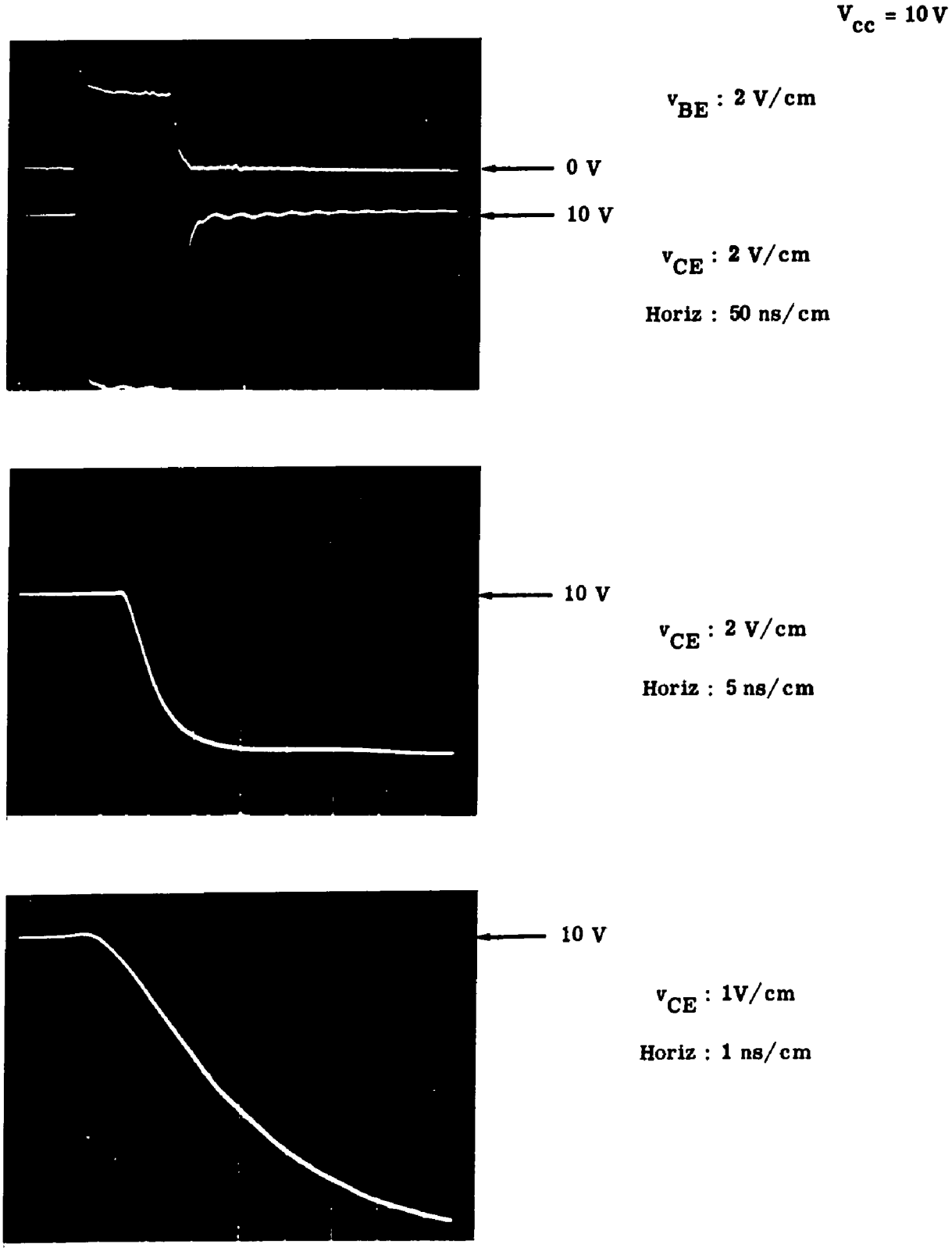


Fig. 2.29. Turn-on characteristics of 2N918

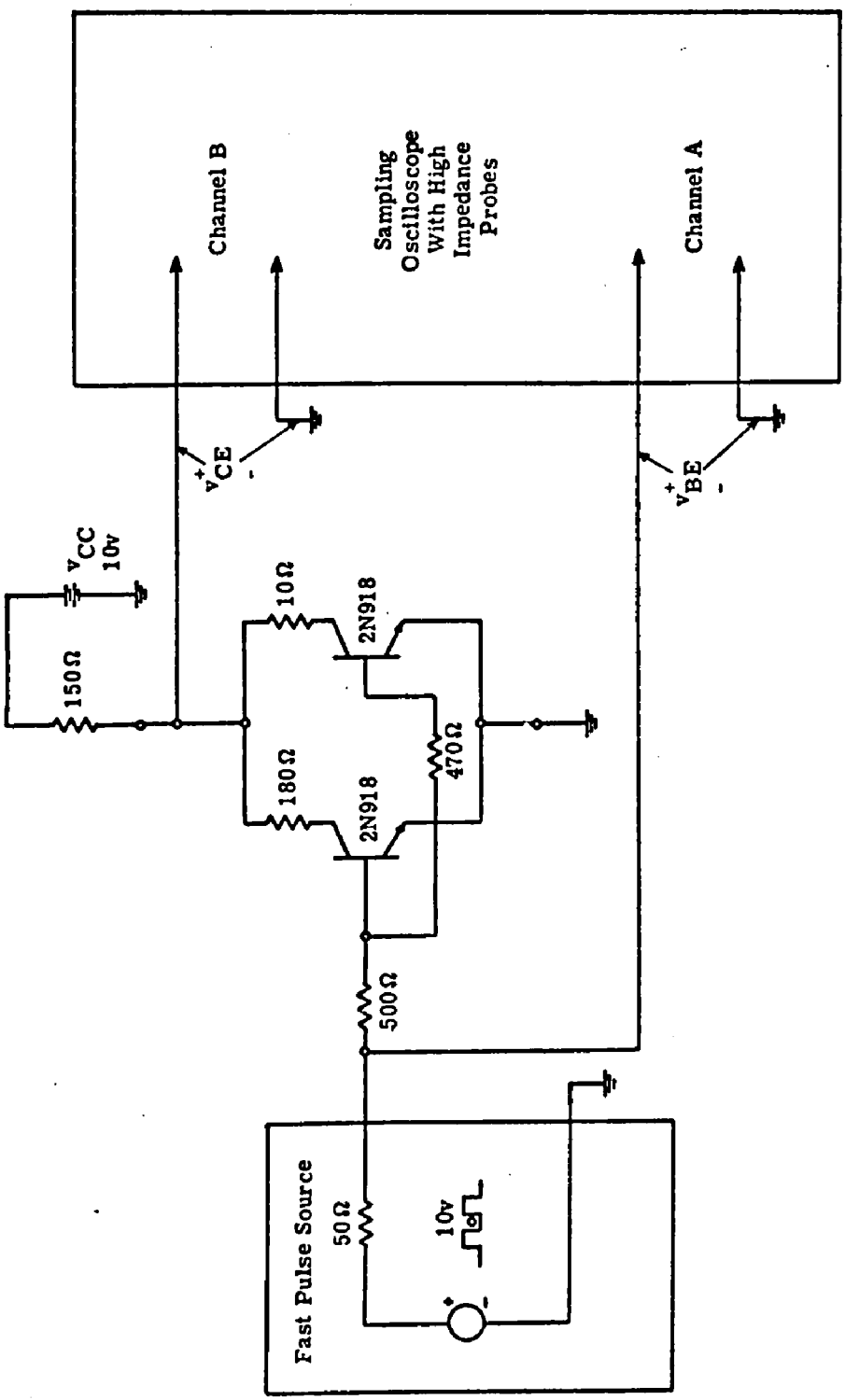


Fig. 2.30. Two-lump equivalent circuit using 2N918 transistors

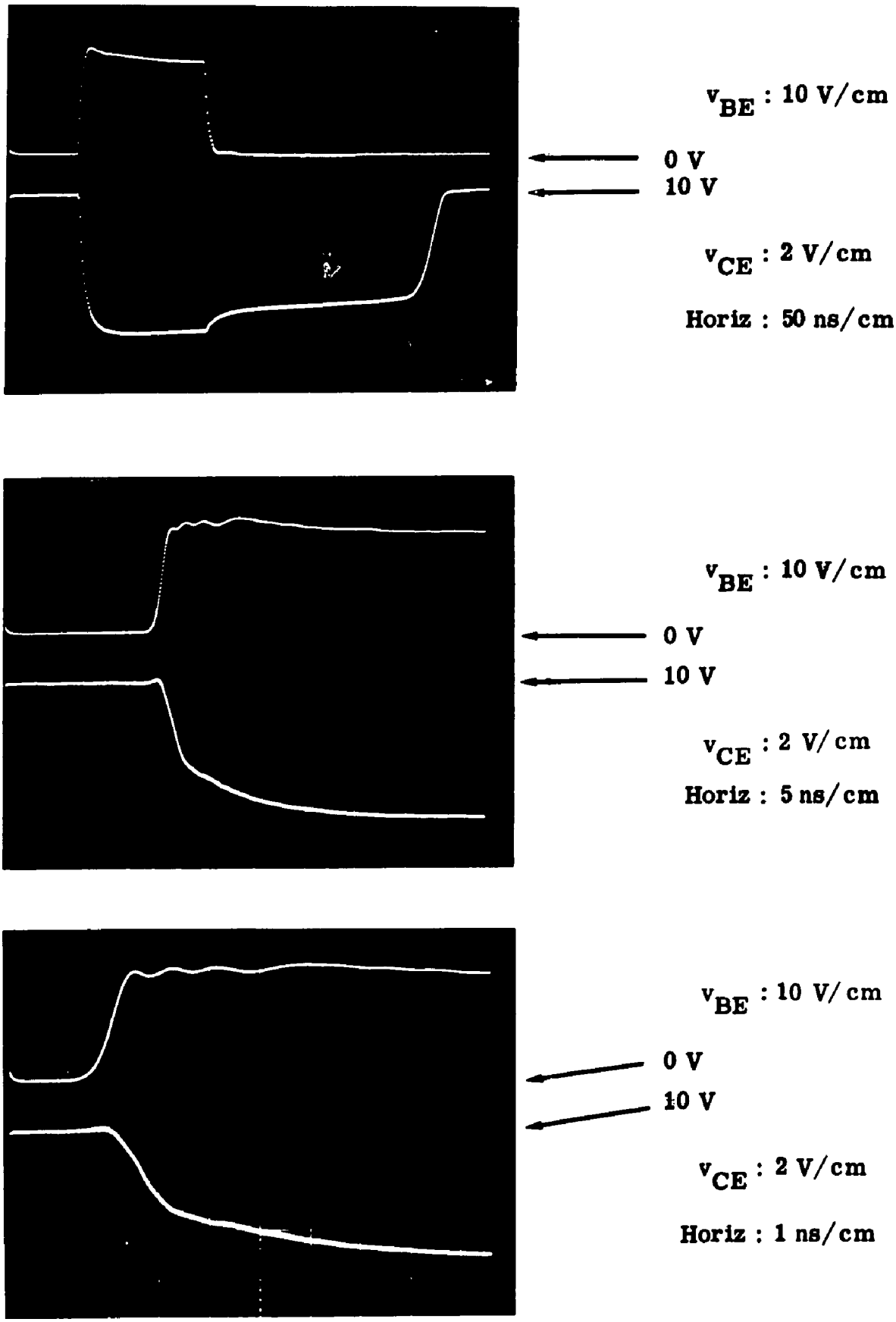


Fig. 2.31. Turn-on characteristics of two-lump equivalent

the two junctions and measuring the remaining resistances. Not only do the separate collector (and emitter) bulk resistances become paralleled, but their values are also reduced to a very minimum by conductivity modulation. As a result, the predominant resistances remaining in the base, collector, and emitter circuits are those attributable to the contact resistances. These are the resistances that were measured at low and high frequencies under conditions of large forward static bias current. With this multi-lump model, it is clear why the transient measurements yielded equivalent resistance values that were much larger than the resistances measured during static forward bias.

2.5.3.7 Selecting Equivalent Resistance Values for Single Lump Models. The main purpose of the various resistance measurements has been to establish suitable values for use in the wideband nonlinear transistor model (Fig. 2.13) used in the computer-aided circuit analysis of VHF power amplifiers. For class C operation in the VHF range, a transistor will be in saturation for only a few nanoseconds. During this short saturation time the device characteristics are best described by the resistances occurring just after the break in the initial turn-on time constant.

A final set of equivalent resistance values for the single lump nonlinear model have been established in the following manner:

1. Due to the high conductivity of the emitter region the emitter contact resistance is responsible for most of the emitter resistance. Also under transient "turn-on" conditions, the emitter-base junction is expected to become forward biased before the collector-base junction. Thus the emitter-base charge distribution will approach a steady-state distribution prior to device saturation. As a result, R_{EE} can be estimated from the average of the values obtained at low and high frequencies (Section 2.5.3.3) with static forward bias.

$$R_{EE} = \frac{(0.56 + 0.35)}{2} = 0.455\ \Omega$$

2. An average saturation resistance, R_{sat}, of $13.27\,\Omega$ was estimated from the switching test measurements (Eq. 2.44). The effective collector resistance can be estimated from this saturation resistance value.

$$R_{CC} = R_{sat} - R_{EE} = 13.27 - .455 = 12.82 \text{ ohms}$$

3. The curves of saturated resistance values as a function of bias current (Figs. 2.21 and 2.23) indicated that the ratio between the collector resistance and the base resistance remains fairly constant over a wide range of bias currents. This ratio can be used to estimate the value of effective

base resistance under transient conditions based on the effective value used for the collector resistance.

$$R_{BB} = \frac{R_{CC}}{\left(R_{CC_{sat}} / R_{BB_{sat}}\right)} = 12.82/(.572) = 22.45 \text{ ohms}$$

These final values

$$R_{BB} = 22.45\ \Omega$$

$$R_{CC} = 12.82\ \Omega$$

$$R_{EE} = 0.455\ \Omega$$

are used in the computer-aided analysis of typical VHF amplifiers to be discussed in following chapters.

2.5.4 Emitter Lead Inductance. A 2N3866 transistor is constructed with approximately 0.109 inch of one mil wire connecting the emitter tab of the semi-conductor chip to the emitter lead of a TO-5 package. An emitter lead self-inductance due to this wire can be estimated by the relationship

$$L = 2S\left[\ell n \frac{4S}{d} - \frac{3}{4}\right] \text{ nanohenries} \qquad (2.45)$$

where

S = length in centimeters

d = diameter in centimeters

for the inductance of a straight length of circular wire (Ref. G4). For

the 2N3866 we estimate an emitter lead inductance of 3.36 nanohenries. Similarly, a base lead inductance of 2.41 nanohenries results from the internal connection to the base region, but this inductance has not been included in the modeling of the 100 MHz amplifier since its reactance is expected to be small in comparison to the series base resistance R_{BB}.

An alternative method for estimating the device terminal inductances utilizes small signal high frequency saturated impedance data collected as described in Section 2.5.3.3. Reactance values resulting from such a measurement at a frequency of 100 MHz are plotted in Fig. 2.32. This plot indicates that the minimum terminal reactances are limited by transistor package and wire bond inductances of

$$L_{BB} = 1.495 \text{ nh}$$

$$L_{CC} = 0.43 \text{ nh}$$

$$L_{EE} = 1.64 \text{ nh}$$

Considering the size of the emitter inductance and the empirical[1] and experimental methods used, this measured value of emitter lead inductance is in moderate agreement with the 3.36 nh value predicted from

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[1] Alternative empirical relationships (Ref. H2) have been used to predict emitter inductance values ranging from 2.16 nh to the 3.36 nh predicted by Eq. 2.45.

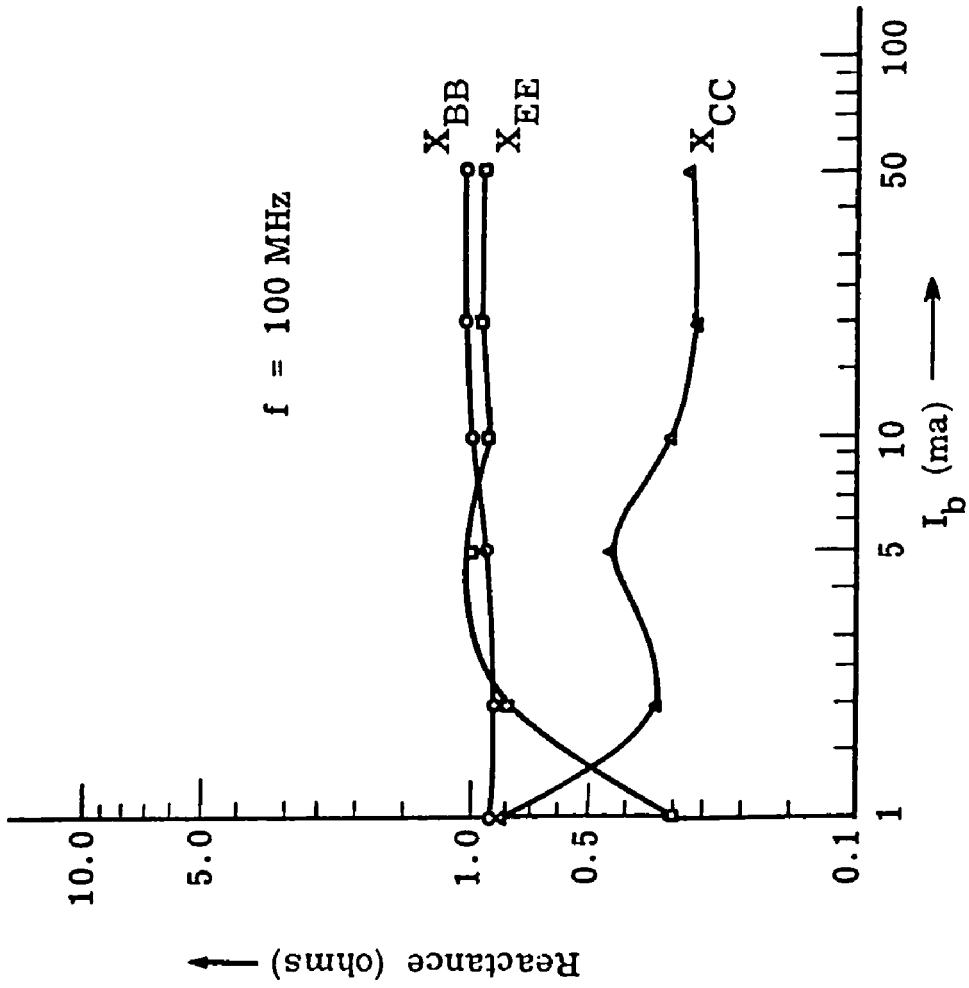

Fig. 2.32. Reactive parts of VHF saturated impedances

the physical dimension considerations. The larger value for L_{EE} (3.36 nh) is considered to be more appropriate for the computer simulated amplifier studies because this larger value helps to compensate for stray emitter circuit inductance that is inevitable in the construction of an experimental common emitter amplifier such as studied in Chapter 5. However, both values were used in computer simulations of a 100 MHz amplifier with no observed difference in computed amplifier performance. The sensitivity of computed amplifier performance to each of the model parameters is considered further in Chapter 5.

CHAPTER 3

ANALYSES WITH IDEAL SWITCH MODEL

3.1 Introduction

A primary objective in the design of RF power amplifiers is often that of obtaining the maximum output power from a given device. For a transistor stage, improvements in both output power and efficiency of energy conversion can be achieved by applying an excess of signal input power to drive the device rapidly between states of cut-off and saturation (Refs. S4, W1). In such overdriven situations the static collector-emitter characteristics of an intrinsic NPN transistor (Ref. M2) are useful for estimating the behavior of the transistor and the output circuitry.

$$V_{C'E'} = -\frac{1}{\lambda} \ell n \left[\frac{I_B' - \left(\frac{1-\alpha_F}{\alpha_F}\right) I_{COL}' + \frac{Q_{RS}}{\alpha_F \tau_R (1-\alpha_F\alpha_R)}}{I_B' + (1-\alpha_R) I_{COL}' + \frac{\alpha_R Q_{RS}}{\alpha_F \tau_R (1-\alpha_F\alpha_R)}} \right] \quad (3.1)$$

$$r_{C'E'} = \frac{\partial V_{C'E'}}{\partial I_{COL}'} = \frac{1}{\lambda} \left\{ \left[\frac{\left(\frac{1-\alpha_F}{\alpha_F}\right)}{I_B' - \left(\frac{1-\alpha_F}{\alpha_F}\right) I_{COL}' + \frac{Q_{RS}}{\alpha_F \tau_R (1-\alpha_F\alpha_R)}} \right] + \left[\frac{(1-\alpha_R)}{I_B' + (1-\alpha_R) I_{COL}' + \frac{\alpha_R Q_{RS}}{\alpha_F \tau_R (1-\alpha_F\alpha_R)}} \right] \right\} \quad (3.2)$$

In the saturation region with an excess base current, $I_B' >> I_{COL}'/\beta_F$, the saturation voltage, $V_{C'E'_{Sat}}$, can be expected to be a few tenths of a volt or less; and the saturation resistance, $r_{C'E'_{Sat}}$, will be a few ohms or less. Conversely, in the cutoff region, the output characteristics will appear as an open circuit. Thus, the output characteristics of an overdriven power amplifier stage can be expected to vary from a low impedance to a high impedance with the input excitation controlling the impedance variation. This variation between two conduction states can be modeled quite simply as an ideal controlled switch. The capacitive nature of the transistor output admittance can be represented by adding a capacitance in shunt with the controlled switch.

An ideal switch representation of a class C [1] amplifier output circuit is illustrated in Fig. 3.1. This representation cannot be used to examine the gain or input behavior of class C amplifiers, but it does model many of the dominant characteristics of the output circuit. Also, performance of this simplified class C circuit can be useful as a reference to gauge other circuits. Understanding of this basic circuit can provide an aid to the understanding of more realistic circuit representations.

Some questions concerning the fundamental characteristics of

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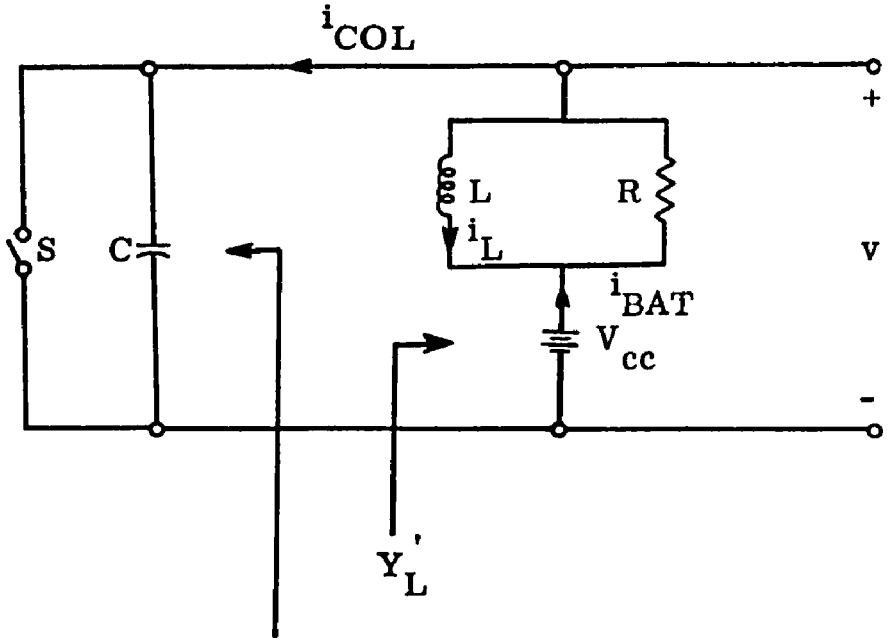
[1] When a device functions as an on-off switch in a tuned circuit, the mode of operation is often referred to as class D instead of Class C.



Idealized model of transistor output characteristics

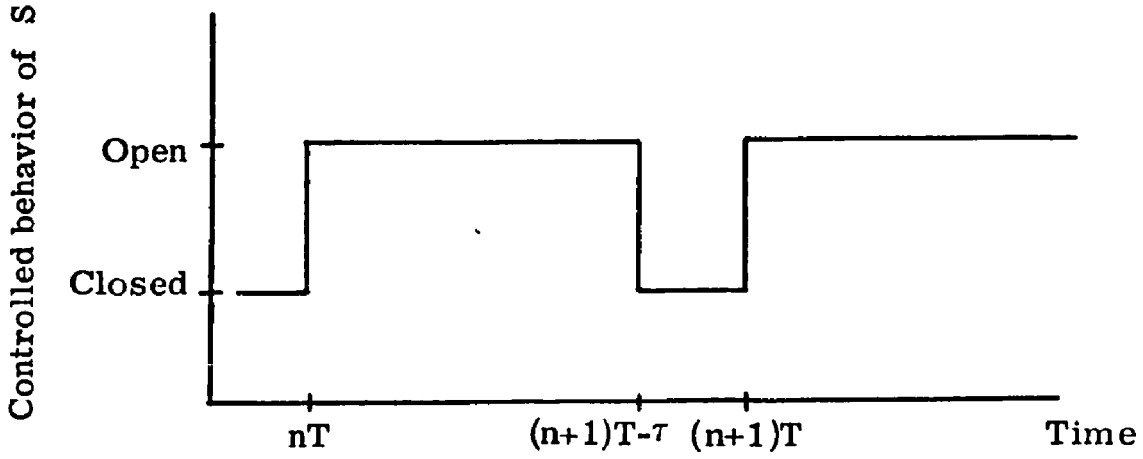


Fig. 3. 1. Idealized class C circuit

class C amplifiers that we have examined with the ideal switch representation are listed below:

(1) What value of R should be chosen to maximize the fundamental output power?

(2) What value of R should be chosen to maximize the output efficiency?

(3) How do the choices of R depend on the duty cycle (τ/T) of the switch?

(4) For a given R and C, what output bandwidth will be obtained?

(5) What harmonic power is expected, and how is it affected by other parameters?

(6) What is the effect of changing V_{cc}?

(7) How does the circuit behavior change if the output capacitance C is given a nonlinear voltage dependency?

(8) What is the influence of the configuration of the output tuning and matching network on amplifier performance?

In general, one cannot obtain closed-form mathematical expressions for answering such questions. However, the answers can be obtained by experimentation using analog or digital simulations.

An expression for the steady-state output voltage of the idealized circuit can be written as

$$v(t) = \begin{cases} V_{cc}\left[1 + \sqrt{\dfrac{1 - 2a\delta\omega_n + a^2\omega_n^2}{1 - \delta^2}}\; e^{-\delta\omega_n t} \sin\left(\omega_n\sqrt{1-\delta^2}\; t+\phi\right)\right] & \text{for } nT \leqq t < (nT - \tau) \\ 0 & \text{for } (nT - \tau) < t \leqq (n+1)T \\ n = 0, 1, 2, \ldots & \end{cases} \tag{3.3}$$

where:

$$\omega_n = \frac{1}{\sqrt{LC}}$$

$$\delta = \frac{1}{2R}\sqrt{\frac{L}{C}}$$

$$a = \left(\frac{L}{R} - \frac{I_{L_0} L}{V_{cc}}\right)$$

$$\phi = \tan^{-1}\left(\frac{a\omega_n\sqrt{1-\delta^2}}{1 - a\delta\omega_n}\right) - \tan^{-1}\left(\frac{\sqrt{1-\delta^2}}{-\delta}\right)$$

I_{L_0} = Current in L at time nT

Evaluation of this expression depends on the inductor current at the start of each cycle (I_{L_0}). A separate equation for I_{L_0} can be found by imposing the condition that the inductor current must be the same at the start and at the end of each cycle. Unfortunately, the resulting

equation has I_{L_0} imbedded in the arguments of transcendental functions, and a direct analytical solution for I_{L_0} is not possible. Although the I_{L_0} equation could be solved numerically, such an approach cannot be readily extended to the more realistic circuit representations that will follow. For this reason, analytical expressions for the circuit behavior are not pursued.

3.2 Numerical Analysis With Ideal Switch and Fixed Capacitance

An alternate approach for determining the circuit behavior is to solve the network differential equations with the aid of a digital computer. With this approach, an initial guess is taken for I_{L_0}, and an iterative procedure is followed until the correct network behavior is obtained. A flow chart of the computer algorithm used to determine the limit cycle of the ideal switch circuit is given in Fig. 3.2. After the limit cycle is established and the steady state waveforms are calculated, a Fourier analysis of the load voltage is performed to determine the fundamental output power and the harmonic content.

Typical waveforms obtained from numerical analysis of the ideal switch amplifier representation are shown in Fig. 3.3. As indicated, these sample waveforms are for the operating conditions of $\tau/T = 0.1$ with a circuit Q of approximately 10. As expected, the output voltage waveform is a damped sinusoid during the time the switch is open and is zero when the switch is closed. With the switch open the inductor current is also a damped sinusoid with negative

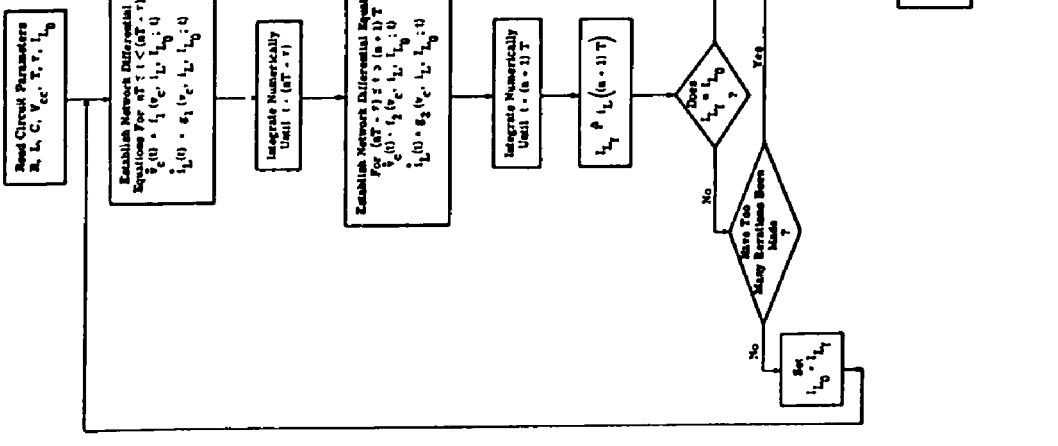


Fig. 3.2. Flow chart illustrating analysis of ideal switch circuit

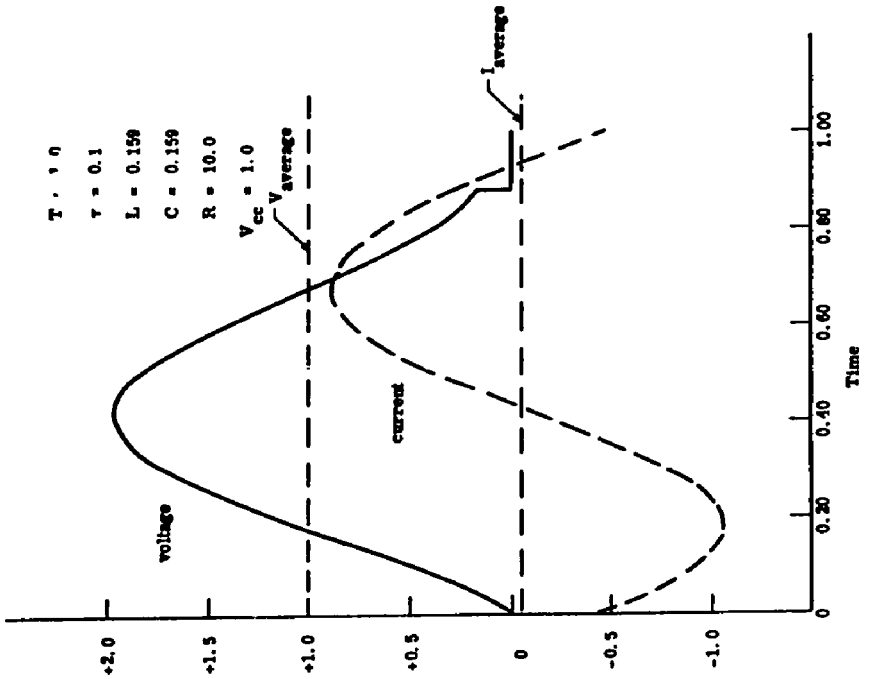


Fig. 3.3. Output voltage and inductor current waveforms

average value for the reference direction chosen. During the time the switch is closed, the constant supply potential is impressed across the inductor, causing a linear region in the inductor current waveform.

The conversion efficiency of the circuit is defined as the ratio of fundamental output power dissipated in R to the power supplied by the battery, V_{cc}.

$$\eta \triangleq P(1) \Big/ P_{V_{cc}} = - \frac{P(1)}{(V_{cc})\left(I_{L_{AVG}}\right)} \tag{3.4}$$

3.2.1 Effect of Switching Period. The effects of switching period (the circuit frequency response) on the fundamental output power, the efficiency, and the harmonic content of the circuit are illustrated in Figs. 3.4 and 3.5. The natural resonant frequency for the circuit, $\frac{1}{2\pi\sqrt{LC}}$, was scaled to unity for this example, and the maximum fundamental output power is found to occur at a driving frequency, $\frac{1}{T}$, slightly lower than the natural frequency. The efficiency peak is broader than the power peak and occurs at a slightly higher driving frequency. Further consideration of these frequency effects will be given in Section 3.2.3.

3.2.2 Effect of Load Resistance. If the load resistance is reduced below 10.0 ohms, the output power is increased but efficiency is decreased (Fig. 3.6) and harmonic content of the load voltage is increased (Fig. 3.7). Operation with large load resistances in the range

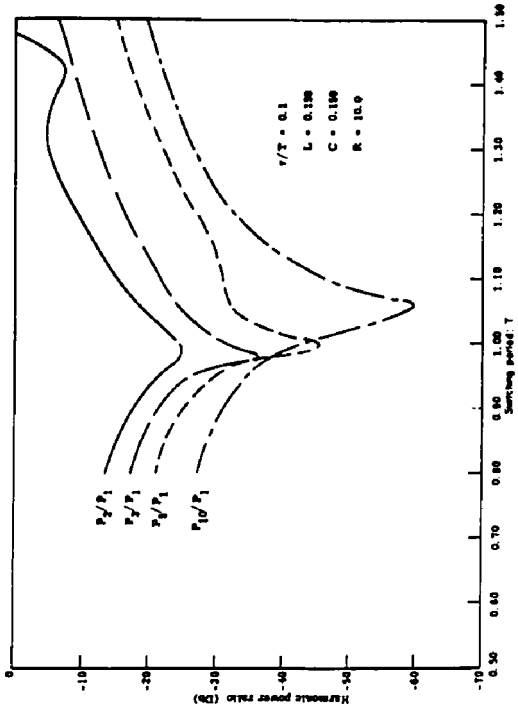


Fig. 3.5. Effect of switching period on harmonic content

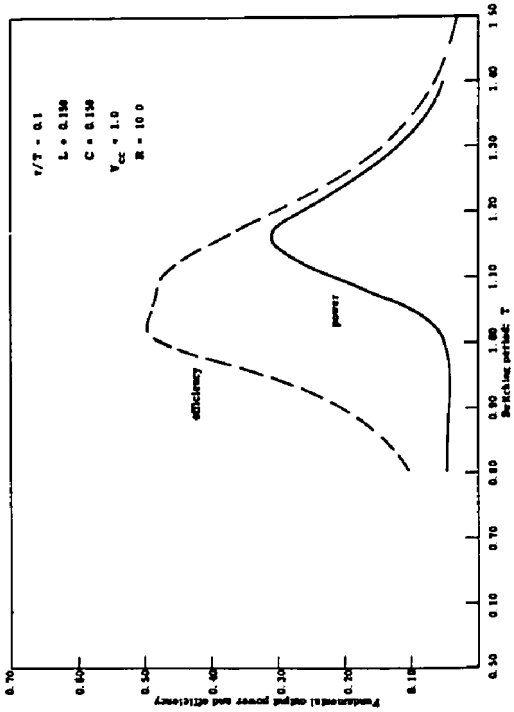


Fig. 3.4. Effect of switching period on power output and efficiency

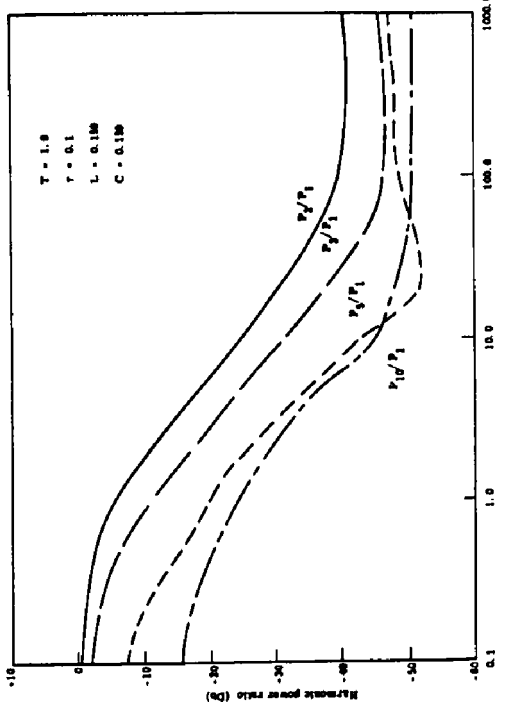


Fig. 3.7. Effect of load resistance on harmonic content

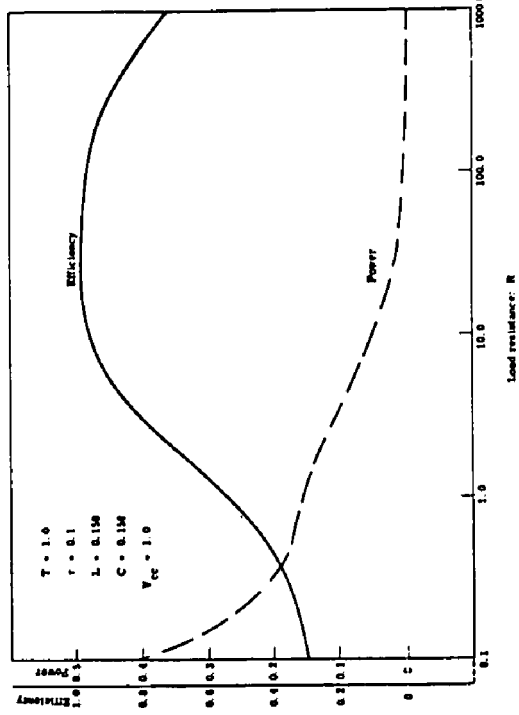


Fig. 3.6. Effect of load resistance on output power and efficiency

of 20.0 to 200.0 ohms leads to high conversion efficiency but very small output power.

The energy delivered to this ideal switch amplifier circuit during each period of operation is proportional to the square of the length of time the switch is closed. This is not surprising since the inductor current changes linearly during this time. In steady-state, most of the net energy added each period is frequency converted by the switching operation and dissipated in the load resistor. A small amount of energy is stored in the capacitor at the instant the switch is closed, and this energy is lost in switching. Thus the efficiency and power output of the circuit depend on the switching duty factor, τ/T, as well as the switch driving period, T.

3.2.3 Effect of Switch Conduction Angle. The conduction angle of a class C amplifier is equivalent to the duty cycle of the idealized circuit expressed in degrees.

viz. $$\theta = \frac{\tau}{T} \times 360^{o}$$

For a class C amplifier, the conduction angle is normally set by the base bias circuitry and the power level of the input signal. In general, the conduction angle can be expected to increase with increases in input driving power. As will be demonstrated, such changes in the conduction angle can have an effect similar to detuning the output circuit. In an actual transistor amplifier, changes in input power can also shift the operating point of the transistor and produce changes in the

"effective" admittances of the device. These admittance changes often cause noticeable detuning of the amplifier. With this idealized amplifier circuit, however, we can examine the effect of conduction angle variations without becoming involved in admittance variations of nonlinear elements.

The effect of varying the duty cycle while maintaining a fixed driving frequency is illustrated in Fig. 3.8. Here, the driving frequency was chosen to be the same as the natural frequency of the network when the switch is open (i.e., $T = 2\pi\sqrt{LC}$). The fundamental output power is observed to increase with the conduction angle as expected. For the larger conduction angles, however, the harmonic content in the output power (Fig. 3.9) begins to increase with the conduction angle. Thus, increasing fundamental output power by means of increases in conduction angle ultimately results in a decrease in output circuit efficiency. The efficiency might be expected to approach unity asymptotically as the conduction angle is reduced to zero; however, Fig. 3.8 shows that the efficiency decreases with conduction angle for the smaller conduction angles. The efficiency plotted here is the ratio of the fundamental output power to the total power supplied to the circuit. To achieve unit efficiency the harmonic power would have to be zero, that is, the output voltage waveform would be a pure sinusoid at the fundamental frequency, and no energy could be lost in the switch. Such a condition would require high circuit Q in addition to very narrow conduction angles. In addition, for

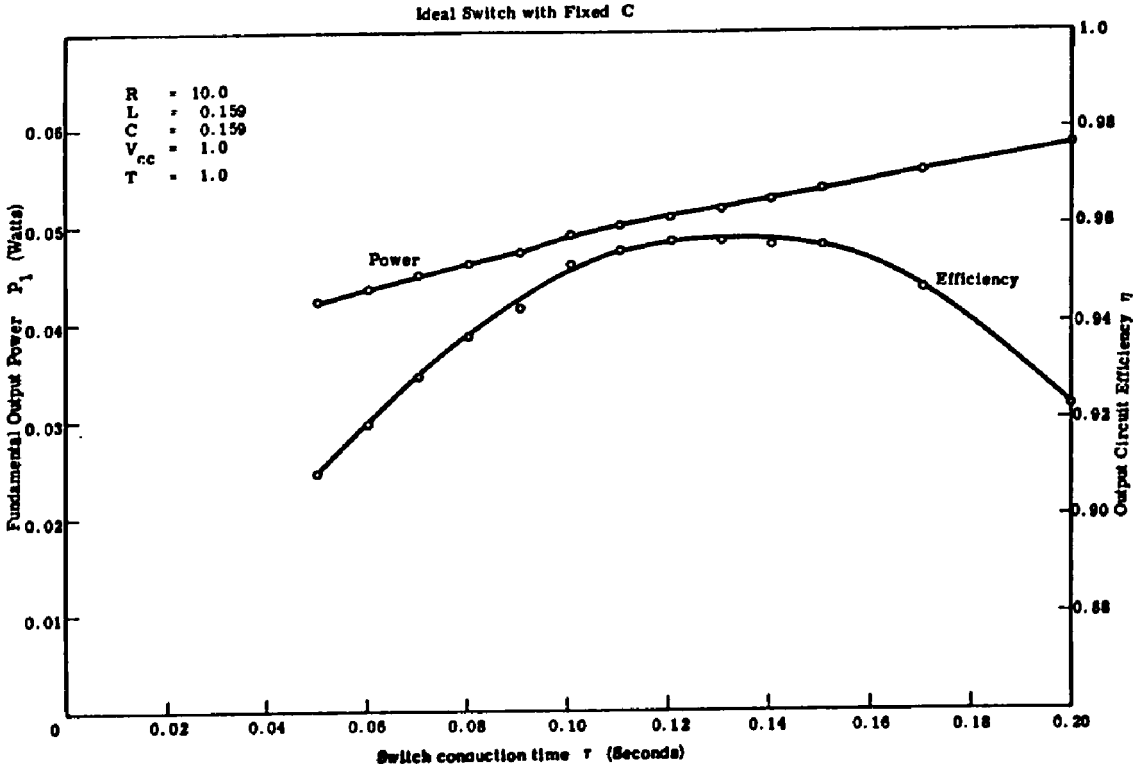


Fig. 3.8. Influence of switch conduction time on output power and efficiency

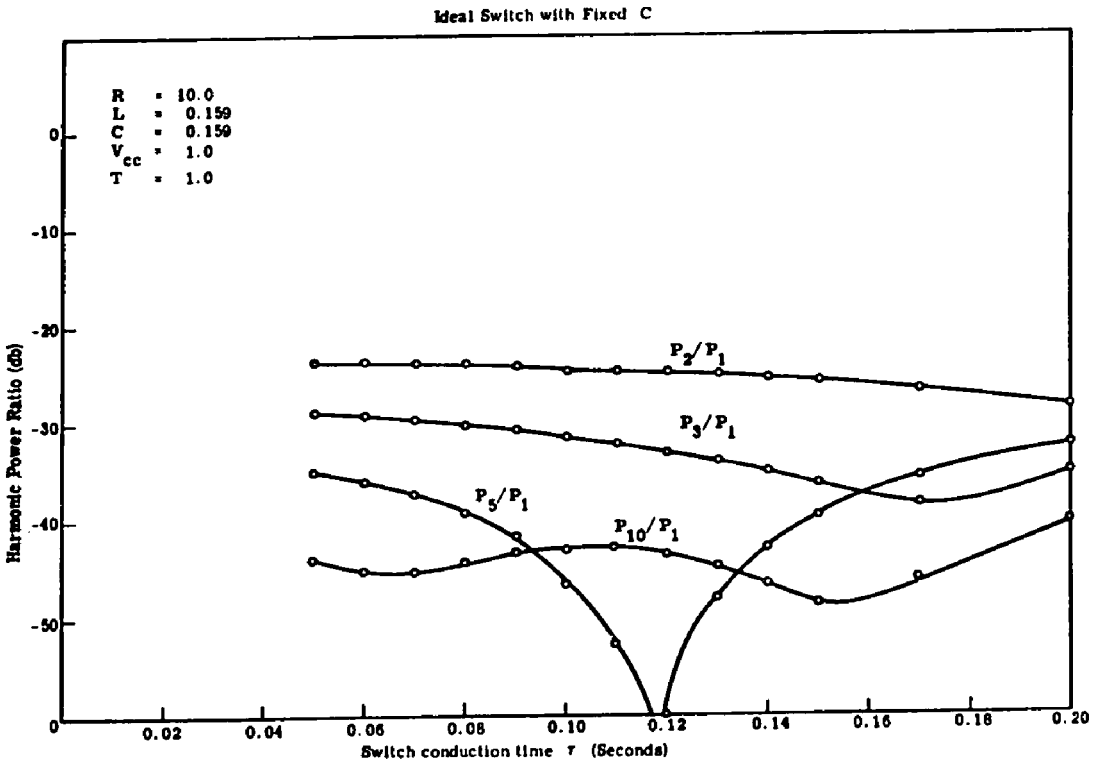


Fig. 3.9. Influence of switch conduction time on harmonic content

unity efficiency the switch must not dissipate energy. In the idealized circuit being considered, an energy loss of $(1/2)\,C[v(T-\tau)]^2$ occurs each time the switch shorts the capacitor. Thus, an average power loss of $C[v(T-\tau)]^2/2T$ must be attributed to the switch. This can be zero only if the switch closes precisely when the output voltage is zero. In the finite Q, narrow conduction angle case, the output voltage will not return to zero with the switch open, and some power will be lost in the switch. For a fixed Q this switch power does not approach zero as the conduction angle goes to zero, and as a result, the efficiency is degraded at the very small conduction angles. Figure suggests that a conduction angle of about 47 degrees will produce optimum efficiency if the Q of the output circuit is about 10 and the natural frequency of the output circuit is the same as the driving frequency.

If the driving frequency is adjusted for each conduction angle, the changes in apparent resonant frequency of the output circuit can be observed. This has been done in Figs. 3.10, 3.11, 3.12 and 3.13 which plot efficiency and output power as a function of the switching period T, where T is just the reciprocal of the driving signal frequency.

For these calculations the natural resonant period (T_N) of the circuit with the switch open is again chosen to be unity and the circuit Q is 10.

$$T_N = 2\pi\sqrt{LC} = 1 \qquad (3.5)$$

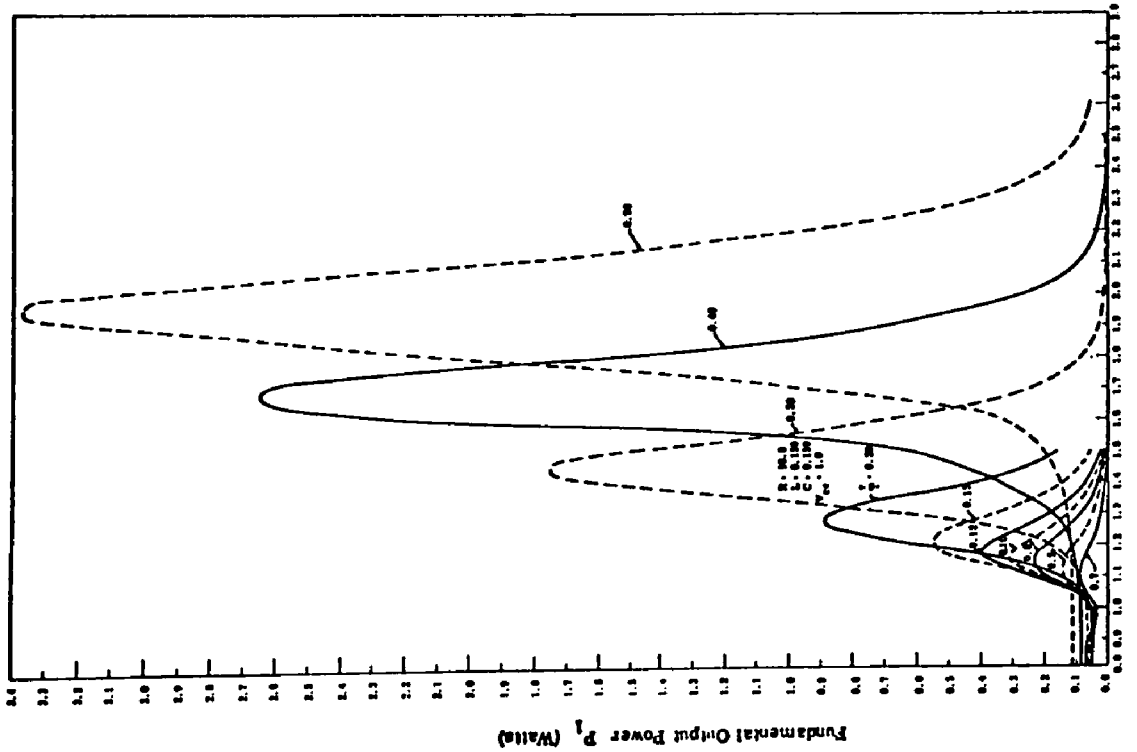


Fig. 3.11 Effect of switch duty factor on frequency behavior of output power

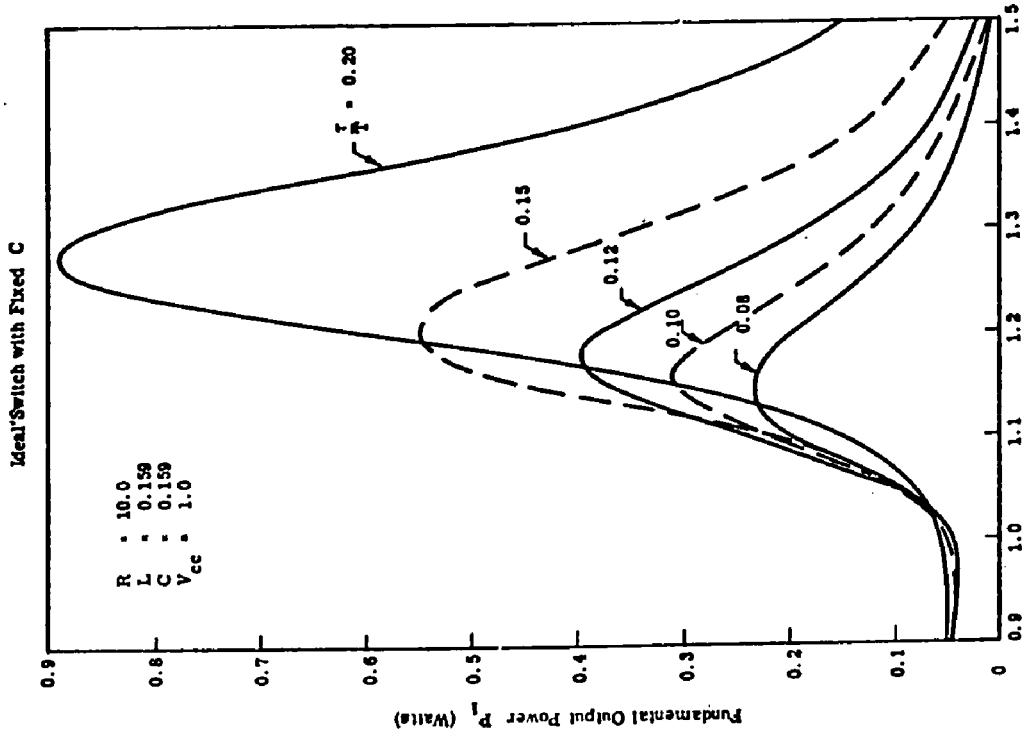


Fig. 3.10. Effect of switch duty factor on frequency behavior of output power (expanded scale)

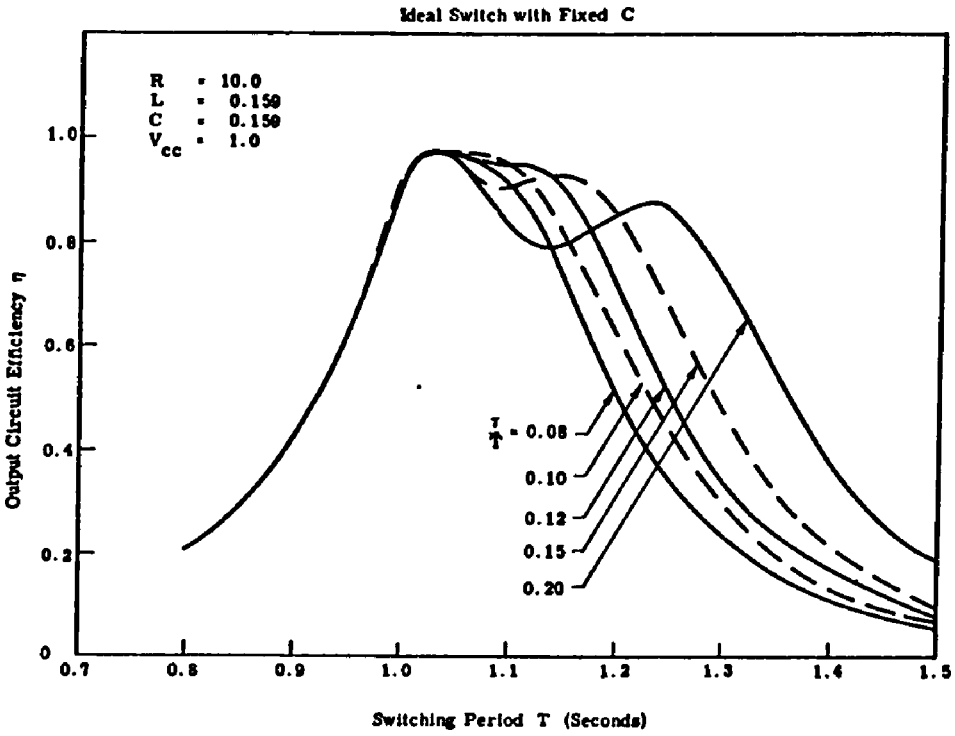


Fig. 3.12. Effect of switch duty factor on frequency behavior of efficiency (expanded scale)

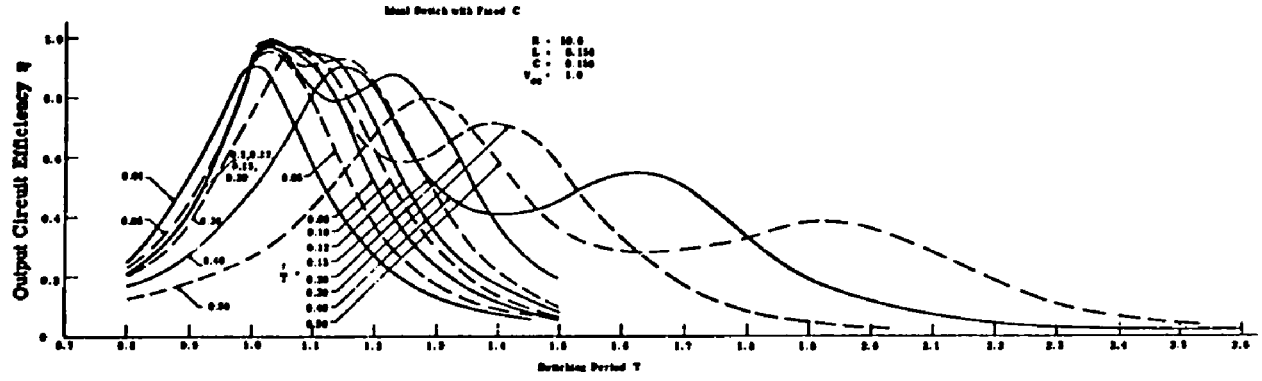


Fig. 3.13. Effect of switch duty factor on frequency behavior of efficiency

$$Q = \frac{2\pi RC}{T_N} \tag{3.6}$$

One observes that the fundamental output power and the efficiency always reach a maximum for switch (excitation) periods greater than the natural period of the circuit. The efficiency curves exhibit an unexpected double peak for larger duty factors. The first peak ($T_{\hat{\eta}_1}$) is always close to T_N, and the period of the second peak ($T_{\hat{\eta}_2}$) is related to the natural period and duty factor by

$$T_{\hat{\eta}_2} = \left[1 + \left(\frac{\tau}{T}\right)\right] T_N \tag{3.7}$$

As a consequence of the second peak, one observes that the efficiency stays relatively high over the entire range of excitation periods $T_N \leq T \leq T_N + \tau$. The curves of fundamental output power can also exhibit a double-peak for small duty factors; but in contrast to the efficiency curves, the power curves become double-peaked for small duty factors. It will be seen that when the power response has two peaks ($T_{\hat{p}_1}$ and $T_{\hat{p}_2}$), the period of the second peak $T_{\hat{p}_2}$ (the longer of the two switching periods) is the more useful of the two. We will adopt the notation $T_{\hat{p}}$ to designate $T_{\hat{p}_2}$ in the cases of double-peaked power response curves and to designate the period for peak response in the single-peaked cases. We see that in all cases

$$T_{\hat{p}} > T_{\hat{\eta}_2}$$

with both $T_{\hat{p}}$ and $T_{\hat{\eta}_2}$ approaching T_N as the duty factor approaches zero.

In order to understand the cause of the double peaks in the efficiency and output power response curves, it is helpful to observe the typical load voltage waveforms that occur near the response peaks. The response curves of Figs. 3.11 and 3.13 were obtained from data computed at discrete switching periods from $T = 0.8$ sec to $T = 2.5$ sec in steps of 0.05 sec. Thus the waveforms presented (Fig. 3.14) do not correspond exactly to the switching periods for the response peaks but they are near those periods. Figure 3.14 shows the three voltage waveforms calculated for a duty factor of 0.05 at the two output power peaks and the single efficiency peak. For this example, a switch-driving period of 1.05 sec ($T_{\hat{\eta}_1}$) produces the maximum output circuit efficiency of 0.925, and a fundamental output power of 0.0844 watts is developed. Increasing the switching period to 1.10 ($T_{\hat{p}_2} = T_{\hat{p}}$) causes the output power to reach its maximum of 0.140 watts, but the efficiency is reduced to 0.773.

A switching period of 0.85 sec ($T_{\hat{p}_1}$) produces another power peak, but at this peak the output power is only 0.0568 watts, and the circuit efficiency is a much lower 0.313. It is clear that this power peak at the shorter switching period is not a useful operating condition. However, it appears that during experimental tuning of an amplifier for maximum output power, one might inadvertently tune to this poor performance point and be unaware that a preferable tuning condition exists.

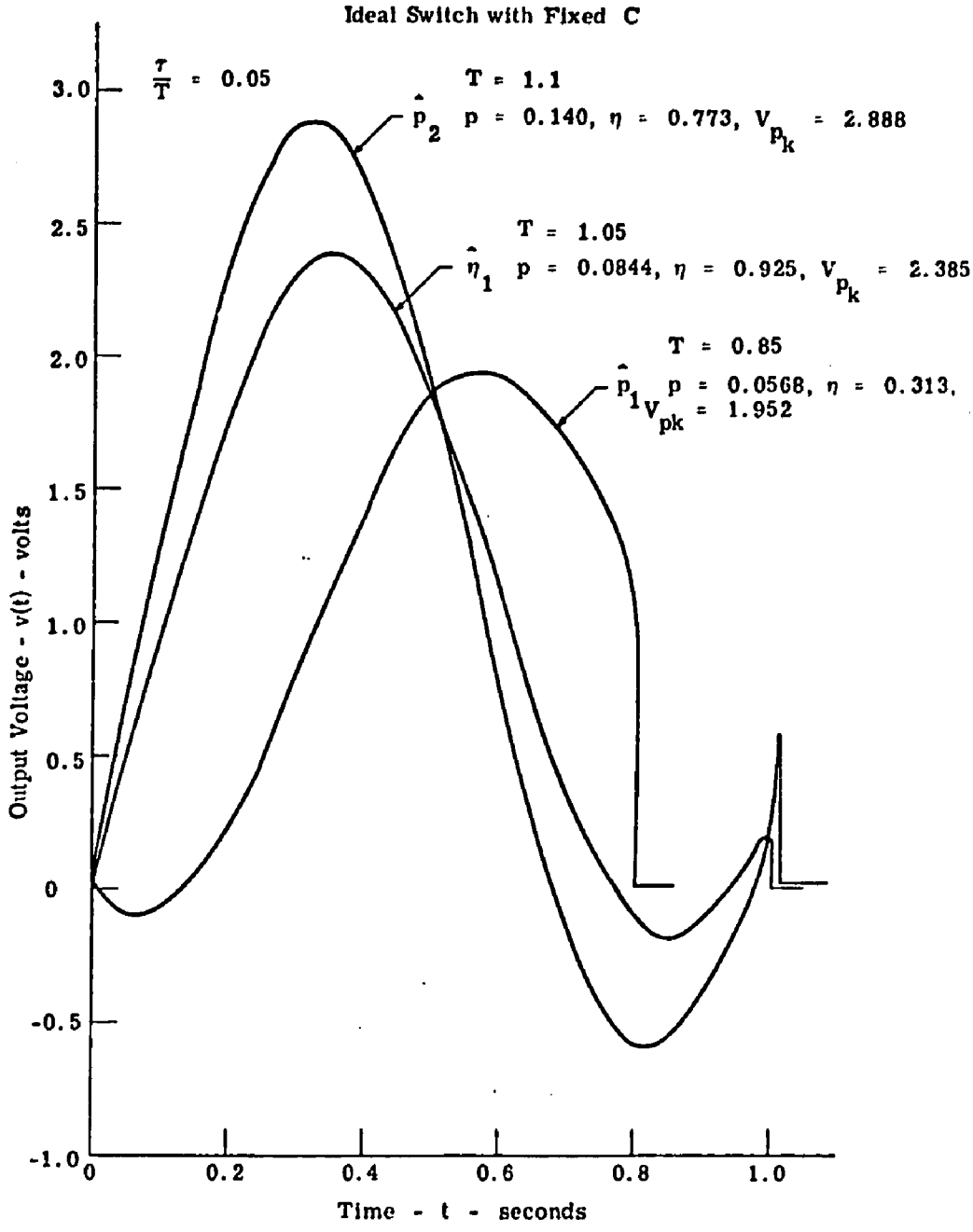


Fig. 3.14. Output voltage

The waveform at the maximum efficiency point is that of a damped sinusoid with the switch being closed as the sinusoid passes through zero at the end of one complete cycle. For the maximum output power condition the switch is allowed to remain open longer and is closed when the output voltage is larger thus causing an increase in switching power loss. This relationship between the waveforms for maximum efficiency and maximum power is typical for all the duty factors that have been investigated.

An analysis of the harmonic power content of each of the three waveforms is presented in Fig. 3.15. Operation at the maximum efficiency point provides a 4 to 5 dB reduction of harmonic power in comparison to operation at the maximum power point. The larger waveform discontinuities that exist for the maximum power conditions are responsible for the increased harmonic power at the higher frequencies.

Typical waveforms for a large duty factor ($\tau/T = 0.3$) are shown in Fig. 3.16. In this case only one driving period produces a maximum in output power, but there are two distinct driving periods that produce peaks in the conversion efficiency. Unlike the small duty factor case, neither of the peak efficiency operating points can be so quickly discounted. However, further considerations will show that the condition yielding the full cycle sinusoid is preferable to the condition for the half cycle sinusoid. The net result is essentially the same for large duty factors as for small duty factors. That is,

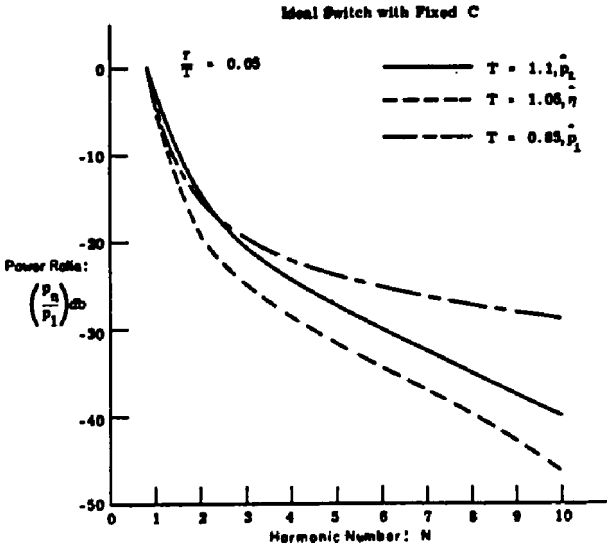


Fig. 3.15. Harmonic content

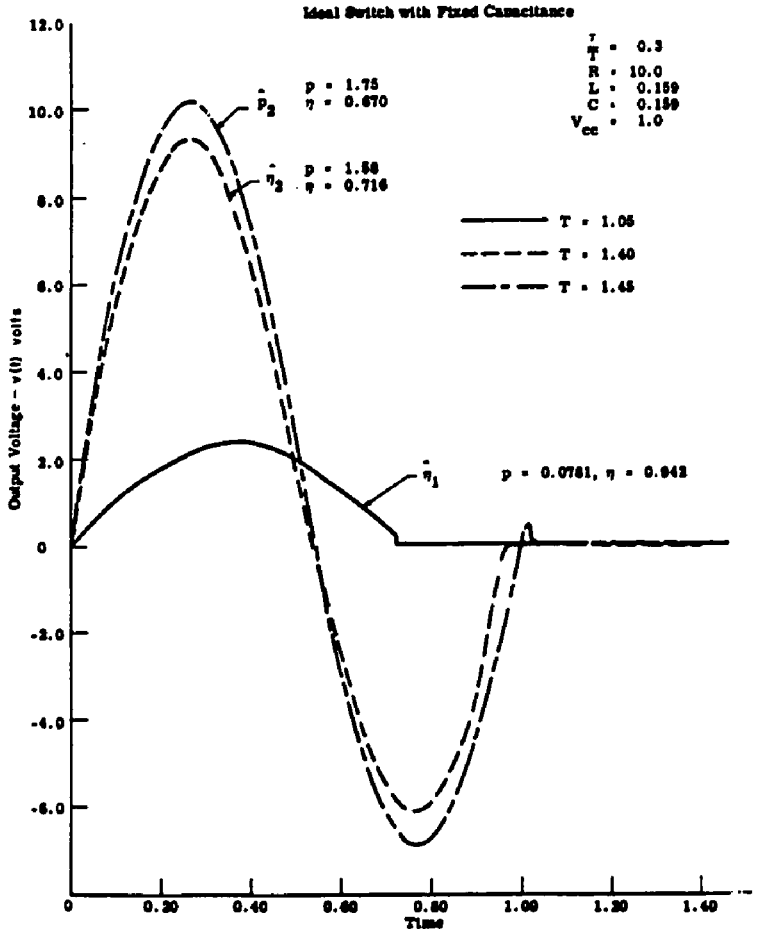


Fig. 3.16. Output voltage

maximum efficiency results if the switch is closed as the output voltage passes through zero after one complete sinusoidal cycle, and maximum output power results if the switch is closed at a slightly later time.

It is interesting to see what effect the switch duty factor has in determining the center frequency for peak output power and the half power bandwidth of the idealized output circuit. This information is available in Fig. 3.11 and is plotted in Fig. 3.17. Both the center frequency $f_{0_{\hat{p}}}$ and the bandwidth $BW_{\hat{p}}$ decrease almost linearly with increases in switch duty factor; but their ratio, $Q_{\hat{p}} = f_{0_{\hat{p}}} / BW_{\hat{p}}$ remains fairly constant at a value of 5.8 ± 0.6 over the entire duty factor range.

The peak output power, $\hat{p}$, and the maximum efficiency obtainable, $\hat{\eta}$, both depend on the switching duty factor. This variation in $\hat{p}$ and $\hat{\eta}$ is illustrated in Fig. 3.18. Recall that the curve for $\hat{p}$ occurs for a different set of tuning conditions than those for $\hat{\eta}$, and thus it is not possible to satisfy the conditions of both curves simultaneously. The driving periods of the switch for obtaining maximum power $T_{\hat{p}}$ and for obtaining maximum efficiency $T_{\hat{\eta}}$ are related to the switch duty factor as shown in Fig. 3.19.

Our study shows that we can tune the output circuit to obtain maximum efficiency or maximum output power with a given supply voltage, load resistance, and output capacitance; but we cannot tune for both conditions. Which condition is preferable? Suppose the

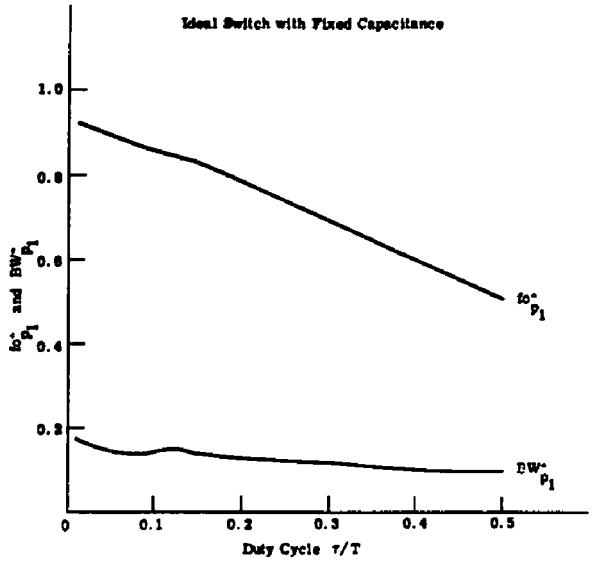


Fig. 3.17. Center frequency and bandwidth

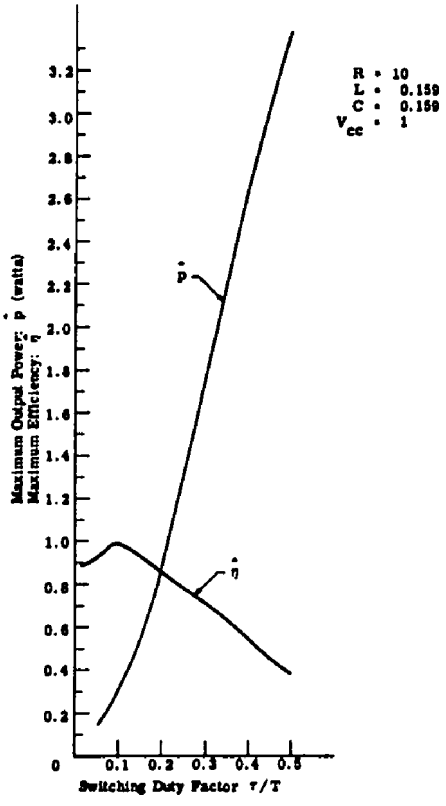


Fig. 3.18. Maximum output power and maximum efficiency vs switching duty factor

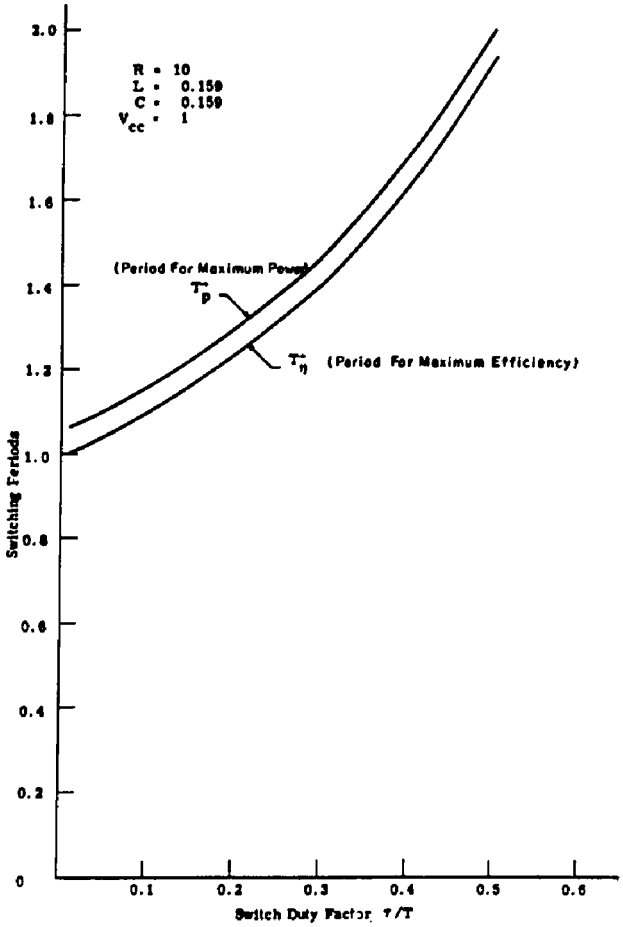


Fig. 3.19. Switching periods for maximum power and maximum efficiency

design problem is to develop the output tuning network of a single frequency, common emitter, class D transistor amplifier such that fundamental output power will be as large as possible with a given transistor operating with a duty factor of 0.30. Operating at the peak of the output power response, we get (from Figs. 3.11, 3.13, and 3.16)

$$T_{\hat{p}} = 1.45 \text{ sec}$$

$$P_{\hat{p}} = 1.75 \text{ watts}$$

$$\eta_{\hat{p}} = 0.72$$

$$V_{\hat{p}} = 10.25 \text{ volts}$$

At the shorter period efficiency peak

$$T_{\hat{\eta}_1} = 1.05 \text{ sec}$$

$$P_{\hat{\eta}_1} = 0.0781 \text{ watt}$$

$$\hat{\eta}_1 = 0.942$$

$$V_{\hat{\eta}_1} = 2.34 \text{ volts}$$

and at the longer period efficiency peak

$$T_{\hat{\eta}_2} = 1.40 \text{ sec}$$

$$P_{\hat{\eta}_2} = 1.58 \text{ watts}$$

$$\hat{\eta}_2 = 0.716$$

$$V_{\hat{\eta}_2} = 9.37 \text{ volts} .$$

If we assume that the power dissipated by the switch, PD, is the same as the total nonuseful dissipated power,[1] then

$$PD_{\hat{p}} = (1 - \eta_{\hat{p}}) P_{\hat{p}}$$

$$= 0.856 \quad \text{watts}$$

$$PD_{\hat{\eta}_1} = 0.00484 \text{ watts}$$

$$PD_{\hat{\eta}_2} = 0.616 \quad \text{watts}$$

In order to compare the three operating points in terms of output power limits due to device dissipation constraints, we can increase the power supply voltage at the $\hat{\eta}_1$ and $\hat{\eta}_2$ conditions until

$$PD_{\hat{\eta}_1}' = PD_{\hat{\eta}_2}' = PD_{\hat{p}} .$$

The resulting output powers scale to

$$P_{\hat{\eta}_1}' = \frac{PD_{\hat{p}}}{PD_{\hat{\eta}_1}} \cdot P_{\hat{\eta}_1} = 1.38 \text{ watts} ,$$

---

[1] In terms of device dissipation considerations this is a rather pessimistic assumption for it asserts that all harmonic energy is dissipated by the switch rather than the load. Nonetheless this assumption is reasonable for high Q loads and provides a useful standard for comparison of the tuning conditions.

$$P_{\hat{\eta}_2}{}' = \frac{PD_{\hat{p}}}{PD_{\hat{\eta}_2}} \cdot P_{\hat{\eta}_2} = 2.20 \text{ watts} ,$$

which should be compared to

$$P_{\hat{p}} = 1.75 \text{ watts} .$$

Thus for the same device power dissipation, operation at the longer period of the two periods for peak efficiency will allow larger output power than either of the other operating points considered. Of course, this comparison has been made under the assumption that the peak voltages do not exceed the device breakdown limits at any of the operating points.

An alternate form of output power scaling is required in order to compare the three operating points on the basis of output power limits within the constraint of equal peak voltage amplitudes. In this case the supply voltage can be varied at the $\hat{\eta}_1$ and $\hat{\eta}_2$ operating points such that the scaled peak output voltages $V_{\hat{\eta}_1}{}''$ and $V_{\hat{\eta}_2}{}''$ satisfy

$$V_{\hat{p}} = V_{\hat{\eta}_1}{}'' = V_{\hat{\eta}_2}{}'' .$$

Under these conditions the scaled output powers become

$$P_{\hat{\eta}_1}{}'' = \left(\frac{V_{\hat{p}}}{V_{\hat{\eta}_1}}\right)^2 P_{\hat{\eta}_1} = 1.49 \text{ watts}$$

$$P_{\hat{\eta}_2}'' = \left(\frac{V_{\hat{p}}}{V_{\hat{\eta}_2}}\right)^2 P_{\hat{\eta}_2} = 1.88 \text{ watts}$$

Again operation at the longer peak efficiency period yields the most output power under the limiting device constraints.

The power output comparison procedure explained above has been conducted for each of the switch duty factors, and the results are shown in Fig. 3.20. The comparison in this figure is only for the power scaling of the peak efficiency points with the longer periods and the peak output power points of the longer periods since these are the useful points from the double-peaked responses. In terms of device dissipation limitations, it is always preferable to operate at the peak efficiency point. In terms of device breakdown voltage limitations, it appears that the choice of tuning condition depends on the switch duty factor. In a design effort to squeeze the maximum output power from a given device, it seems necessary to supplement the usual laboratory adjustment techniques with information gained from computer analysis and constrained optimization of the circuit design.

It should be observed that tuning for conditions other than maximum output power with a fixed supply voltage is not free from danger of causing device damage. For example, consider tuning to the maximum efficiency condition and increasing the supply voltage until the device power dissipation limit is reached. If the input driving frequency were to decrease slightly, the output power would

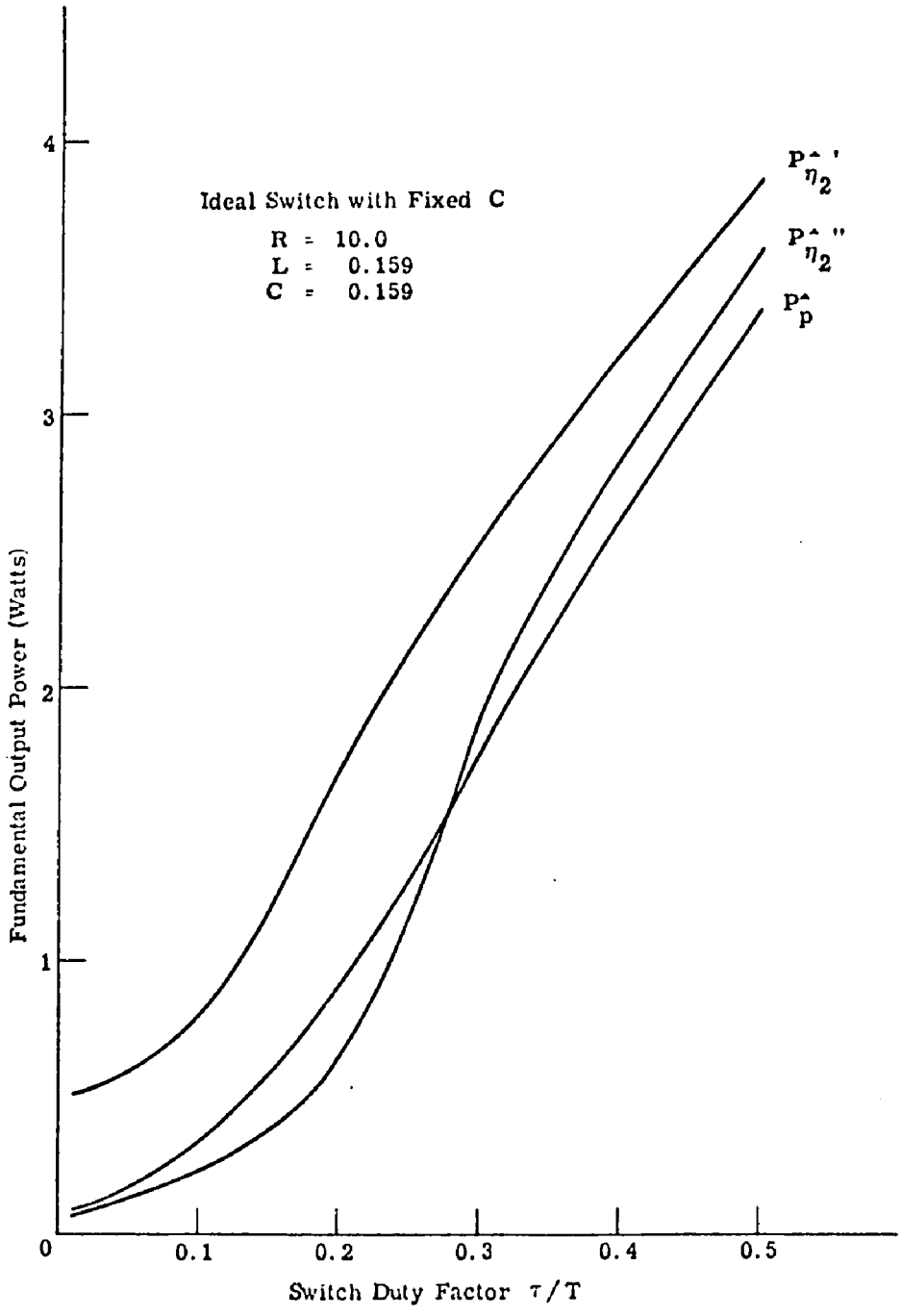


Fig. 3.20. Scaled output power

increase, the efficiency would decrease, and the device power dissipation limit would then be exceeded. Thus, in this sense, it does not seem to be good engineering practice to design only for conditions of maximum efficiency at the operating frequency.

3.2.4 Effect of Circuit Capacitance. To understand the effect of the capacitance value on circuit performance, consider the effect of doubling the circuit capacitance while halving the inductance to maintain a constant natural frequency. The load resistance for obtaining maximum output power will now be just one half of its original value. If the load resistance is halved, then the entire network impedance will be reduced by a factor of two. Thus for the same supply voltage, the output power will double and the circuit efficiency will remain the same as in the original circuit.

3.2.5 Effect of Supply Voltage. Since the idealized circuit representation is linear, increases in supply voltage will produce linear increases in the amplitudes of all the circuit voltages and currents. The output power will increase as the square of the supply voltage, and the efficiency will remain unchanged. Because of these simple relationships, the supply voltage parameter need not be considered further until more general nonlinear circuit representations are encountered.

3.3 Ideal Switch with Nonlinear Capacitance

The ideal switch circuit of Fig. 3.1 can be made more representative of the output circuit of a class C transistor amplifier if the capacitor value is assigned a nonlinear dependence on its terminal voltage. The expression chosen for the depletion layer or barrier capacitance of a junction diode is (see Section 2.5)

$$C_{DEP}(v) = \frac{C_J}{[A(v)]^{\gamma}} + C_F \tag{3.8}$$

where

$$A(v) \triangleq \text{Supremum} \left\{ \begin{matrix} v + V_Z \\ A_{LIM} \end{matrix} \right\}$$

and

C_J is a capacitance constant dependent on the junction area and the semiconductor doping concentrations

VZ is the junction barrier potential dependent on the semiconductor material used

γ is an exponential constant that typically lies in the range of 0.2 to 0.5 depending on the junction impurity profile

C_F is a fixed capacitance resulting from overlay and bonding capacities

A_{LIM} is a limiting value of the voltage dependent argument chosen to limit the maximum depletion capacitance and to prevent the capacitance from attaining negative values

The capacitor current for this capacitance representation is given by

$$i_c(t) = C[v(t)] \times \frac{d}{dt} v(t) \qquad (3.9)$$

For convenience in entering data into the analysis program an equivalent capacitance is defined as the capacitance present when the output voltage is V_{cc}.

$$CEQVCC \triangleq C_{DEP}(v)\Big|_{v=V_{cc}} = \frac{C_J}{\left(V_{cc} + V_z\right)^{\gamma}} + C_F \qquad (3.10)$$

For the following analyses the value of the fixed capacitance was arbitrarily selected to be ten percent of the equivalent capacitance,

$$C_F = 0.1 \times CEQVCC$$

and the limiting value of the argument was chosen as

$$A_{LIM} = 0.01 \text{ volt} .$$

The remaining parameter values for defining the nonlinear circuit capacitance; CEQVCC, VZ, and γ are entered as data in the analysis program so that their significance in the circuit behavior can be investigated.

In previous analyses of the linear idealized circuit, values of R = 10, L = 0.159, and C = 0.159 produced a maximum in fundamental output power when the switching period T was 1.17. To

establish a nominal value for CEQVCC in this nonlinear case, the behavior of output power with CEQVCC was observed under conditions similar to those in the linear circuit (Fig. 3.21). A value of CEQVCC = 0.159 is seen to produce a fundamental output power peak near T = 1.17, and this value of CEQVCC was taken as the nominal capacitance value in the nonlinear case in order to enhance the similarity with the linear case.

Typical waveforms and capacitance variations for this nonlinear circuit near resonance are shown in Fig. 3.22. Here the total circuit capacitance is seen to vary by a ratio of 5 to 1 during one cycle of the periodic output. Even with this large capacitance variation, the dependence of output power, efficiency, and harmonic content on switching period, load resistance, and duty cycle (Figs. 3.23, 3.24, 3.25, 3.26, 3.27) are found to be almost identical to the behaviors observed in the linear case. The circuit performance is also surprisingly independent of the values taken for the parameters VZ and γ. In Figs. 3.28 and 3.29 we observe that a 10 to 1 variation in VZ or γ produces only about 20 percent variation in fundamental output power and about 10 percent variation in output circuit efficiency. The effects of switching duty factor on the frequency response of output power and conversion efficiency with the nonlinear capacitance case are illustrated in Figs. 3.30 and 3.31.

The effects of variation of the DC supply voltage, V_{cc}, are illustrated in Figs. 3.32 and 3.33. For these analyses an equivalent

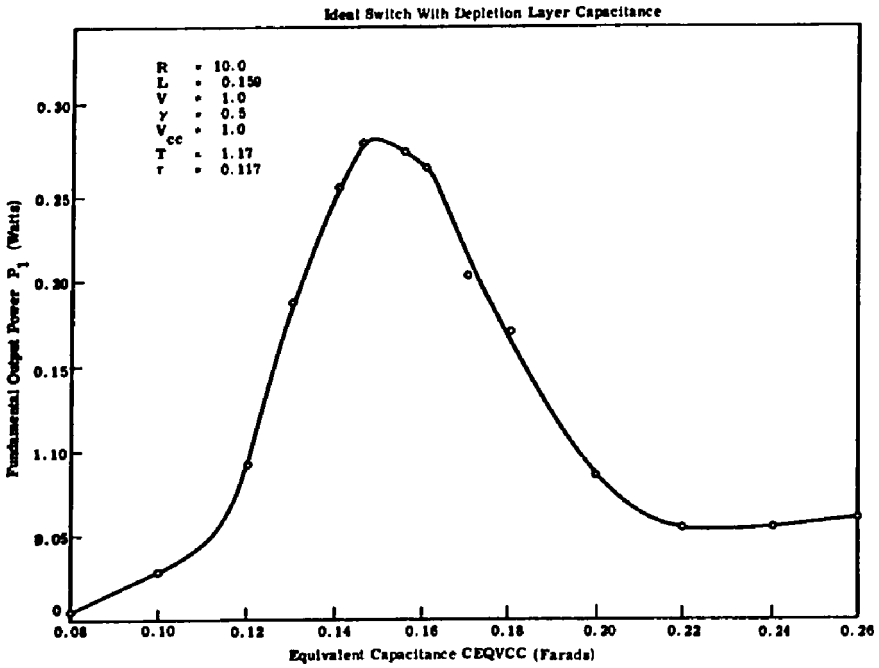


Fig. 3.21. Selection of nominal value for CEQVCC

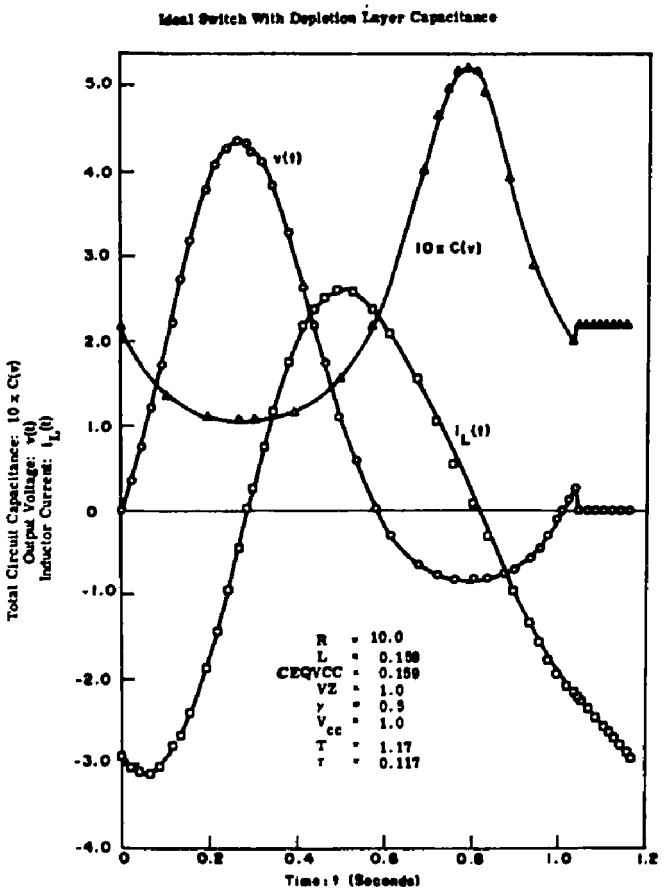


Fig. 3.22. Response of nonlinear circuit

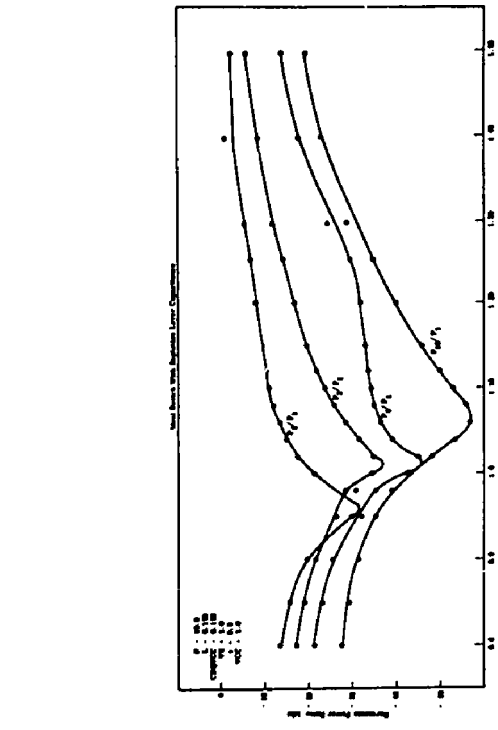


Fig. 3.24. Frequency behavior of harmonic content

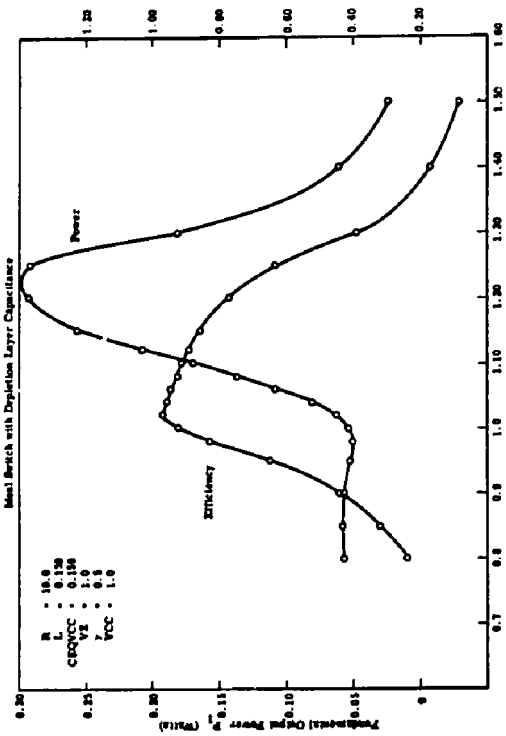


Fig. 3.23. Frequency response of output power and efficiency

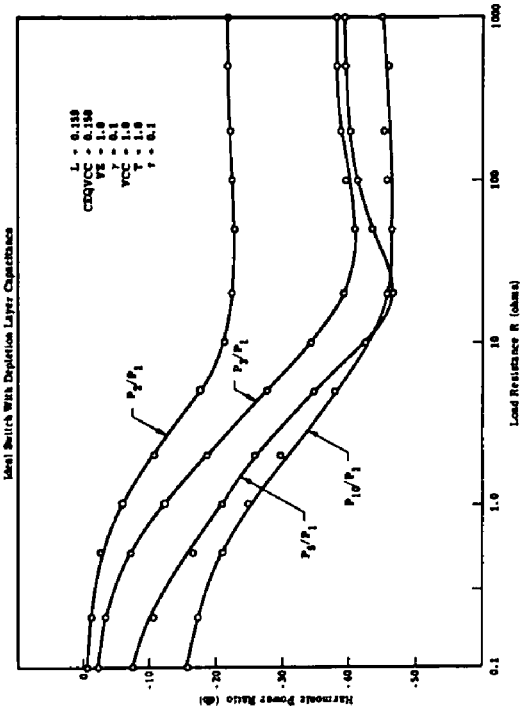


Fig. 3.26. Effect of load resistance on harmonic content

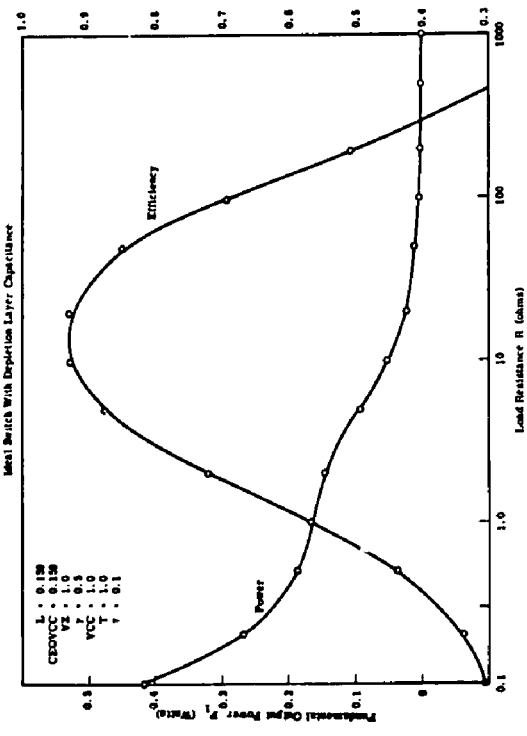


Fig. 3.25. Effect of load resistance on output power and efficiency

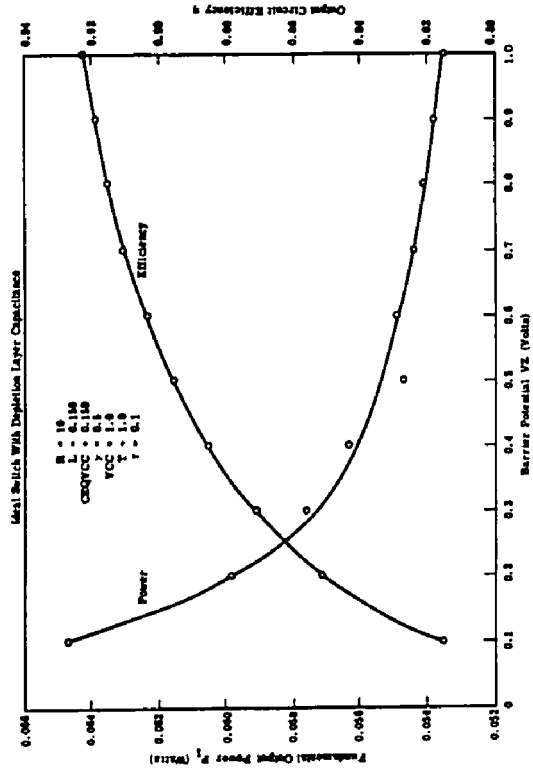


Fig. 3.28. Sensitivity of output power and efficiency to capacitance barrier potential

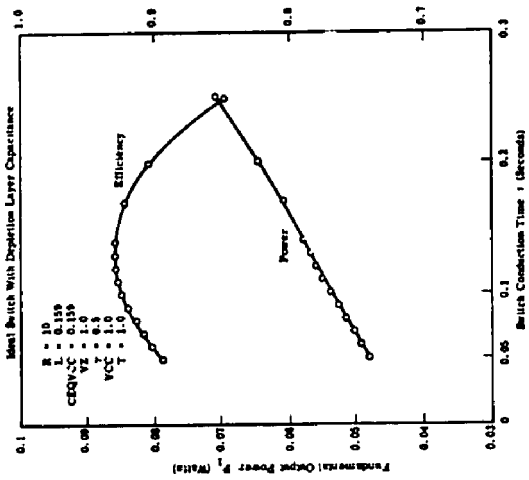


Fig. 3.27. Effect of conduction angle on output power and efficiency

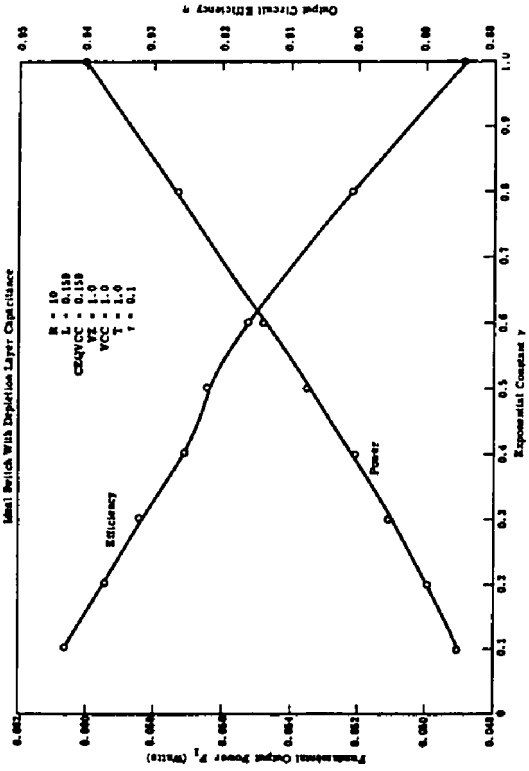


Fig. 3.29. Sensitivity of output power and efficiency to capacitance exponential constant

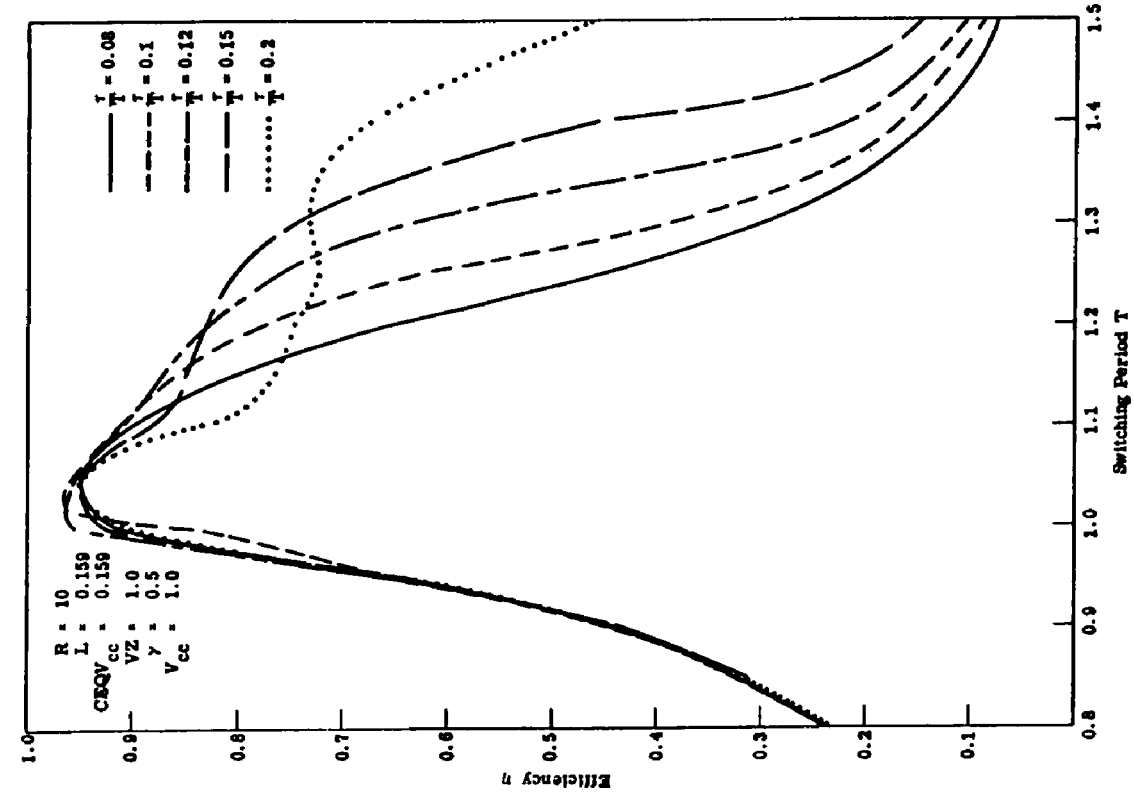


Fig. 3.31. Efficiency vs switching period

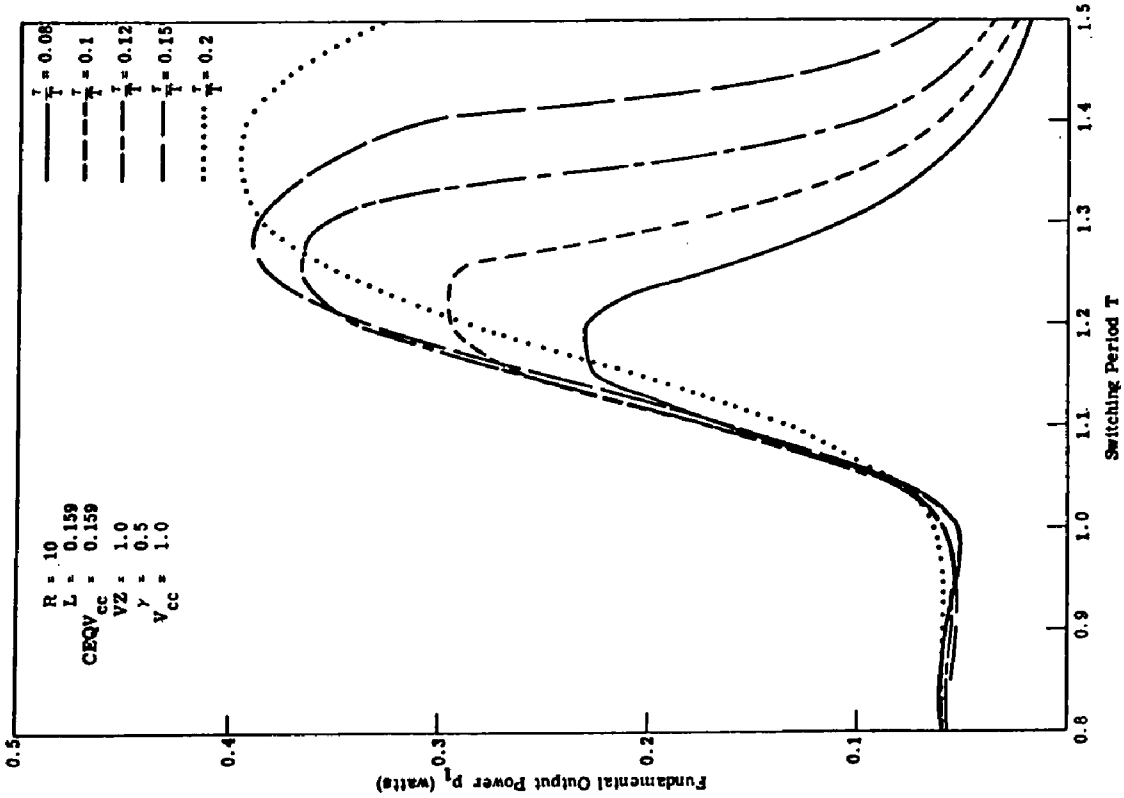


Fig. 3.30. Fundamental output power vs switching period

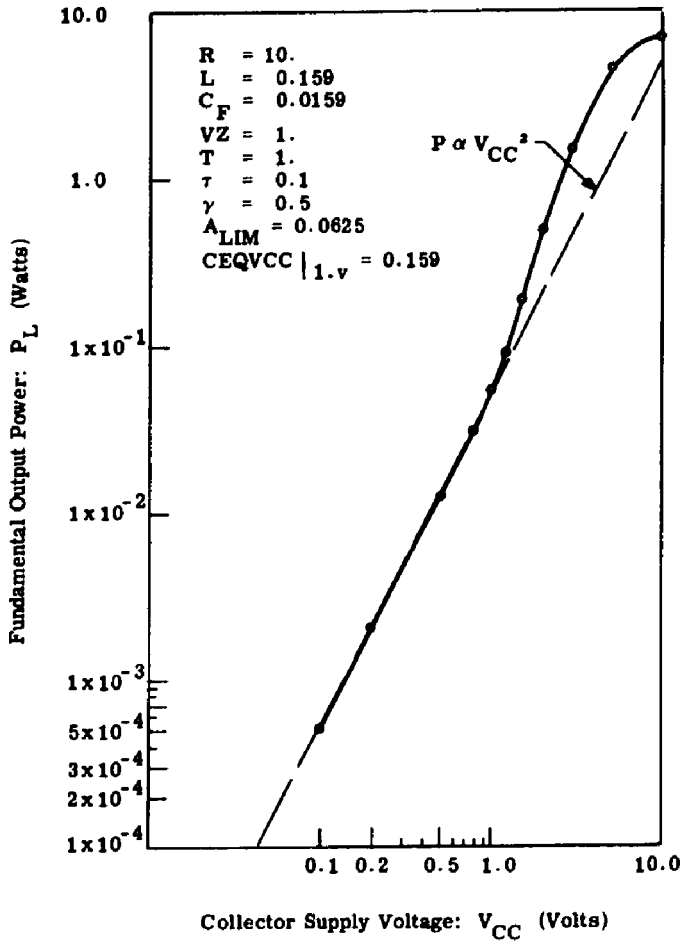


Fig. 3.32. Effect of supply voltage on output power

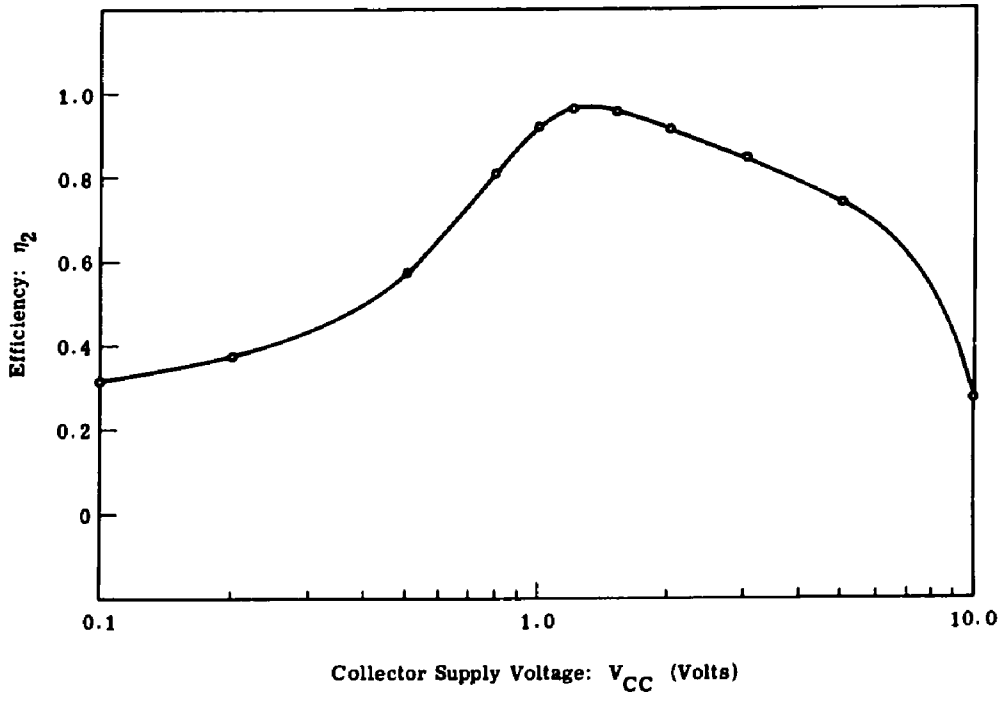


Fig. 3.33. Effect of supply voltage on efficiency

capacitance (Eq. 3.10) of 0.159 farad was chosen at a reference supply voltage of 1.0 volt. Increasing the supply voltage from this reference value reduces the "effective" circuit capacitance and increases the resonant frequency of the output circuit. As a result of this output tuning effect the output power can be found to increase more rapidly or more slowly than the square of the supply voltage. The variation in output power for this example (Fig. 3.32) indicates that the circuit is tuned slightly below the power resonance frequency when the supply voltage is 1.0 volt because the output power increases faster than the square of V_{cc} in the region of V_{cc} from 1.0 to 8.0 volts. With supply voltages greater than 8.0 volts the circuit seems to be tuned to a frequency higher than the excitation frequency, for in this region, the output power increases less rapidly than V_{cc}^2. This departure from square law variation in output power will be observed again in Section 6.5 where there are again regions of supply voltage in which the output power is not linearly related to V_{cc}^2.

The results of the analyses involving the voltage-sensitive depletion capacitance indicate that the circuit performance does not differ greatly from that obtained with the fixed capacitance analyses. The principle effect, for a circuit Q of approximately ten, is a reduction of the peak to peak output voltage with an attendant drop in the maximum values attained for power output and efficiency.

3.4 Series RL Tuning

The maximum efficiency, power output, and bandwidth obtainable with a specified transistor as a class C amplifier are dependent on the passive networks chosen for tuning at the amplifier input and output. These passive networks for tuning and matching the transistor output characteristics to the load are usually special forms of the classical LC ladder networks illustrated in Fig. 3.34. In addition to influencing the frequency behavior of the amplifier, these tuning networks also affect the large signal linear "equivalent" admittances (Section 1.2) of the transistor.

In this section, the effects of the output network configuration have been investigated by analyzing amplifier behavior with the tuning network of Fig. 3.34b. The actual circuit representation used for the analysis is shown in Fig. 3.35. In practical applications, dc-current flow through the load resistor is normally prevented by shunting the load with a large value inductor or by applying the supply voltage, V_{cc}, to another point in the circuit through a large value inductor. The iterative digital computation procedure used for this analysis allows us to dispense with the extra complexity introduced by such biasing inductors. To do this we introduce a variable battery in conjunction with the load resistor. This variable battery voltage is then adjusted automatically to compensate for the dc voltage drop and dc power loss in the load.

Typical voltage and current waveforms for the circuit for output

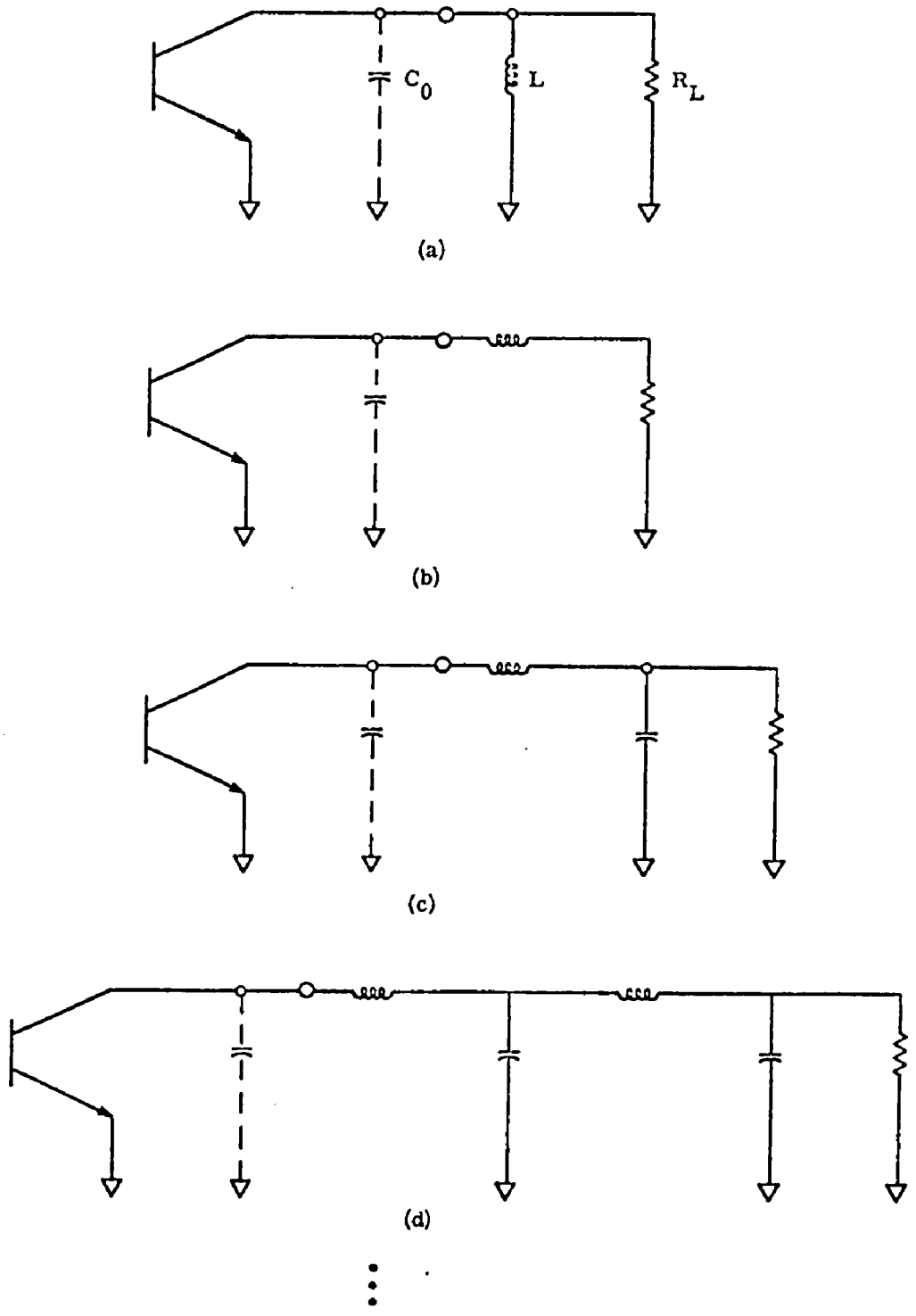


Fig. 3.34. Classical forms of output matching circuits

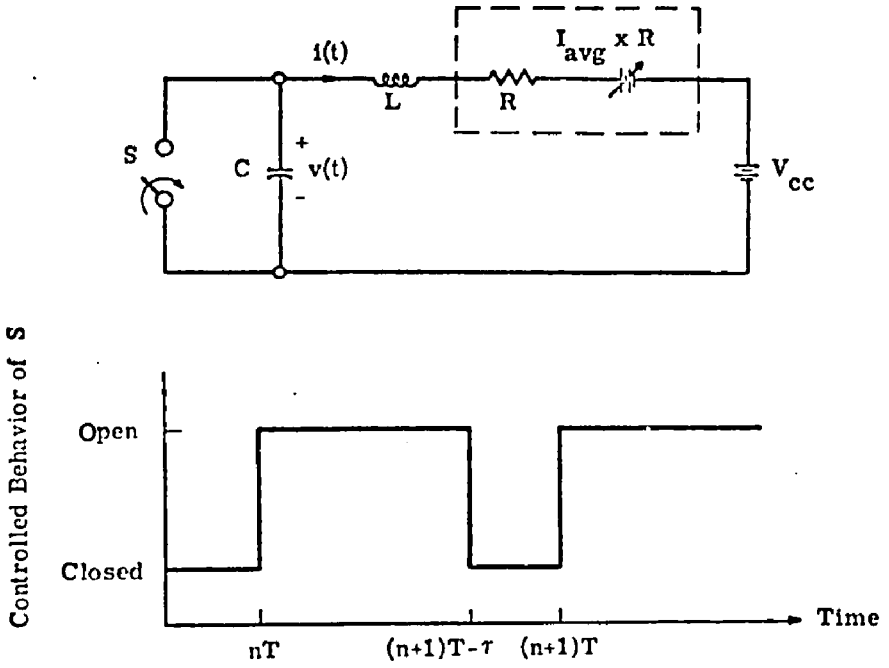


Fig. 3.35. Idealized output circuit

circuit Q's of ten and one are presented in Figs. 3.36 and 3.37, respectively. For the high Q case, the waveforms are essentially identical to those obtained in previous analyses with the parallel RLC output circuit of Fig. 3.1. The apparent advantage of the series RL configuration is that the shape of the load voltage is the same as the inductor current without the dc component. This current waveshape more closely approximates a sinusoid than does the capacitor voltage, and as a result, less harmonic power is dissipated with this series RL connection than with the parallel RLC connection. For low Q operation the waveforms for the two connections are not as similar,

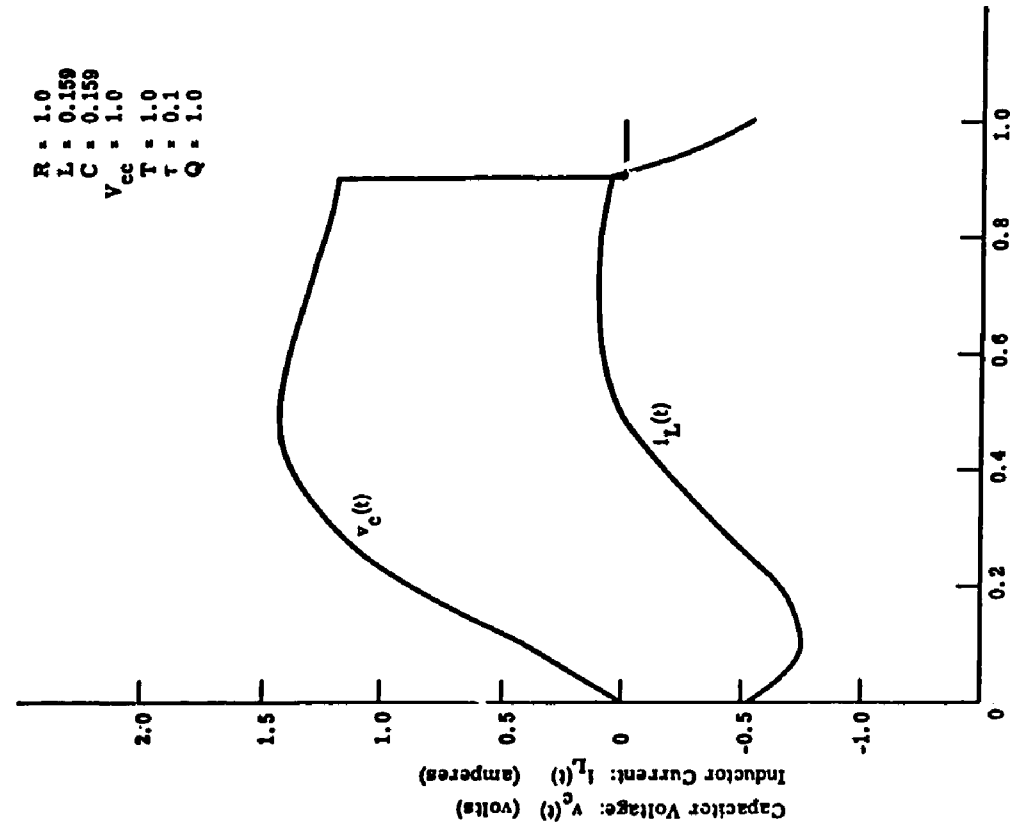


Fig. 3.37. Response of low Q circuit

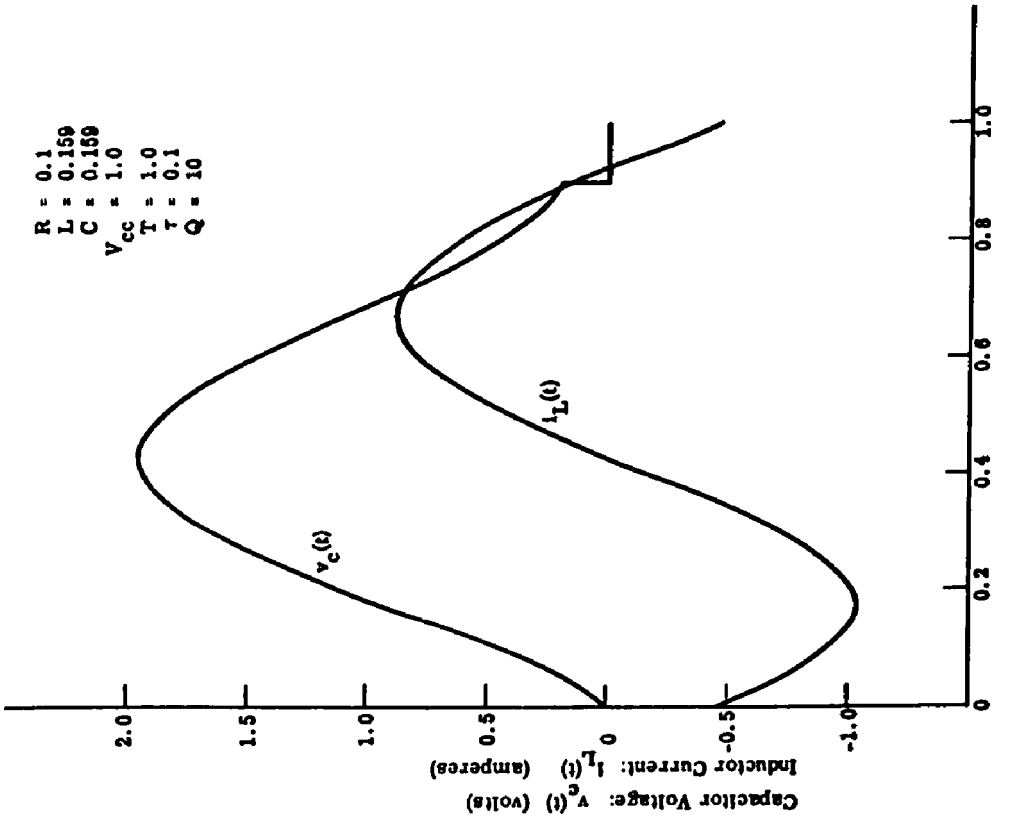


Fig. 3.36. Response of high Q circuit

but the peak values are approximately the same.

Figure 3.38 indicates the effects of the switching period on the fundamental output power and the conversion efficiency of the circuit with a Q of ten. The curve of output power has a peak of about 0.3 watts at a switching period of 1.17 seconds, and these values are practically the same as those observed for the parallel RLC tuning. However, there is a slight difference in the power bandwidths of the two tuning configurations. For this series RL case with $\tau/T = 0.1$, the half-power bandwidth is 0.173 Hz which is larger than the 0.145 Hz calculated for the parallel RLC output circuit (Fig. 3.4).

The efficiency of the series RL output circuit is very high (0.997) for switching periods from 1.02 to 1.05 seconds. The bandwidth for 80 percent efficiency is 0.163 Hz, and for 60 percent efficiency the bandwidth is 0.235 Hz. The overall shape, peak frequency, and bandwidth is very similar to the parallel RLC case, except for the latter case, the maximum obtainable efficiency is not quite as high (0.987).

The harmonic content in the load power varies with the switching period as shown in Fig. 3.39. Qualitatively these curves resemble those of Fig. 3.5 for the parallel RLC load, but these curves indicate a 5 to 10 dB reduction in harmonic output using the series RL output.

The fundamental output power and the efficiency depend on the equivalent load resistance (Fig. 3.40). This dependence has been analyzed by fixing the switching period to 1.0 second and the switching

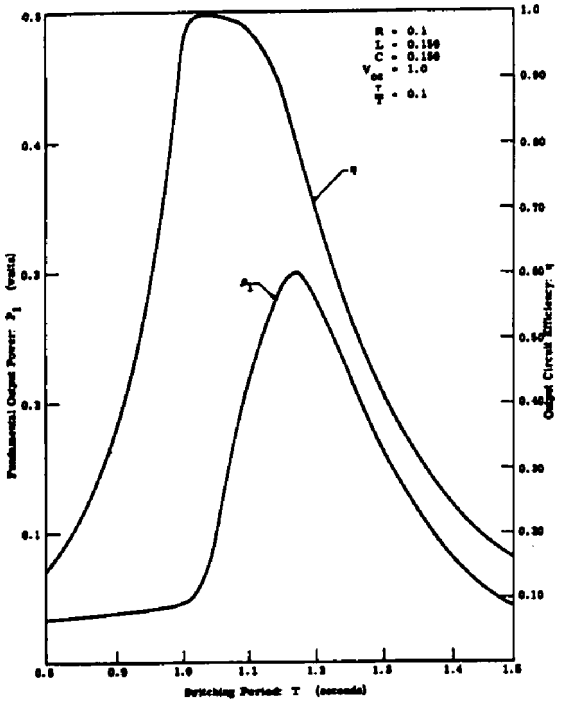


Fig. 3.38. Frequency response of output power and efficiency

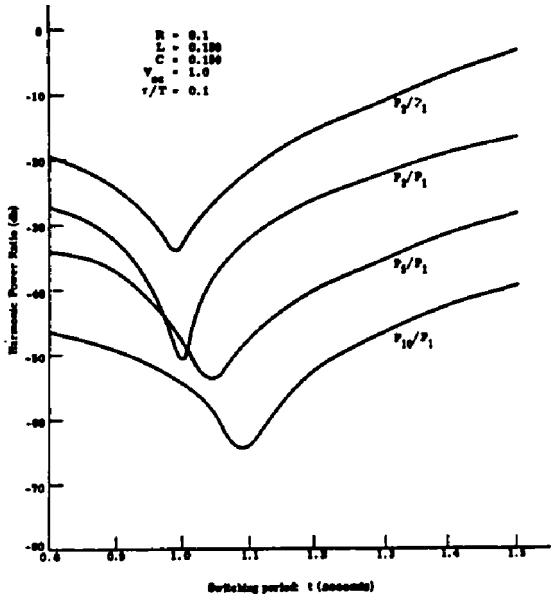


Fig. 3.39. Frequency behavior of harmonic content

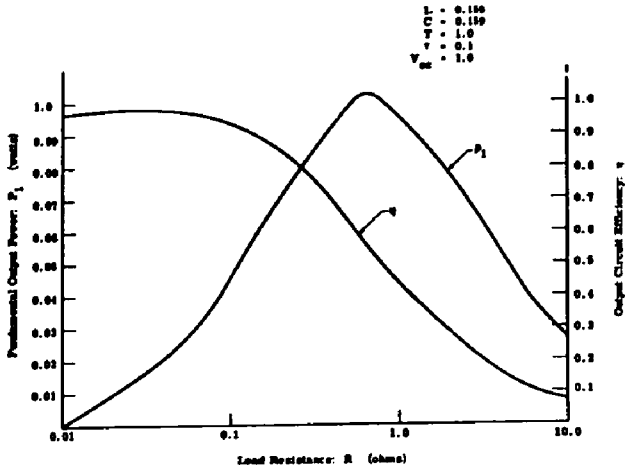


Fig. 3.40. Effect of load resistance on output power and efficiency

duty factor to 0.1 and then varying the load resistance over a wide range of values. When the circuit Q is high ($Q > 5$), the fundamental output power varies almost linearly with R. However, when the Q is low ($Q < 1$), the output power is seen to vary inversely with load resistance. This behavior is quite different from the behavior observed for the parallel circuit. With the parallel output circuit the output power was found to vary inversely to the load resistance in all Q ranges.

For the stated switching conditions, a maximum efficiency of 97 percent was obtained for series load resistances between 0.02 and 0.05 ohms. This is analogous to an efficiency of 98 percent that occurred for the parallel tuning when the load conductance was between 0.02 and 0.05 mhos.

From the numerical analyses we conclude that for a circuit Q often, the shift from parallel RLC output tuning to series RL tuning has little effect on circuit performance. However, for the low Q of unity, the series tuning circuit yields larger bandwidth, higher efficiency, and less harmonic content.

3.5 Harmonic Tuning

Before leaving the amplifier studies with ideal switch transistor representations, it is interesting to use this model to determine the potential utility of harmonic frequency tuning in a power amplifier output circuit to increase fundamental output power, gain and efficiency.

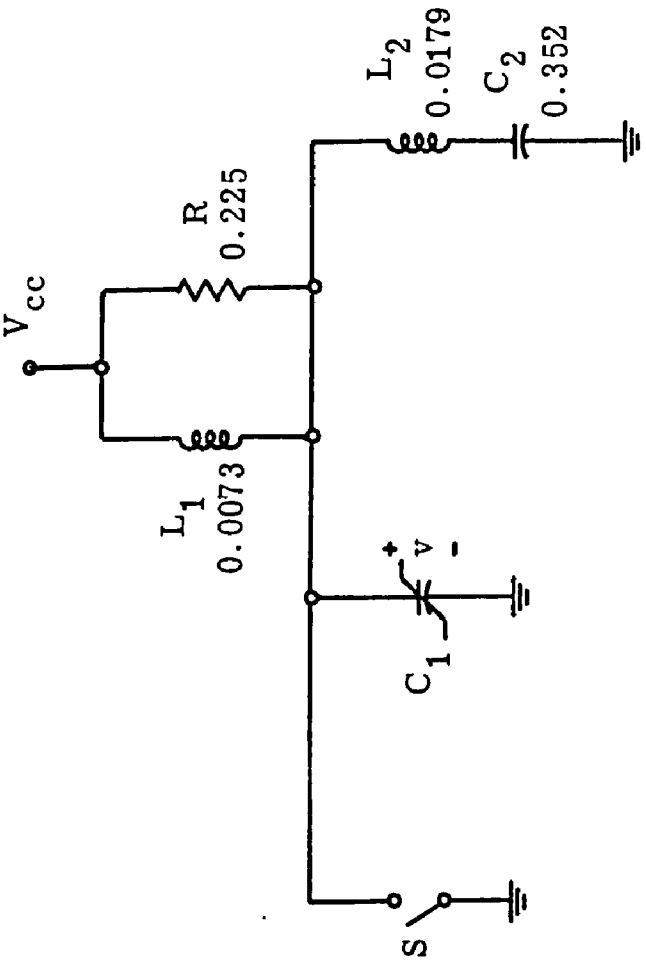
The output powers and efficiencies of class C amplifiers can often be increased by judicious treatment of the harmonic voltages and currents that exist in the output circuitry (Refs. H10, H11). The circuit representation of Fig. 3.41 was analyzed to provide an estimate of the utility of harmonic tuning. In this network, the series resonant trap can be adjusted to prevent the appearance of any one harmonic voltage component across the load. Reactive shorting of a harmonic component forces its energy into the fundamental and other harmonic components of the output voltage waveform.

A differential equation description of the network (state equations) during the time the switch is open is expressed by

$$\begin{bmatrix} C_1 & 0 & 0 & 0 \\ 0 & L_1 & 0 & 0 \\ 0 & 0 & C_2 & 0 \\ 0 & 0 & 0 & L_2 \end{bmatrix} \cdot \begin{bmatrix} \dot{v}_{C_1} \\ \dot{i}_{L_1} \\ \dot{v}_{C_2} \\ \dot{i}_{L_2} \end{bmatrix} = \begin{bmatrix} -\frac{1}{R_L} & -1 & 0 & -1 \\ 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 \\ 1 & 0 & -1 & 0 \end{bmatrix} \cdot \begin{bmatrix} v_{C_1} \\ i_{L_1} \\ v_{C_2} \\ i_{L_2} \end{bmatrix} + \begin{bmatrix} \frac{1}{R_L} \\ -1 \\ 0 \\ 0 \end{bmatrix} \cdot \begin{bmatrix} V_{cc} \end{bmatrix} \tag{3.11}$$

and during the time the switch is closed by

$$\begin{bmatrix} C_1 & 0 & 0 & 0 \\ 0 & L_1 & 0 & 0 \\ 0 & 0 & C_2 & 0 \\ 0 & 0 & 0 & L_2 \end{bmatrix} \cdot \begin{bmatrix} \dot{v}_{C_1} \\ \dot{i}_{L_1} \\ \dot{v}_{C_2} \\ \dot{i}_{L_2} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & -1 & 0 \end{bmatrix} \cdot \begin{bmatrix} v_{C_1} \\ i_{L_1} \\ v_{C_2} \\ i_{L_2} \end{bmatrix} + \begin{bmatrix} 0 \\ -1 \\ 0 \\ 0 \end{bmatrix} \cdot \begin{bmatrix} V_{cc} \end{bmatrix} \tag{3.12}$$



$$A = \text{Supremum} \left\{ \left\{ \frac{v + VZ}{A_{LIM}} \right\} \right\}$$

$$CEQVCC = C_1(v)\Big|_{v=V_{CC}} = 1.005$$

$$C_1(v) = \frac{C_J}{(A)^\gamma} + C_F$$

$C_J = 2.54$

$C_F = 0.17$ $\quad VZ = 0.5$

$A_{LIM} = 0.0625$

Fig. 3.41. Equivalent amplifier with harmonic tuning

The element values for the analysis for this circuit are indicated in Fig. 3.41. The effects of harmonic tuning on the output power, efficiency and frequency response (Figs. 3.42 and 3.43) were determined by numerical integration of Eqs. 3.11 and 3.12 until the steady state operation of the circuit was reached. The Fourier coefficients of the load voltage waveforms (Fig. 3.44) were then determined numerically to evaluate the fundamental components of the output power spectra. The plotted results demonstrate that this form of harmonic tuning can increase output power and efficiency, but the circuit behavior becomes much more sensitive to the excitation frequency as illustrated by the abrupt variations of output power and efficiency in Figs. 3.42 and 3.43 at a switching period of 1.6.

It may seem that for effective harmonic tuning the nonlinear capacitance element, C_1, is necessary to provide a parametric conversion of harmonic power to the lower fundamental frequency. This necessity of a nonlinear reactive element was investigated by replacing the nonlinear C_1 by a fixed capacitor (C_1 = 1.005 F, fixed). The results of this linear circuit analysis are also shown in Figs. 3.42 and 3.43, and they indicate that the nonlinear reactive element is not required in order to observe the effects of increased output power and efficiency. For example, we will find (Chapter 6) from analyses with the same circuit conditions and fixed switch capacitance but without harmonic tuning (Fig. 6.3), the maximum fundamental output power is 1.16 watts with an efficiency of 54 percent and a fractional

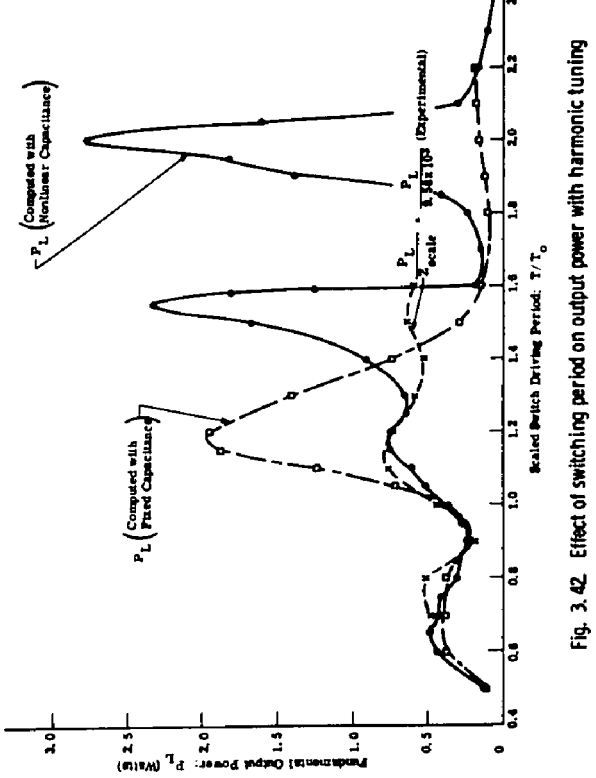


Fig. 3.42 Effect of switching period on output power with harmonic tuning

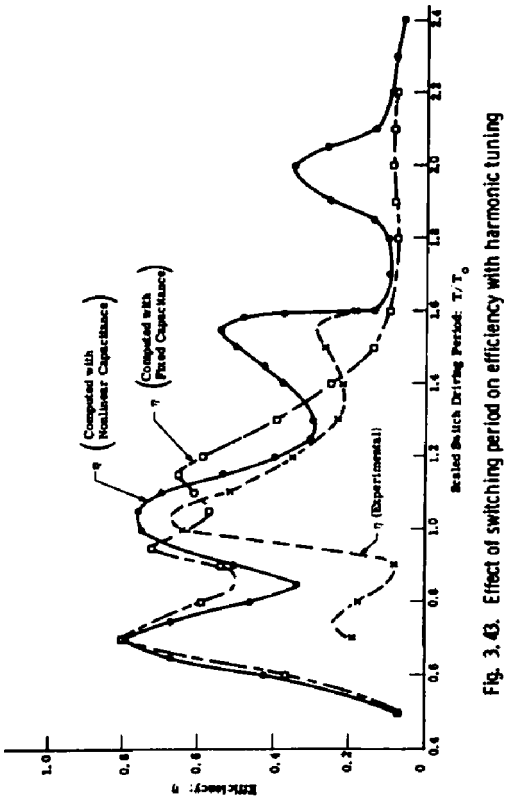
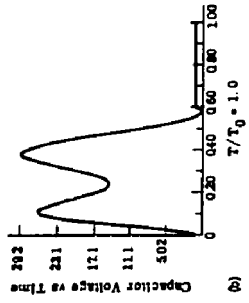
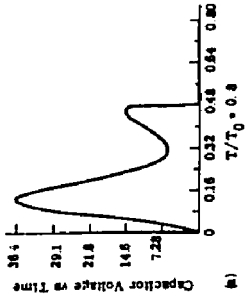


Fig. 3.43. Effect of switching period on efficiency with harmonic tuning





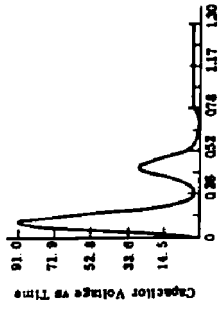


Fig. 3.44 Computed waveforms with harmonic tuning

power bandwidth of 45 percent (Figs. 6.12a and 6.13a). Addition of harmonic tuning increases the maximum output power to 2.01 watts and the efficiency to 62 percent but reduces the fractional power bandwidth to 22.4 percent.

Frequency scaling of the nonlinear harmonic tuning circuit by a factor of 5×10^5 and impedance scaling by 0.958×10^4 leads to the experimental circuit of Fig. 3.45 with an equivalent center frequency of 500 kHz. Waveforms from this experimental circuit (Fig. 3.46) are presented for conditions equivalent to those for the computed waveforms (Fig. 3.44). For further comparison, the experimental results were also presented in Figs. 3.42 and 3.43. The moderately good agreement between the experimental measurements and the computed results verifies the adequacy of the ideal switch representation for analysis of this low frequency, overdriven circuit.

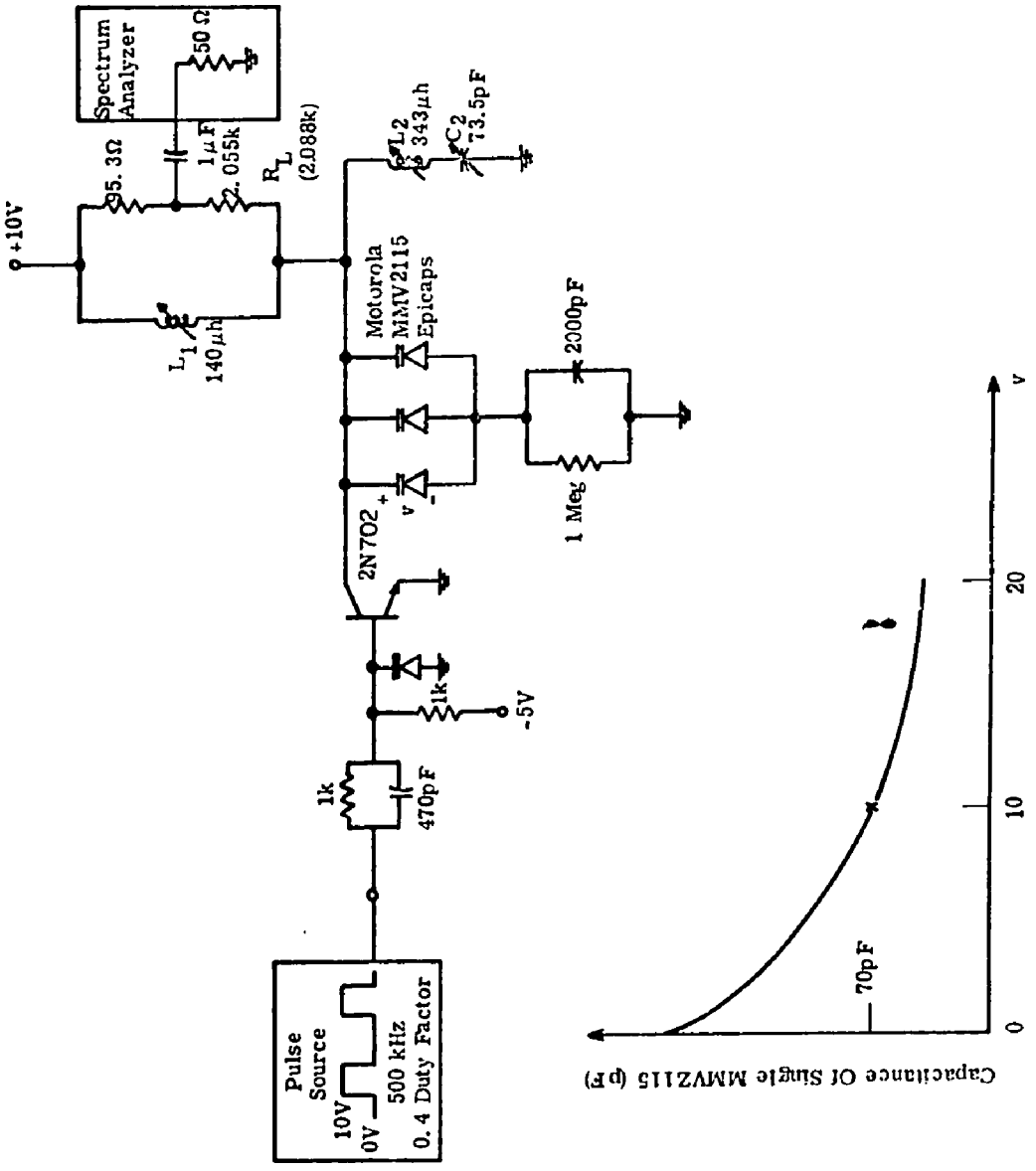
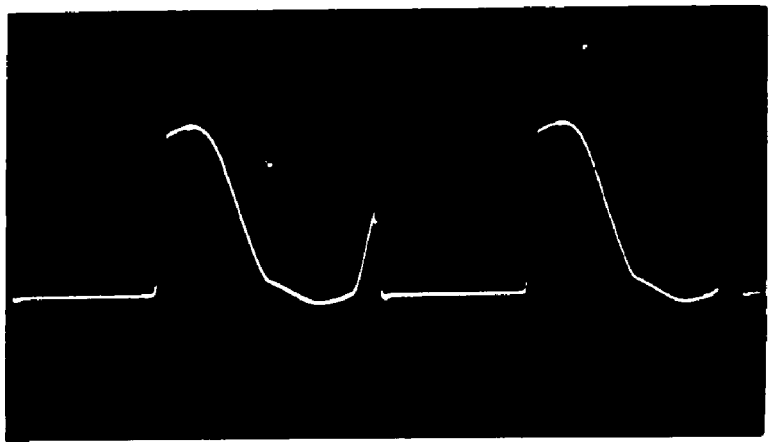


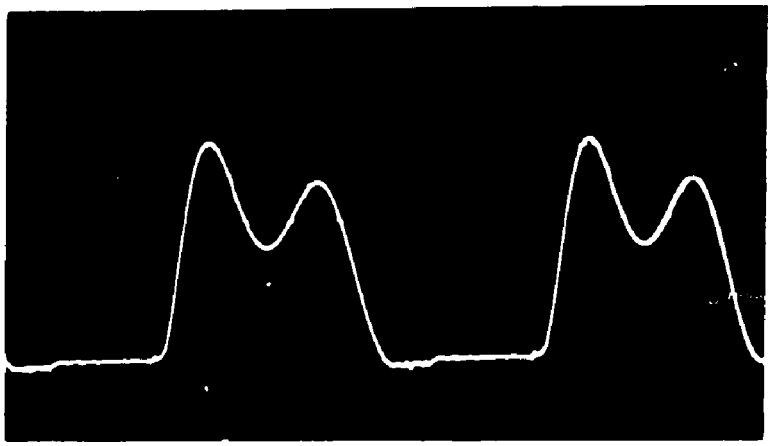
Fig. 3.45. Experimental amplifier with harmonic tuning



T/T_0 = .8

Vertical: 20 v/cm

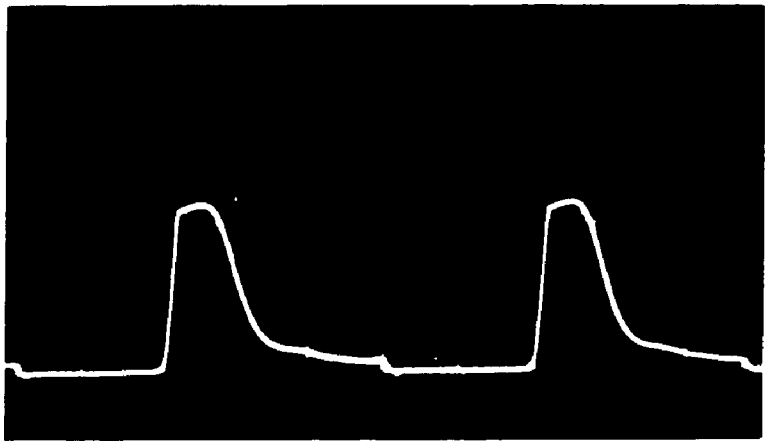
Horizontal: 2 μs/cm



T/T_0 = 1.

Vertical: 10 v/cm

Horizontal: 2 μs/cm



T/T_0 = 1.3

Vertical: 20 v/cm

Horizontal: 2 μs/cm

Fig. 3.46. Experimental collector-emitter voltage waveforms with harmonic tuning

CHAPTER 4

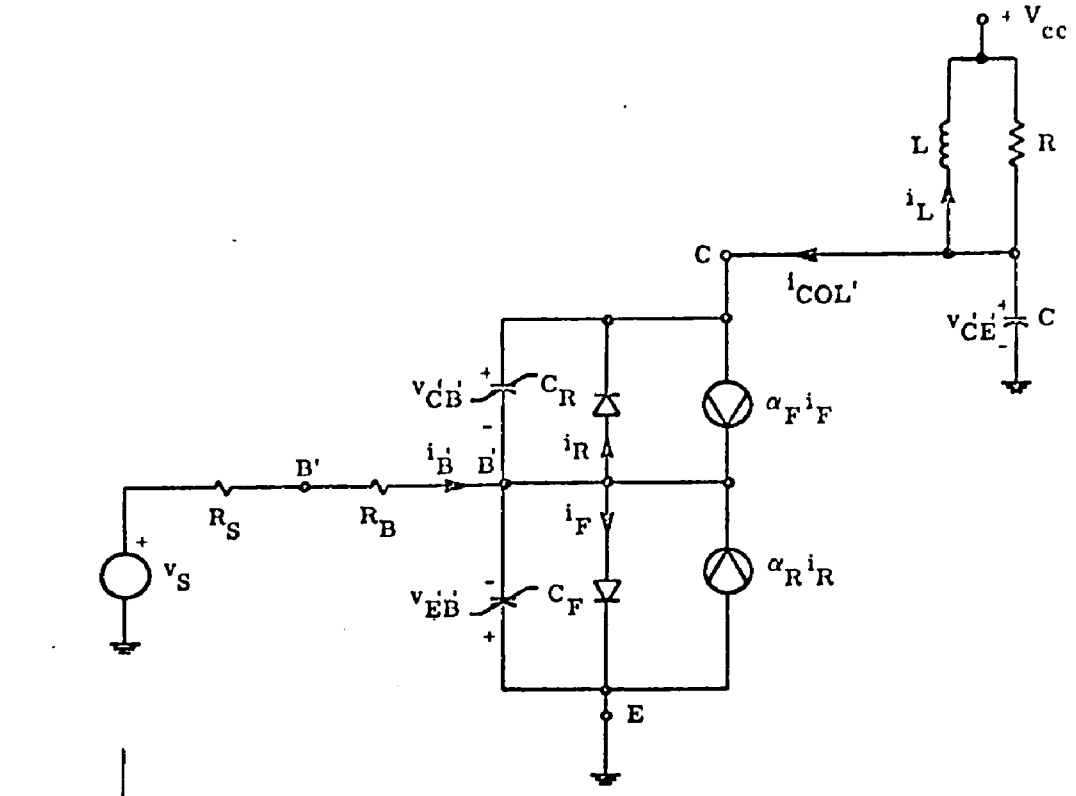
CLASS C AMPLIFIER ANALYSIS WITH INTRINSIC TRANSISTOR MODEL

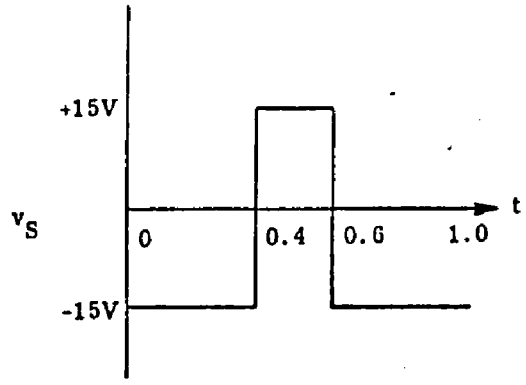
4.1 Introduction

The engineering value of the transistor models developed in the modeling chapter (Chapter 2) lies in their ability to predict the performance of high frequency power amplifiers. In this chapter the intrinsic transistor model (Section 2.4.3) is used to analyze two class C amplifiers. The first circuit is a low frequency amplifier with pulsed input excitation which causes the transistor to function very much like the controlled switch used in Chapter 3. The results computed numerically for this amplifier are verified with a low frequency (5 kHz) experimental amplifier. The second amplifier is studied under conditions of sinusoidal excitation at a frequency of 100 MHz. Comparisons between computed and experimental results for the 100 MHz amplifier indicate the need for extending the intrinsic transistor model to achieve improved simulation.

4.2 Computed Behavior of Low Frequency Amplifier

The amplifier circuit of Fig. 4.1 was chosen for initial analyses with the intrinsic voltage controlled transistor model. It is about the simplest possible class C transistor amplifier, since no tuning is employed in the base circuit and simple parallel tuning is employed





$V_{cc} = 10.0$ $\quad \tau_R = 0.159$

$R = 10.0$ $\quad Q_{FS} = 7.81 \times 10^{-10}$

$L = 0.159$ $\quad Q_{RS} = 1.56 \times 10^{-9}$

$C = 0.159$ $\quad \lambda = 39.5$

$R_S = 1.0$ $\quad C_{CDEP} = 0.01$

$R_B = 1.0$ $\quad C_{CDIFF} = \lambda Q_{RS} e^{-\lambda v_{CB'}}$

$\alpha_F = 0.98$ $\quad C_{EDEP} = 0.01$

$\alpha_R = 0.5$ $\quad C_{EDIFF} = \lambda Q_{FS} e^{-\lambda v_{EB'}}$

$C_R = C_{CDIFF} + C_{CDEP}$ $\quad \tau_F = 0.796$

$C_F = C_{EDIFF} + C_{EDEP}$

Fig. 4.1. Amplifier circuit with voltage-controlled model

for the collector. In addition to its simplicity, this configuration has been analyzed by others using analytic methods (Refs. H5, S2, S3, W1) and represents a realistic form of the ideal switch circuits analyzed numerically in Chapter 3. The transistor parameters were chosen to be representative of VHF transistors, but not specifically the 2N3866 because characterization of the 2N3866 had not been completed at the time of this analysis.

A state equation description for the amplifier circuit can be expressed as

$$\begin{bmatrix} -C_F-C_R & -C_R & 0 \\ C_R & C_R+C & 0 \\ 0 & 0 & L \end{bmatrix} \begin{bmatrix} \dot{v}_{E'B'} \\ \dot{v}_{C'E'} \\ \dot{i}_L \end{bmatrix} = \begin{bmatrix} \frac{1}{R_S} & 0 & 0 \\ 0 & -\frac{1}{R} & -1 \\ 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} v_{E'B'} \\ v_{C'E'} \\ i_L \end{bmatrix}$$

$$+ \begin{bmatrix} \alpha_F-1 & \alpha_R-1 \\ -\alpha_F & 1 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} i_F \\ i_R \end{bmatrix} + \begin{bmatrix} \frac{1}{R_S} & 0 \\ 0 & \frac{1}{R} \\ 0 & -1 \end{bmatrix} \begin{bmatrix} v_S \\ V_{cc} \end{bmatrix} \qquad (4.1)$$

with

$$i_F = \frac{Q_{FS}}{\alpha_F \tau_F} \left(e^{-\lambda v_{E'B'}} - 1 \right) \qquad (4.2)$$

$$i_R = \frac{Q_{RS}}{\alpha_R \tau_R} \left(e^{-\lambda(v_{E'B'} + v_{C'E'})} - 1 \right) \tag{4.3}$$

$$C_F = \lambda Q_{FS} e^{-\lambda v_{E'B'}} + C_{EDEP}(v_{E'B'}) \tag{4.4}$$

$$C_R = \alpha Q_{RS} e^{-\lambda (v_{E'B'} + v_{C'E'})} + C_{CDEP}(v_{E'B''}, v_{C'E'}) \tag{4.5}$$

The state variables chosen for this analysis are the emitter-base voltage, the output capacitor voltage, and the inductor current.

4.2.1 Numerical Difficulties With Voltage-Control Model.

Several different numerical methods were tried for integrating Eqs. 4.1. The basic difficulty encountered by all of the integration schemes was one of obtaining a suitable compromise between integration accuracy or stability and computation time. In this problem, the computation interval is relatively long; but at two times within the interval the state variables undergo rapid transitions which produce abrupt changes of the parameters dependent upon exponential functions. To preserve numerical stability during these rapid transitions, the integration step size of the independent variable must be reduced to a small value (Refs. C3, C2, G1). If this small step size is maintained constant for the entire integration interval, the computation becomes long and expensive. Therefore a requirement for a practical integration method is the capability of automatically adjusting the integration step size

as the computation progresses.

Selection or development of such an integration algorithm is not a trivial matter. When the calculation of the system derivatives is extensive, implicit integration routines seem to offer a minimum error-time product (Refs. R3, F2, G2). Two implicit numerical integration algorithms used with moderate success in this study are the Hamming predictor-corrector routine provided in the IBM Scientific Subroutine Package and a variable order integration scheme developed by Gear (Ref. G2). Stability and accuracy problems have been encountered with both algorithms when extreme network values were chosen, but these algorithms have been found to be adequate for realistic circuit descriptions.

In addition to the numerical problems associated with the integration of the state equations, there is some difficulty in determining the terminal currents, i_B' and i_{COL}', from the state variables and their derivatives. For example, there are two obvious ways to compute the collector current from the state variables $(v_{E'B'}, v_{C'E'})$ and their derivatives $(\dot{v}_{E'B'}, \dot{v}_{C'E'})$. One approach is to use Kirchhoff's current law to express i_{COL}' as a function of the currents within the transistor

$$i_{COL}' = \alpha_F i_F - i_R + (\dot{v}_{E'B'} + \dot{v}_{C'E'}) C_R \ ;$$

alternatively i_{COL}' can be expressed in terms of currents in the

passive external circuitry

$$i_{COL'} = -i_L - \frac{1}{R}(v_{C'E'} - V_{cc}) - C\dot{v}_{C'E'} \cdot$$

As long as the collector-base junction is reverse biased, the collector current is small in comparison to the relatively large currents in the high-Q collector tuning circuitry. As a result, the numerical errors accumulated in the computations of the external currents become quite significant in the subtractions employed in the second method. In this situation it has been found better to use the model equations directly to compute the collector current.

The other computational extreme is encountered when the transistor is saturated. At this time the collector current is of the same order of magnitude as the currents in the external circuitry, and the subtraction process poses no difficulty. However, in this forward bias situation, the collector current is very sensitive to the junction potentials (due to the sensitivity of the exponential functions in i_F, i_R, and C_F for positive exponents), and small errors in junction potential can produce very large errors in the computation of the collector current. Thus, the collector current should be computed from the external circuit constraints whenever the collector-base junction is forward biased.

4.2.2 Results of Computer Analysis With Voltage-Control Model. For the computer analysis of the circuit of Fig. 4.1, transistor

parameters were chosen to represent a device with a 2 GHz gain-bandwidth product, f_T, operating at a frequency of 1 GHz. The actual values indicated in the circuit resulted after the frequency was scaled down by 10^9 and the impedance level was reduced by a factor of 10. With this scaling, the values used in the output circuit (L, R, and C) are the same as those used in previous analyses with the ideal switch representations for the transistor. Typical waveforms of the periodic response of the amplifier are given in Fig. 4.2. The output voltage waveform $v_{C'E'}$ is very similar in shape to the output waveforms computed using ideal switch representations of the transistor's output characteristics (Chapter 3). Because of this similarity the analyses with variations in load resistance, supply voltage, driving frequency, etc., were not repeated for this amplifier.

The waveforms observed for $v_{E'B'}$ and $i_{B'}$ are what one would normally expect from such a circuit configuration; however, the double-peaked behavior of the collector current, $i_{COL'}$, was not anticipated and is not generally predicted by most class C analyses. In most analyses, the collector current is assumed to be rectangular or some smeared reproduction of the injected pulse of base current (Refs. S2, S3, W1). However, this analysis shows that the transistor saturates and the base current exerts no direct control on the collector current. With a moderately high-Q collector load, the reactive currents can cause the collector current to reduce sharply or even

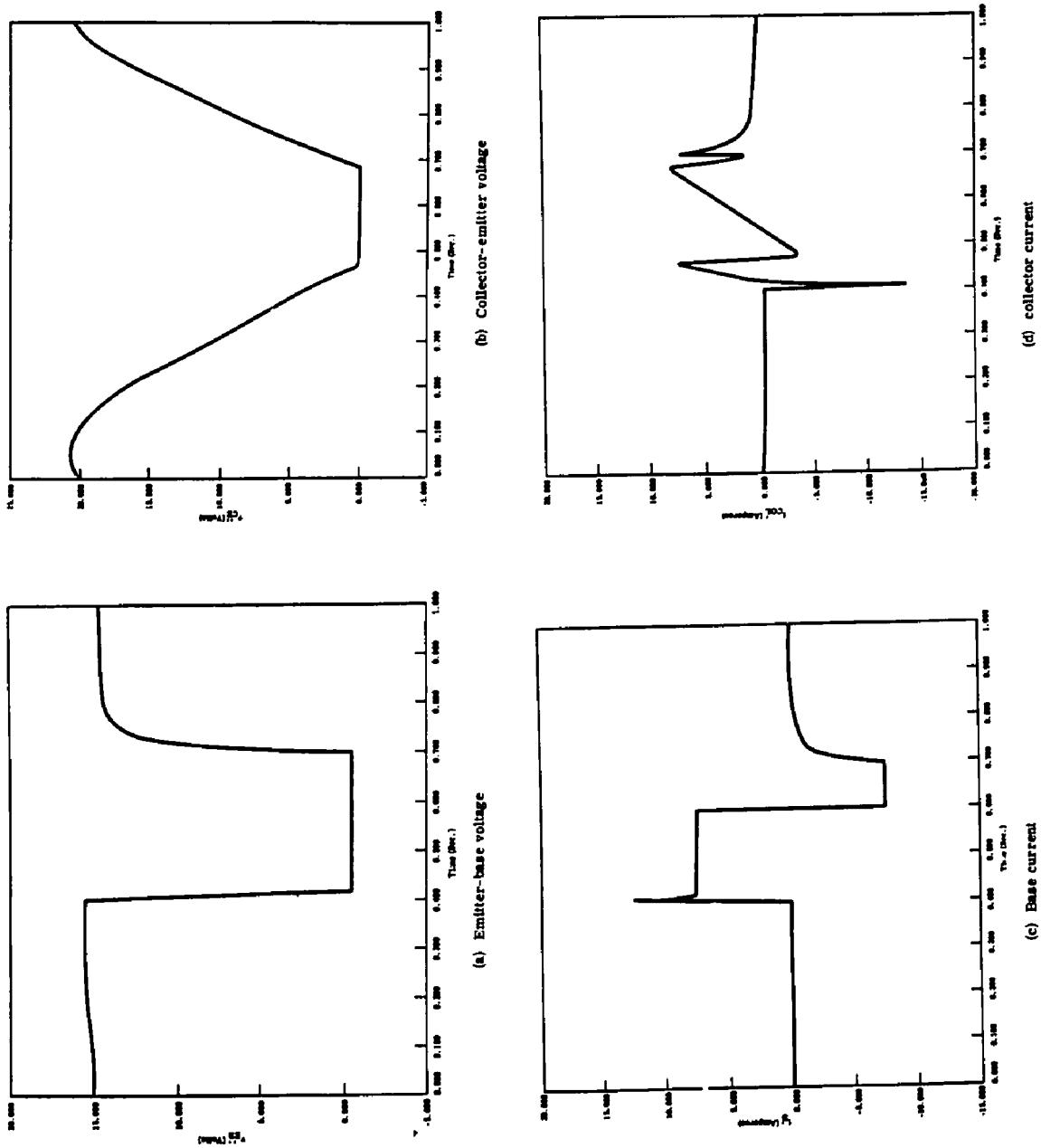


Fig. 4.2. Waveforms from amplifier analysis

reverse direction during the time that the transistor is in saturation.

4.3 Experimental Verification of Computer Analysis

The double-peaked collector current waveform has been observed experimentally with the low-frequency amplifier configuration shown in Fig. 4.3. Typical waveforms observed with this experimental circuit (Fig. 4.4) are much like those predicted by the computer analysis. The transistor used in the experimental circuit had a gain-bandwidth product that was much greater than twice the resonant frequency of the output circuit. To help adjust for this difference between the experimental circuit and the circuit used for the computer analysis, capacitances C_{CB} and C_{EB} were added in shunt with the transistor junctions. This is equivalent to increasing the depletion capacitance disproportionately with respect to the diffusion capacitance, but it does reduce the switching speed of the transistor and increase the switching transients observed in the base current waveform.

The main conclusion drawn from this experimental amplifier was that the complex collector current waveshape predicted by the numerical analysis with the intrinsic model (Fig. 4.2d) is reasonable. This level of verification is certainly not conclusive but does increase our confidence in the analysis methods employed.

4.4 Experimental 100 MHz Class C Amplifier

As stated before, the adequacy of a transistor circuit model

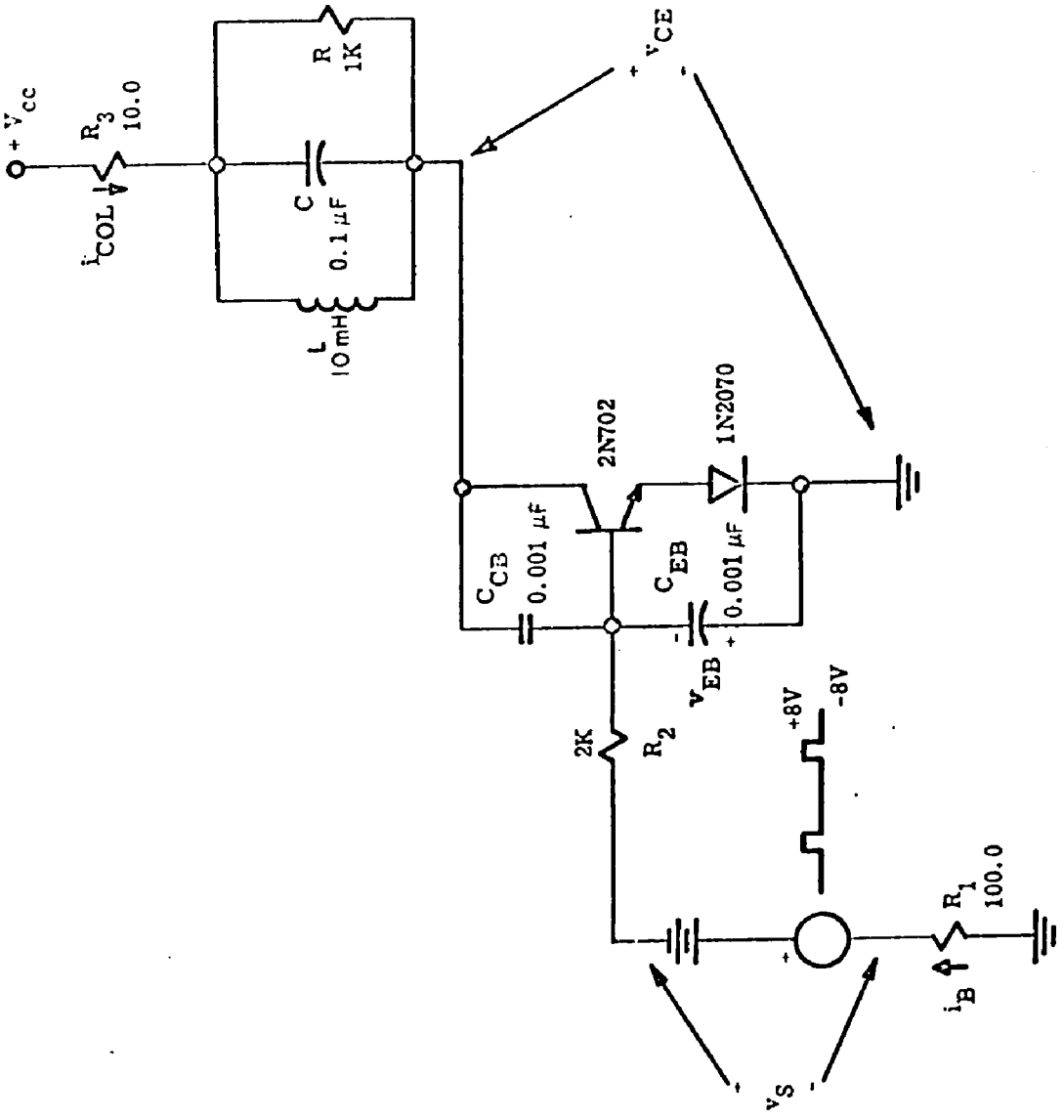


Fig. 4.3. Low-frequency amplifier

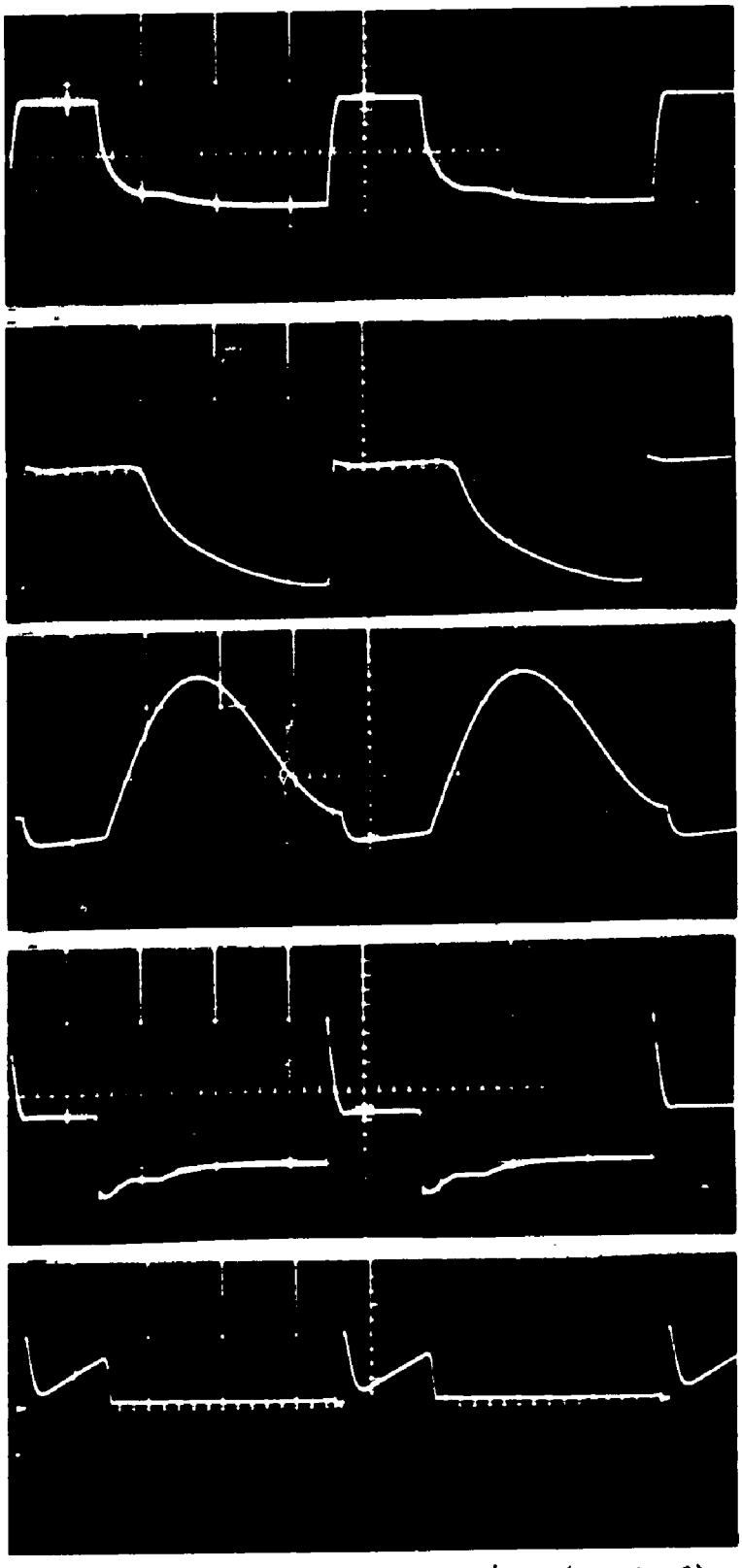


Fig. 4.4. Behavior of low-frequency amplifier

and associated computer analysis programs to predict high-frequency large-signal circuit behavior can be tested best by comparisons to experimentally observed amplifier behavior. The 100 MHz amplifier of Fig. 4.5 was constructed and measured to provide such a comparison base to be used with the simulation using the intrinsic transistor model (Fig. 2.12). The input circuit was not tuned or matched to the 2N3866 characteristics because, for this analysis, the main interest lay in the behavior of the collector circuit. Thus, the interactions and complexities introduced by base circuit tuning were not desired. The effects to be studied with this amplifier are those of collector supply voltage, load resistance, and input driving frequency. The nominal values used for this study are $V_{cc} = 10V$, $R_L = 225\,\Omega$, $f_0 = 100$ MHz as indicated in Fig. 4.5.

4.4.1 Effect of Collector Supply Voltage. From circuit analyses with ideal switch simulations (Chapter 3) we found that output power increases approximately as the square of the supply voltage, provided that the other circuit parameters remain fixed. At first glance, it may appear that this result is in contradiction to most analyses of class C amplifiers (Refs. S4, T1, R1) which predict linear increases in output power with supply voltage. This linear variation is predicted by low-frequency nonsaturated analysis of the collector circuit. viz (from Fig. 4.6)

$$P_{OUT} = \frac{(V_{cc} - V_{cesat})^2}{2R_L}$$

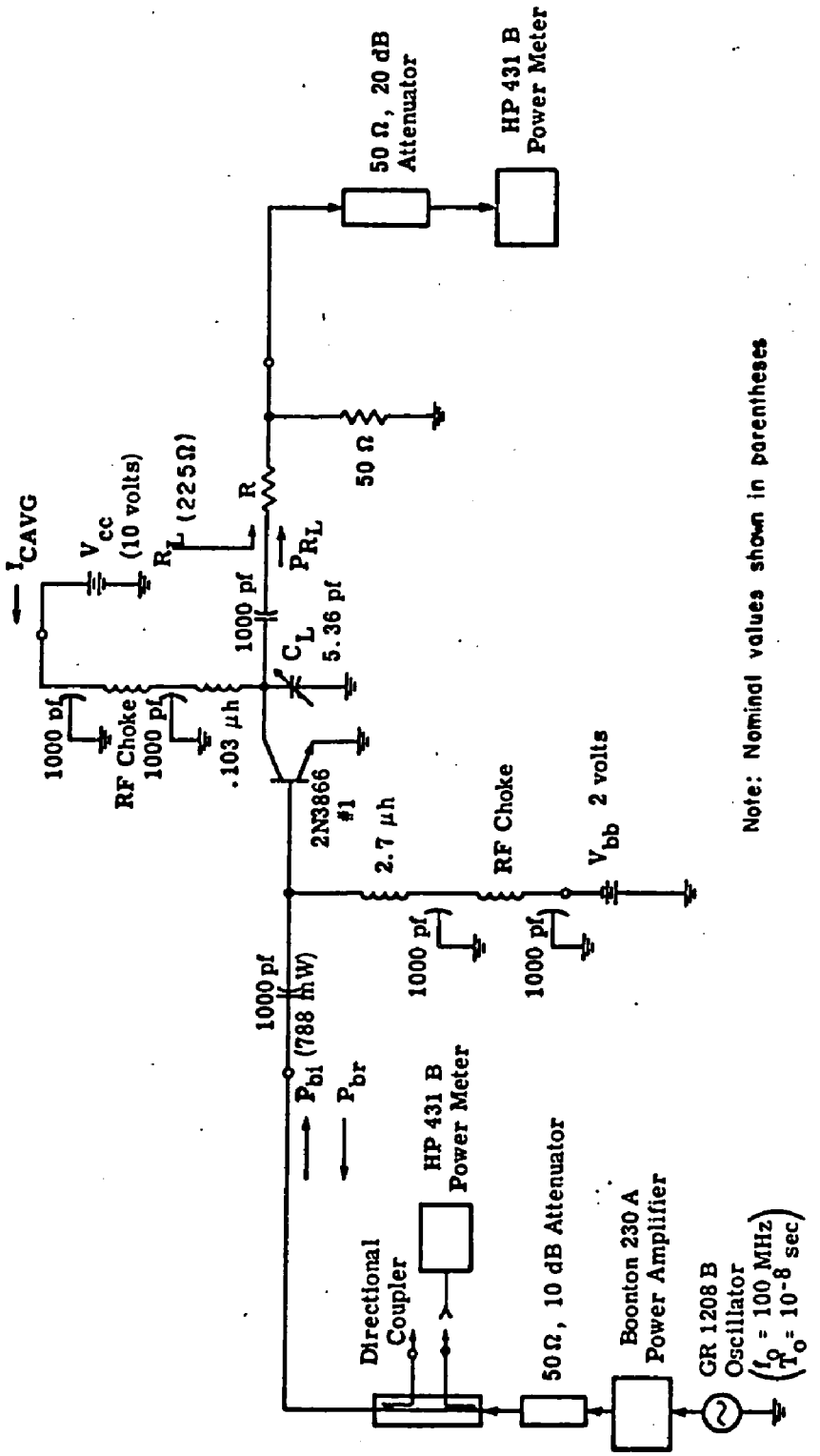


Fig. 4.5. Experimental amplifier and measurement circuitry

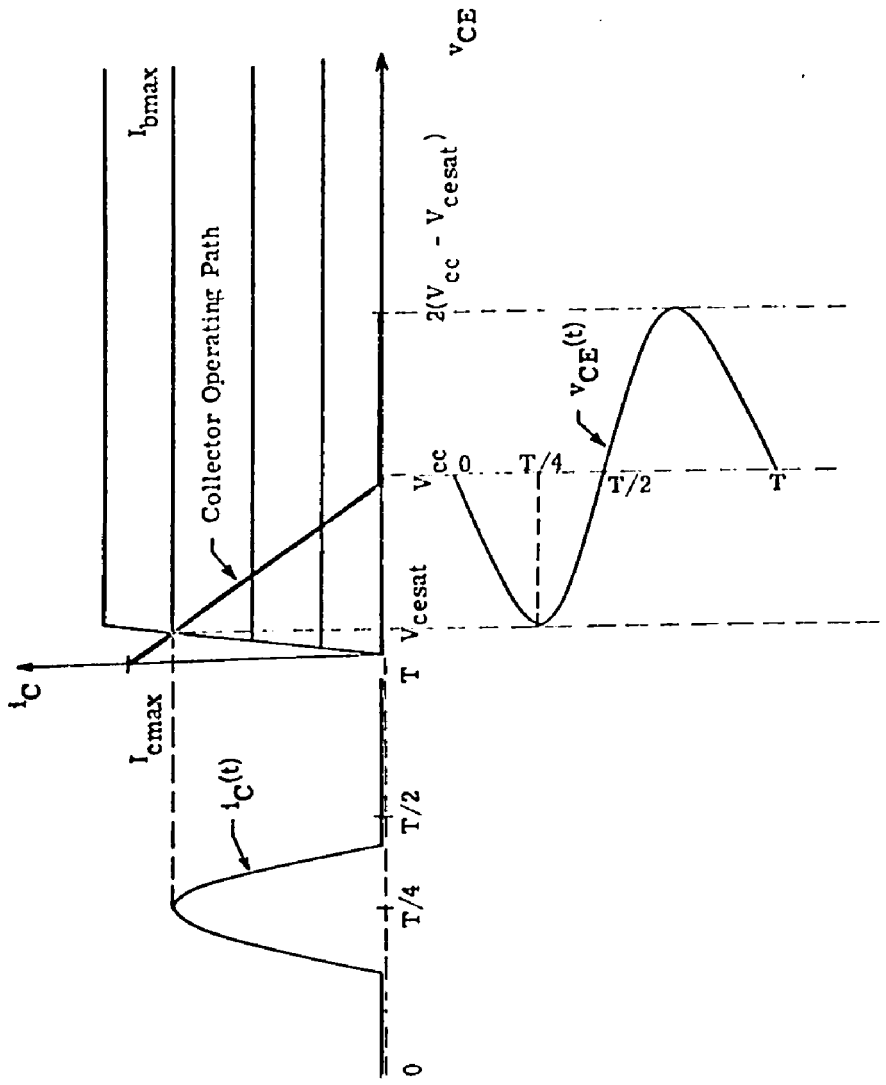


Fig. 4.6. Collector circuit behavior of low-frequency class C amplifier

$$I_{cmax} = \beta I_{bmax} \quad \text{(fixed by input drive)}$$

$$R_L \Big|_{\text{For Maximum } P_{OUT}} = \frac{V_{cc} - V_{cesat}}{I_{cmax}}$$

$$P_{OUT} = \frac{(V_{cc} - V_{cesat})\,\beta\, I_{bmax}}{2} \approx \frac{\beta\, I_{bmax}}{2} \cdot V_{cc}$$

Such analysis assumes that the load resistance, R_L, is increased correspondingly with increases in V_{cc}. However, if R_L is not readjusted with changes in V_{cc}, we can expect the output power to vary as $(1/2R_L) \cdot V_{cc}^2$ when the amplifier is driven into saturation and to remain relatively constant, $G \cdot P_{in}$, when V_{cc} becomes large enough to prevent saturation. This expected behavior was observed for the experimental amplifier (Fig. 4.7) except for very large V_{cc}. For these large supply voltages the output circuit apparently becomes detuned, causing the gain to decrease slightly as V_{cc} is increased. Figure 4.8 shows the corresponding variations in efficiency with supply voltage variations.

4.4.2 Effects of Load Resistance and Period of Driving Source.

The variations in output power and output circuit efficiency resulting from changes in load resistance are shown in Figs. 4.9 and 4.10. Figures 4.11 and 4.12 illustrate the frequency dependence of the amplifier. These results have no special significance in terms of desirable amplifier performance, but they do provide the required

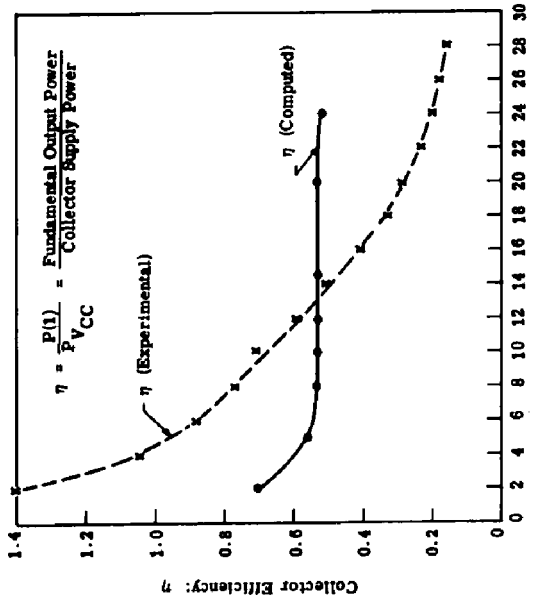


Fig. 4.8. Effect of collector supply voltage on efficiency

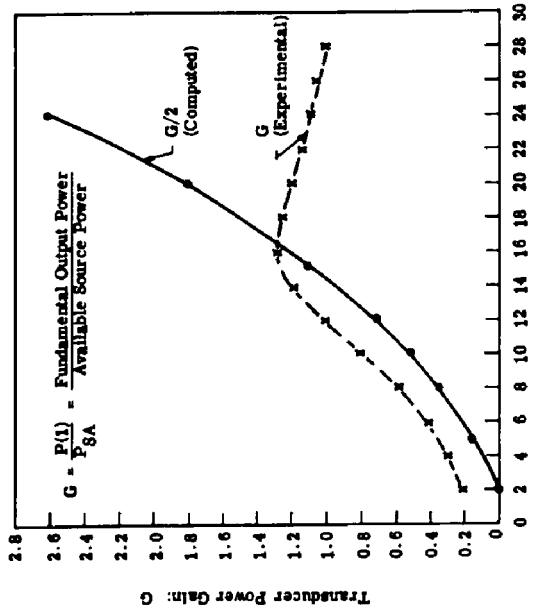


Fig. 4.7. Effect of collector supply voltage on gain

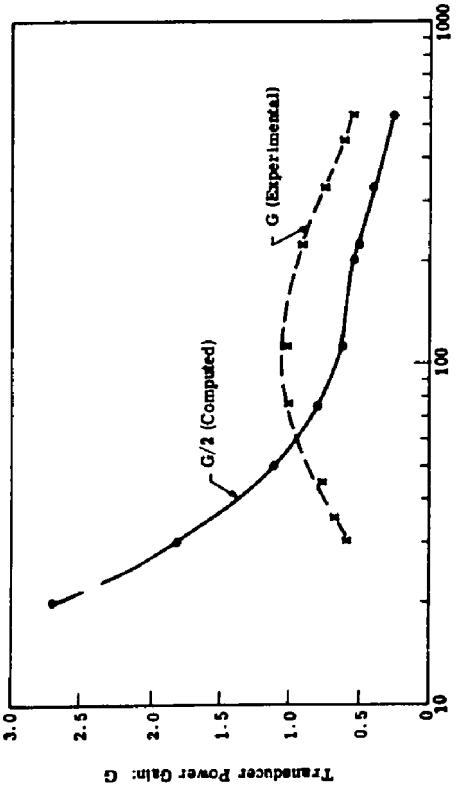


Fig. 4.9. Effect of load resistance on gain

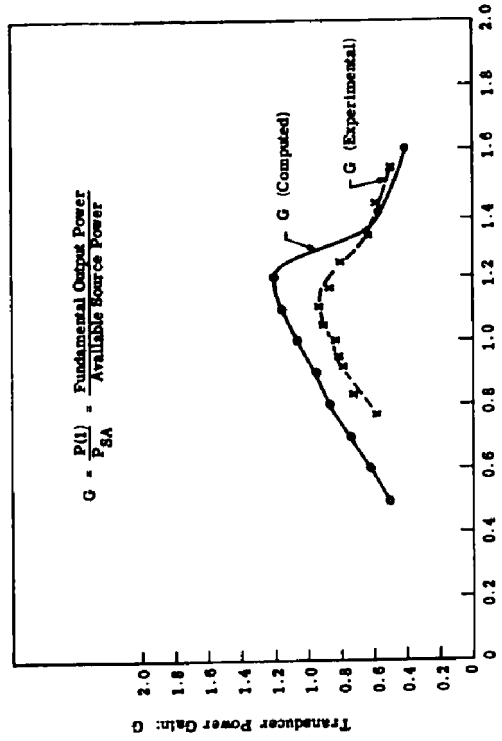


Fig. 4.11 Effect of driving period on gain

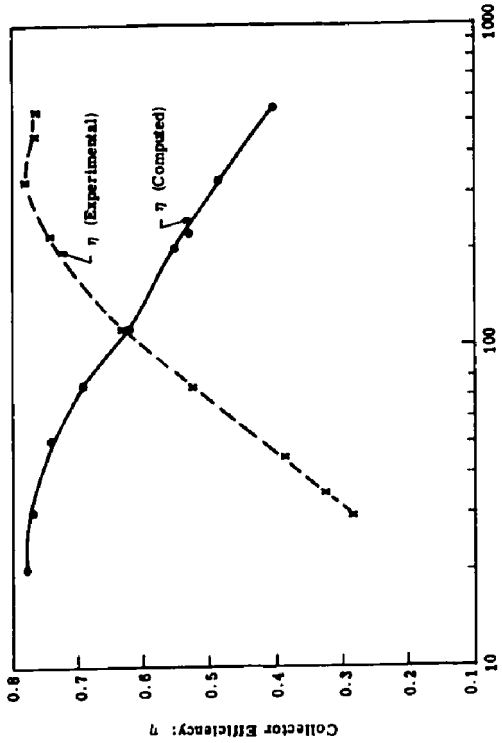


Fig. 4.10 Effect of load resistance on efficiency

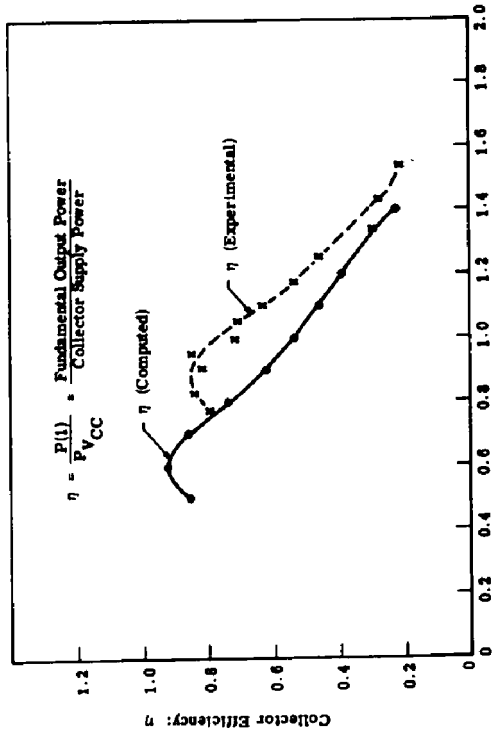


Fig. 4.12 Effect of driving period on efficiency

standard for comparison with the results predicted by computer-aided analyses.

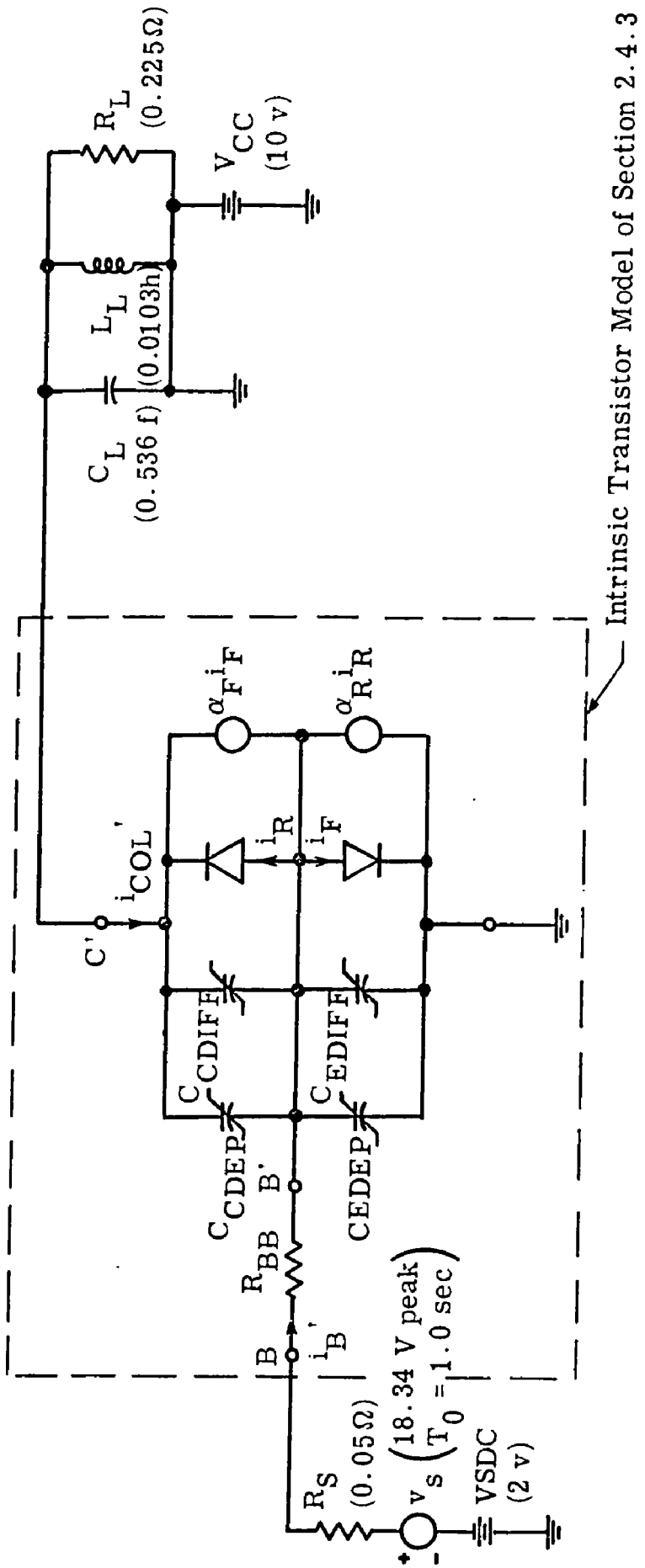
4.5 Computer Analysis of 100 MHz Class C Amplifier

The parameters obtained for the intrinsic model of the 2N3866 transistor were combined with a computer-analysis program to study the behavior of a class C amplifier with the same component values as used in the preceding experimental amplifier. The circuit equivalent to the experimental amplifier appears in Fig. 4.13. For numerical convenience the frequency has been scaled down by a factor of 10^8 and the current levels have been scaled up by 10^3. The transistor parameters for this simulation were chosen from Sections 2.3, 2.5.1.4, and 2.5.3.1. The depletion capacitances were assigned fixed values for the numerical analysis. The values chosen were selected from the capacitance characteristics (Figs. 2.16 and 2.17) at the average junction potentials, i.e.,

$$C_{EDEP} = C_{EDEP}(v_{E'B'}) \Big| \begin{array}{l} \approx 6.5 \text{ pf} \\ v_{E'B'} = \overline{v_{E'B'}} = \text{VSDC} = 2 \text{ v} \end{array}$$

$$C_{CDEP} = C_{CDEP}(v_{C'B'}) \Big| \begin{array}{l} \approx 2.3 \text{ pf} \\ v_{C'B'} = \overline{v_{C'B'}} = V_{CC} + \text{VSDC} = 12 \text{ v} \end{array}$$

The computed behavior of the amplifier is included with the experimental behavior in Figs. 4.7 through 4.12.



$$i_F = \frac{Q_{FS}}{\alpha_F \tau_F}\left(e^{-\lambda v_{E'B'}} - 1\right)$$

$$i_R = \frac{Q_{RS}}{\alpha_R \tau_R}\left(e^{-\lambda v_{C'B'}} - 1\right)$$

$$C_{EDIFF} = \lambda Q_{FS}\, e^{-\lambda v_{E'B'}}$$

$$C_{CDIFF} = \lambda Q_{RS}\, e^{-\lambda v_{C'B'}}$$

α_F = 0.988 $\quad Q_{FS}$ = 4.66×10^{-10} coul

α_R = 0.667 $\quad Q_{RS}$ = 1.16×10^{-7} coul

τ_F = 0.011 sec $\quad C_{EDEP}$ = 0.65 f (Fixed)

τ_R = 2.56 sec $\quad C_{CDEP}$ = 0.23 f (Fixed)

λ = 21.3 1/volt $\quad R_{BB}$ = 0.020 Ω

Fig. 4.13. Equivalent circuit for computer analysis

4.6 Comparisons and Conclusions

The intrinsic voltage controlled transistor model has been used in this chapter to study two tuned power amplifiers. The model was found to provide good simulation of a low frequency, pulsed input amplifier in which the transistor action is similar to an ideal switch. Complex base and collector circuit voltage and current waveforms were properly simulated by the model and analysis method as verified by measurements of an equivalent experimental amplifier.

A second amplifier employed a 2N3866 transistor at a frequency of 100 MHz. Comparison of the computed and experimental frequency response of the amplifier (Fig. 4.11) indicates that the maximum computed gain was approximately 30 percent greater than the experimentally measured gain. The maximum computed efficiency exceeded the experimental efficiency by only 8 percent, but the computed efficiency peak occurred at a higher frequency than determined experimentally (Fig. 4.12).

The measured gain of the 100 MHz amplifier increased approximately as V_{CC}^2 for $V_{CC} < 15$ volts, but leveled off for larger values of supply voltage (Fig. 4.7). Although slightly larger in value, the compute gain behaved similarly to the measured gain for the lower supply voltages. However, the computed gain continued to increase as V_{CC}^2 for large supply voltages, implying that the model used for the simulation was driven into saturation even at the high current levels

associated with the large supply voltages. The compute efficiency remains relatively constant for $V_{CC} > 6$ volts, but because the transistor in the experimental amplifier does not behave as a saturated switch at the larger supply voltages, the measured efficiency reduces as V_{CC} increases (Fig. 4.8).

The characteristics of the computed and measured gain variation with load resistance are approximately the same for $R_L > 100\,\Omega$ (Fig. 4.9). For smaller load resistances, the experimental gain is apparently reduced by transistor losses not simulated by the intrinsic model. In addition, the computed and measured efficiencies (Fig. 4.10) do not agree well at all. Improved description of the device losses seems necessary if the effects of load resistance are to be modeled properly.

We conclude that the intrinsic voltage controlled transistor model is adequate for many low frequency amplifier simulations that are limited to small ranges in circuit conditions, however, an improved model is desirable for better simulation of high frequency amplifiers subjected to large variations in circuit conditions. One might conjecture that the most essential additions to the model would be a collector resistance to account for losses with small load resistances and base and emitter impedances to limit the base drive current and prevent device saturation during conditions such as large collector supply voltage. Such additions are provided by the extended

transistor model (Section 2.5), and their effects are considered in the next chapter (Chapter 5). Further computations involving the intrinsic transistor model are presented in Chapter 6 for comparison with the other models.

CHAPTER 5

CLASS C AMPLIFIER ANALYSIS WITH EXTENDED TRANSISTOR MODEL

5.1 Introduction

The intrinsic transistor model was expanded in Chapter 2 to provide a more complete description of transistor behavior in high-frequency, large-signal applications. In this chapter the resulting extended transistor model is utilized to simulate numerically a VHF power amplifier. The amplifier simulated in this case employs simple tuning of both input and output. As in the study of the intrinsic model, experimental results are compared to the results of the digital computations.

The importance of each of the elements in the extended model has yet to be established. The question of the relative significance of each element of the model in predicting the overall behavior of a class C amplifier arises in the attempt to describe a transistor's high-frequency large-signal characteristics with a nonlinear dynamic circuit model. Using the VHF amplifier simulation, the sensitivities of several performance factors to variations in transistor model parameters and external circuit parameters have been computed to estimate the significance of each parameter. The sensitivities are presented

in this chapter and are useful for indicating the precision to which each circuit and model parameter value needs to be determined in order to accurately compute RF power amplifier behavior.

5.2 Experimental Amplifier

The experimental amplifier and measurement circuitry (Fig. 5.1) is very similar to that of Fig. 4.5. This amplifier is more representative of practical tuned power amplifiers in that the base input circuit is tuned as well as the collector output circuit. As with the previous amplifier analyses, our interest lies in determining the computational utility of the model to predict experimentally measured behavior. The experimental parameters chosen for a wide range of variation were the source driving frequency, the load resistance, and the collector supply voltage. The nominal values of these variable parameters were: f_0 = 100. MHz, R_L = 225. ohms, and V_{cc} = 10. volts, respectively. The experimentally observed performance of this amplifier is given in Figs. 5.2 through 5.14.

5.3 Amplifier Analysis with Extended Transistor Model

An equivalent circuit representation for the amplifier with the extended transistor model is shown in Fig. 5.15. For this equivalent circuit, the element values have been scaled to reduce the frequency by 10^8 and to increase the current by 10^3. A dynamic description of the resulting seventh order nonlinear system is given by the following

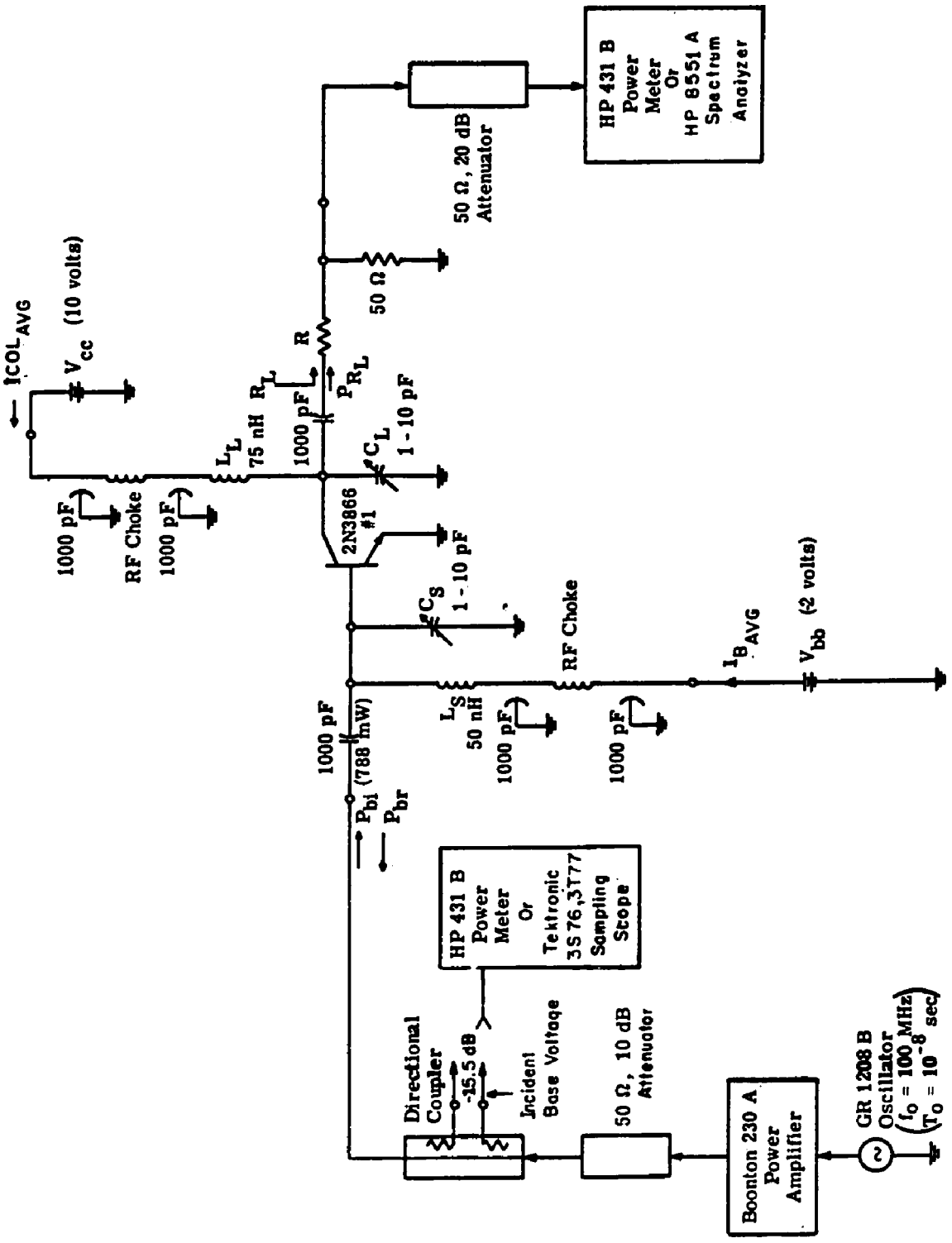


Fig. 5.1. Experimental amplifier and measurement circuit



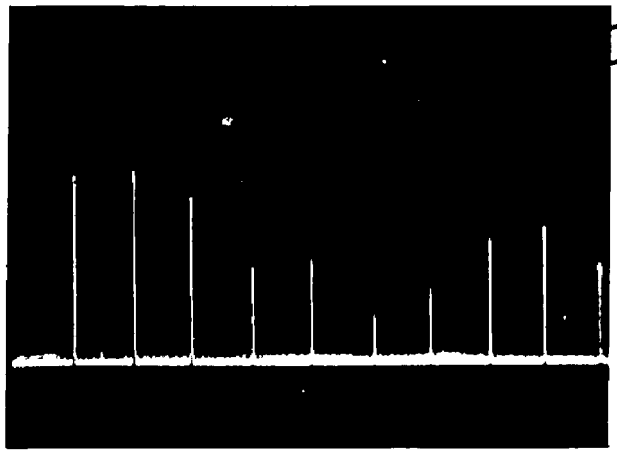
Incident Base Voltage
(-15.5Db) 0.5 v/cm

Total Base Voltage
Vertical: 5 v/cm
Horizontal: 2 ns/cm



Incident Base Voltage (-15.5Db)
0.5 v/cm

Collector Voltage
Vertical: 10 v/cm
Horizontal: 2 ns/cm



100 MHz
200 MHz

Load Power Spectrum
Vertical: 10 dB/cm
Horizontal: 100 MHz/cm

Fig. 5.2. Waveforms for 100-MHz experimental amplifier

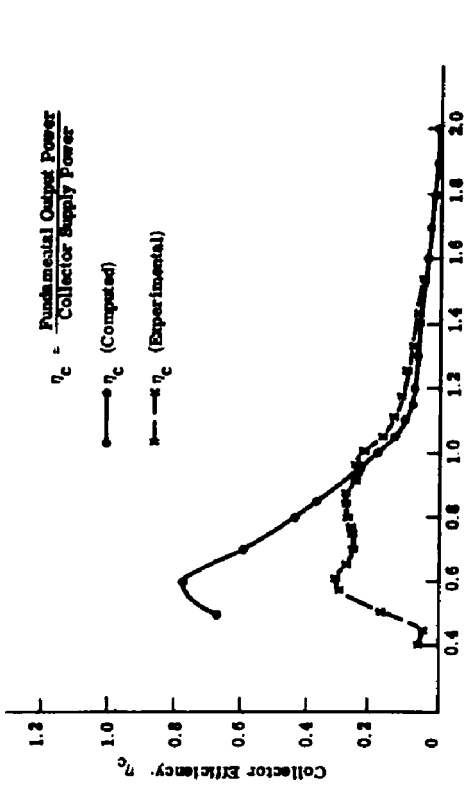


Fig. 5.4. Effect of driving period on efficiency

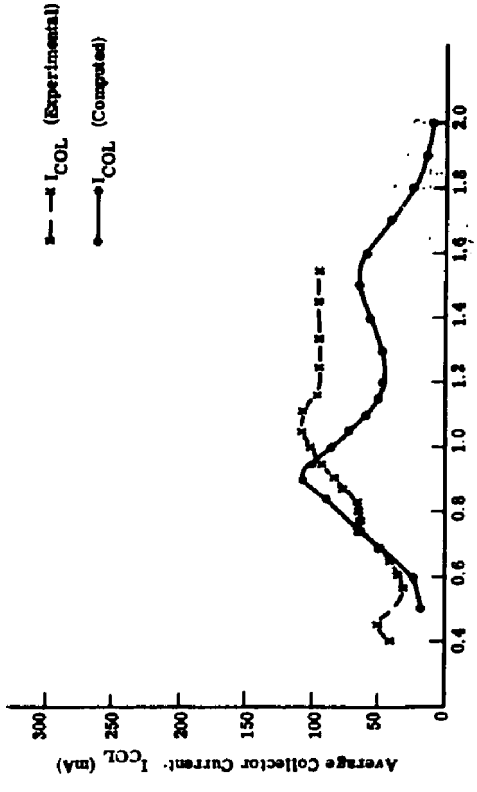


Fig. 5.6. Effect of driving period on collector current

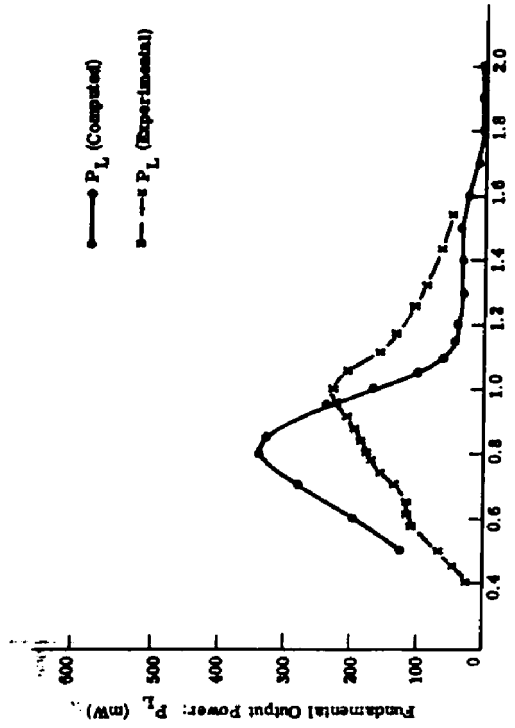


Fig. 5.3. Effect of driving period on output power

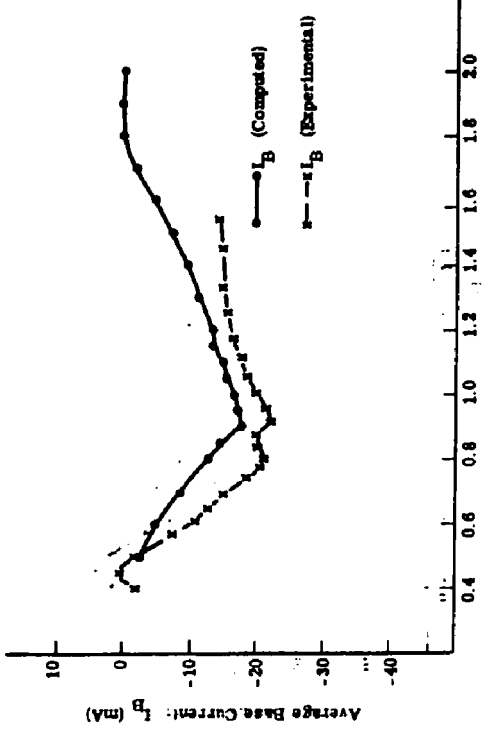


Fig. 5.5. Effect of driving period on base current

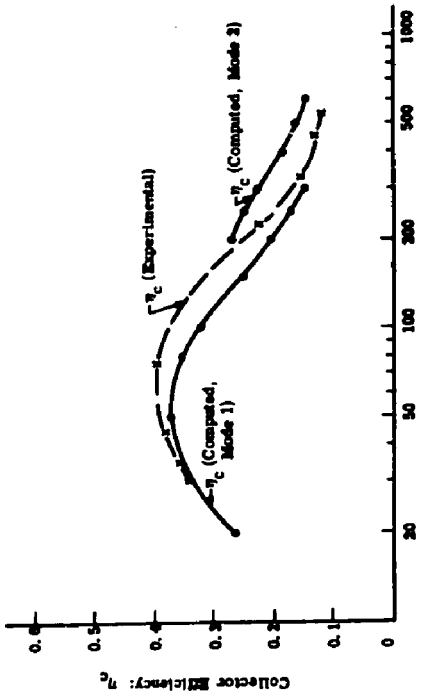


Fig. 5.8. Effect of load resistance on efficiency

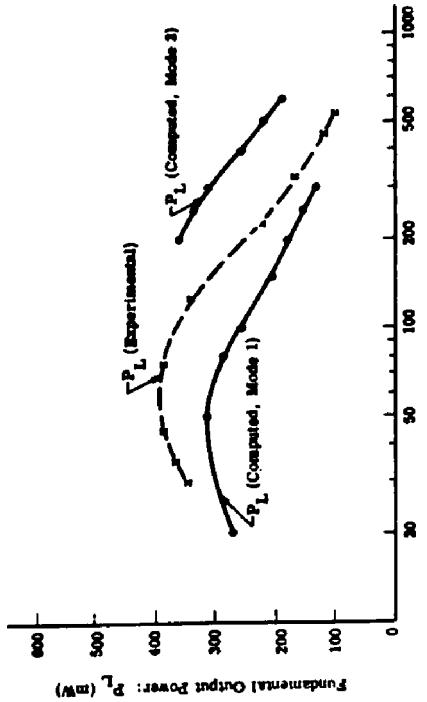


Fig. 5.7. Effect of load resistance on output power

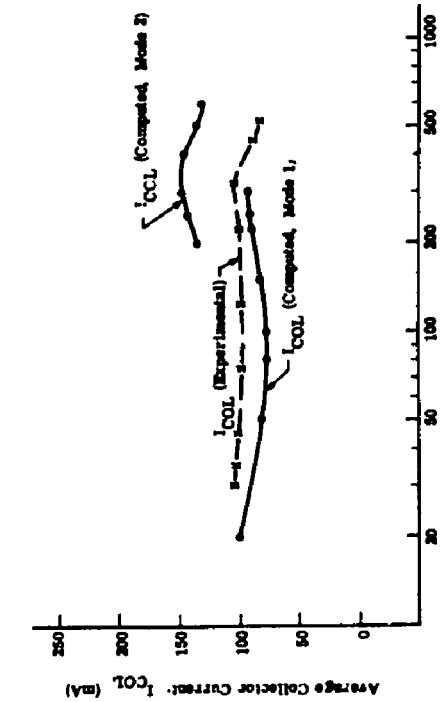


Fig. 5.10. Effect of load resistance on collector current



Fig. 5.9. Effect of load resistance on base current

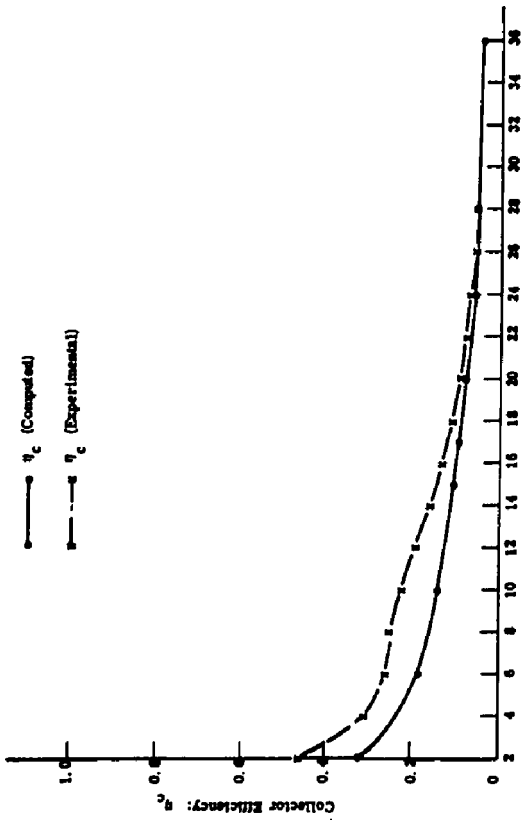


Fig. 5.12 Effect of supply voltage on efficiency

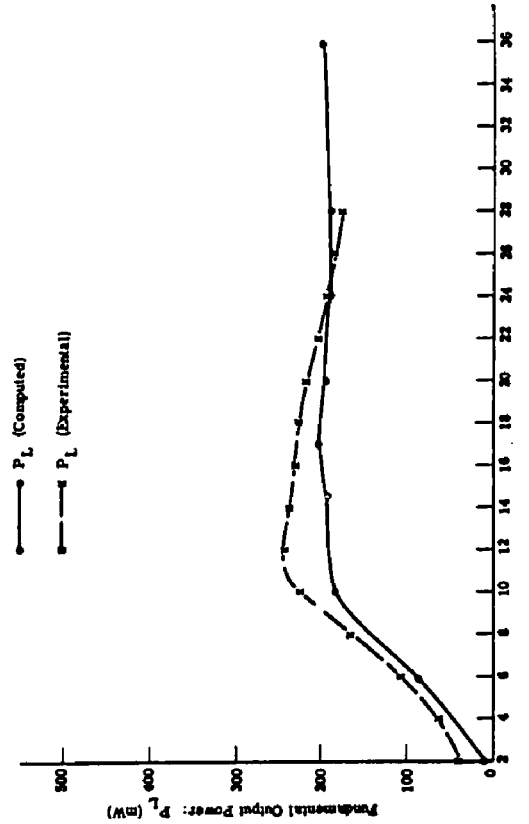


Fig. 5.11 Effect of supply voltage on output power

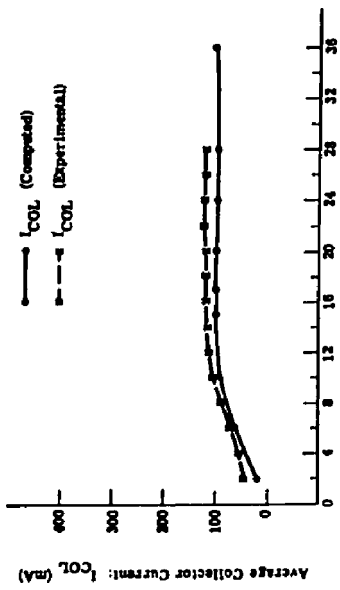


Fig. 5.14 Effect of supply voltage on collector current

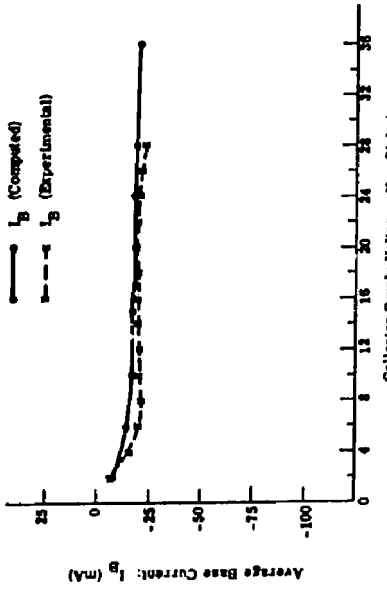
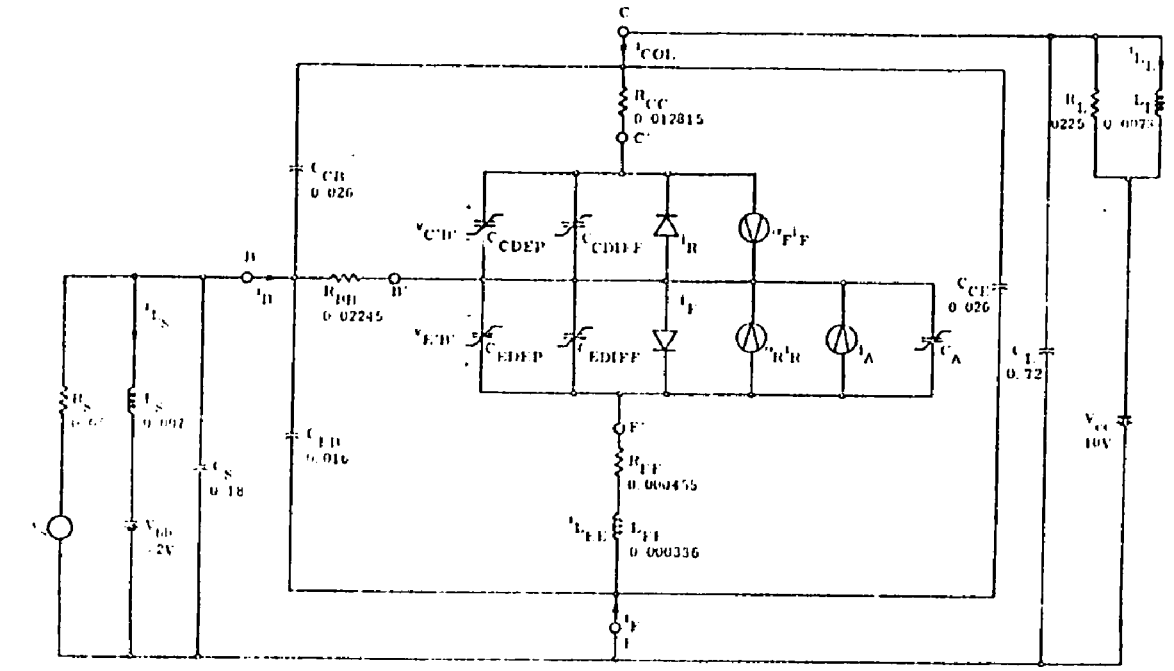


Fig. 5.13 Effect of supply voltage on base current



$$I_F = \frac{Q_{FS}}{\alpha_F \tau_F}\left(e^{-\lambda v_{E'B'}} - 1\right)$$

$$I_R = \frac{Q_{RS}}{\alpha_R \tau_R}\left(e^{-\lambda v_{C'B'}} - 1\right)$$

$$C_{EDIFF} = \lambda Q_{FS} e^{-\lambda v_{E'B'}}$$

$$C_{CDIFF} = \lambda Q_{RS} e^{-\lambda v_{C'B'}}$$

$$C_{EDEP} = \frac{C_{JE}}{(A_E)^{\gamma_E}} + C_{FE}$$

$$A_E = \text{Supremum}\left\{\begin{matrix} VZE \\ A_{ELIM} \end{matrix} + v_{E'B'}\right\}$$

$$C_{CDEP} = \frac{C_{JC}}{(A_C)^{\gamma_C}} + C_{FC}$$

$$A_C = \text{Supremum}\left\{\begin{matrix} VZC \\ A_{CLIM} \end{matrix} + v_{C'B'}\right\}$$

$$I_A = \frac{Q_{FS}}{\alpha_F \tau_F}\left[\frac{1}{1-(v_{EB} - V_A)^{N_A}} - 1\right]$$

$$C_A = \frac{\tau_F I_A}{V_A - v_{E'B'}}$$

$$V_S = VSDC + VSA \sin\frac{2\pi}{T} t$$

$\alpha_F = 0.9877$

$\alpha_R = 0.6667$

$Q_{FS} = 4.66 \times 10^{-10}$

$Q_{RS} = 1.16 \times 10^{-7}$

$\tau_F = 0.011$

$\tau_R = 2.5$

$\lambda = 21.3$

$C_{JE} = 1.04$

$C_{FE} = 0.01$

$VZE = 0.8$

$\gamma_E = 0.314$

$A_{ELIM} = 0.06$

$C_{JC} = 0.341$

$C_{FC} = 0.17$

$VZC = 0.5$

$\gamma_C = 0.474$

$A_{CLIM} = 0.0625$

$V_A = 6.2$

$N_A = 4.0$

$VSDC = -2$

Fig. 5.15. Scaled equivalent amplifier representation with extended transistor model

state equations:

$$\underset{\sim}{S}\,\dot{\underline{X}} = \underset{\sim}{A}'\,\underline{X} + \underset{\sim}{B_N}'\,\underline{U_N} + \underset{\sim}{B_S}'\,\underline{U_S} \tag{5.1}$$

where

$$\underline{X}^T = \left[v_{EB},\ v_{CE},\ v_{E'B''},\ v_{C'B''},\ i_{L_S},\ i_{L_{EE}},\ i_{L_L}\right]$$

$$\underline{U_N}^T = \left[i_F,\ \alpha_F i_F,\ i_R,\ \alpha_R i_R,\ i_A\right]$$

$$\underline{U_S}^T = \left[v_S,\ V_{CC},\ V_{BB}\right]$$

$$\underset{\sim}{S} = \begin{bmatrix} C_S+C_{BE}+C_{CB} & C_{CB} & 0 & 0 & 0 & 0 & 0 \\ C_{CB} & C_L+C_{CE}+C_{CB} & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & C_E & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & C_C & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & L_S & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & L_{EE} & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & L_L \end{bmatrix}$$

$$\underset{\sim}{A'} = \begin{bmatrix} -\frac{1}{R_S} - \frac{1}{R_{BB}+R_{CC}} & -\frac{1}{R_{BB}+R_{CC}} & 0 & \frac{1}{R_{BB}+R_{CC}} & 1 & \frac{1}{R_{BB}+R_{CC}} & 0 \\ -\frac{1}{R_{BB}+R_{CC}} & -\frac{1}{R_L} - \frac{1}{R_B+R_{CC}} & 0 & \frac{1}{R_{BB}+R_{CC}} & 0 & -\frac{R_{BB}}{R_{BB}+R_{CC}} & -1 \\ 0 & 0 & 0 & 0 & 0 & -1 & 0 \\ \frac{1}{R_{BB}+R_{CC}} & \frac{1}{R_{BB}R_{CC}} & 0 & -\frac{1}{R_{BB}+R_{CC}} & 0 & \frac{R_{BB}}{R_{BB}+R_{CC}} & 0 \\ -1 & 0 & 0 & 0 & 0 & 0 & 0 \\ -\frac{R_{CC}}{R_{CC}+R_{BB}} & \frac{R_{BB}}{R_{CC}+R_{BB}} & 1 & -\frac{R_{BB}}{R_{CC}+R_{BB}} & 0 & -R_{EE} - \frac{R_{BB}R_{CC}}{R_{BB}+R_{CC}} & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}$$

$$\underset{\sim}{BN}' = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & -1 & -1 \\ 0 & -1 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix} \qquad \underset{\sim}{BS}' = \begin{bmatrix} -\frac{1}{R_S} & 0 & 0 \\ 0 & \frac{1}{R_L} & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & -1 \\ 0 & 0 & 0 \\ 0 & -1 & 0 \end{bmatrix}$$

with the necessary side conditions

$$i_F = \frac{Q_{FS}}{\alpha_F \tau_F} \left(e^{-\lambda v_{E'B'}} - 1 \right) \tag{5.2}$$

$$i_R = \frac{Q_{RS}}{\alpha_R \tau_R} \left(e^{-\lambda v_{C'B'}} - 1 \right) \tag{5.3}$$

$$i_A = \frac{Q_{FS}}{\alpha_F \tau_F} \left[\frac{1}{1 - (v_{E'B'}/V_A)^{N_A}} - 1 \right] \tag{5.4}$$

and

$$C_E^* = C_{EDIFF} + C_{EDEP} + C_A \tag{5.5}$$

---

*As described in Chapter 2.

$$C_C = C_{CDIFF} + C_{DEP} \tag{5.6}$$

The technique employed for finding the forced steady-state solution was the same as had been used successfully in earlier analyses of the various class C amplifier simulations. The actual algorithm used for solution of this system of equations is illustrated and discussed in Appendix C. The steps involved in the numerical solution can be summarized as:

(1) Guess the initial values of the seven state variables.

(2) Solve the system of equations for one period of the input forcing signal with a double precision predictor-corrector numerical integration routine.

(3) Compare the final values of the state variables to the initial values.

(a) If the final values are sufficiently near the initial values, the steady-state solution has been found, and the next portion of the analysis can be conducted.

(b) If the final and initial values are not sufficiently near, set the initial values to be equal to the final values and repeat parts (2) and (3).

(4) Integrate the steady-state waveforms to determine average base current, average collector current, collector power dissipation, etc.

(5) Perform a numerical Fourier analysis of the solution waveforms, and compute the power gain, output power, efficiency, etc.

5.3.1 Effects of Signal Source Amplitude. The computed effects of input source amplitude on amplifier behavior are indicated in Figs. 5.16, 5.17 and 5.18. These calculated results show that a source amplitude of 8 volts peak produces average base and collector current values (-17. ma and 85 ma, respectively) close to the values measured experimentally (-20 ma and 110 ma). The source amplitude determined from the experimental measurements at 100 MHz with the directional coupler and a peak reading voltmeter in the input circuit was 18.3 volts peak. However, observations with a sampling type oscilloscope (Fig. 5.2) indicated appreciable distortion was present in the incident signal from the input source and that the peak amplitude of the fundamental component was approximately 8.0 volts.

The problems created by the distortion and uncertainty of input signal amplitude can be alleviated by choosing a computational source amplitude that provides agreement between the experimental and computed device terminal currents and by comparing the output load powers rather than the power gains.[1] Such an approach was used for the

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[1] Of course, the power gains can be obtained from the output load powers and the input source amplitudes, e.g.,

$$\text{Transducer Power Gain} = \frac{P_{Load}}{(VSA)^2/8R_s}$$

but will have limited meaning for comparisons with this 100 MHz amplifier.

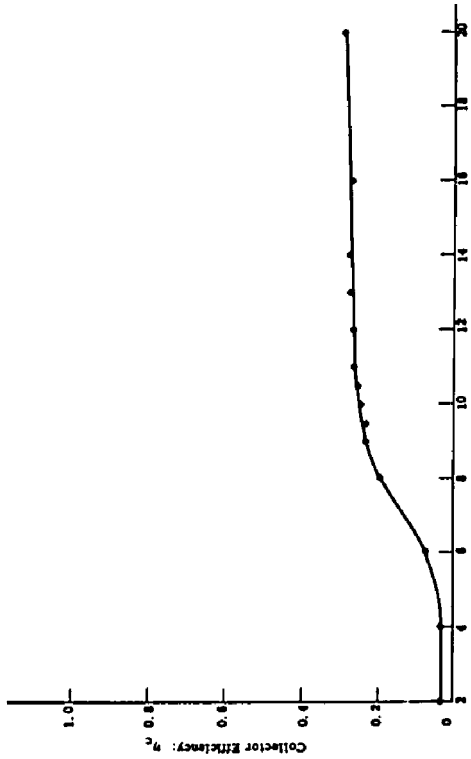

Fig. 5.17. Effect of source amplitude on efficiency

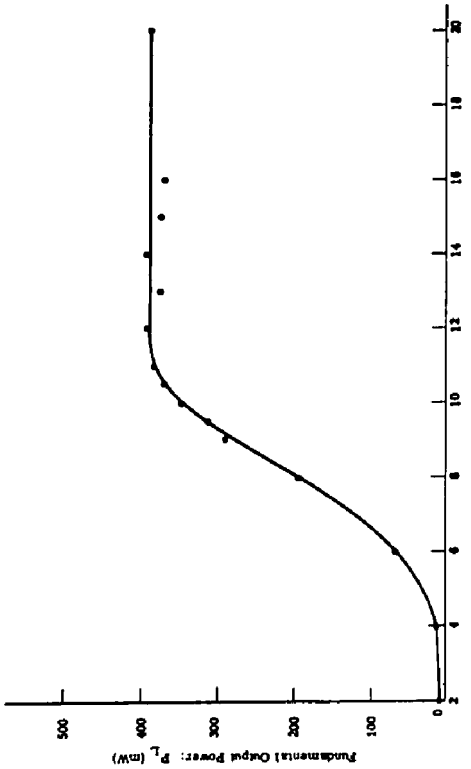

Fig. 5.16. Effect of source amplitude on output power

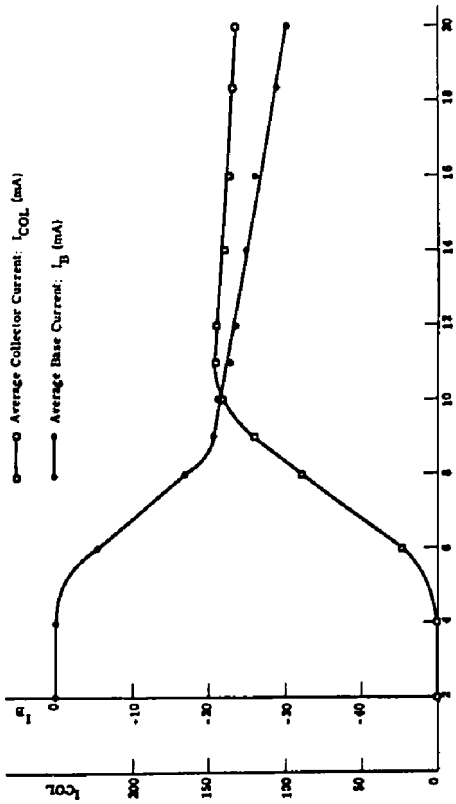

Fig. 5.18. Effect of source amplitude on base and collector current

analyses with the extended transistor model.

5.3.2 Computed Performance. The computed waveforms and load power spectrum of the 100 MHz amplifier operating with the reference circuit conditions of Fig. 5.15 are shown in Figs. 5.19 and 5.20. The waveforms of collector-emitter and emitter-base voltage[1] exhibit the same peak amplitudes and shapes, within experimental measurement accuracy, as observed with the experimental amplifier (Fig. 5.2). One advantage of the computer simulation lies in the ability to predict waveshapes such as the terminal currents and the junction voltages that cannot conveniently be measured experimentally. (E.g., experimental attempts to observe the current waveshapes at VHF frequencies usually disturb the amplifier circuit to such an extent that the results are unreliable.) The complexity of the base and collector current waveforms illustrates the falacy of assuming simple analytic pulse forms to predict high frequency amplifier performance. Assumptions of sinusoidal emitter-base junction potential are also unrealistic in such large signal analyses.

For comparison with the experimentally observed amplifier behavior, the computed effects of input signal frequency over a two octave bandwidth are also given in Figs. 5.3 through 5.6. Effects of load resistance and collector supply voltage are illustrated in Figs. 5.7

[1]Note that experimentally the base-emitter voltage was observed and computationally the emitter-base voltage is shown. This polarity reversal should be remembered when making the emitter-base waveform comparisons.

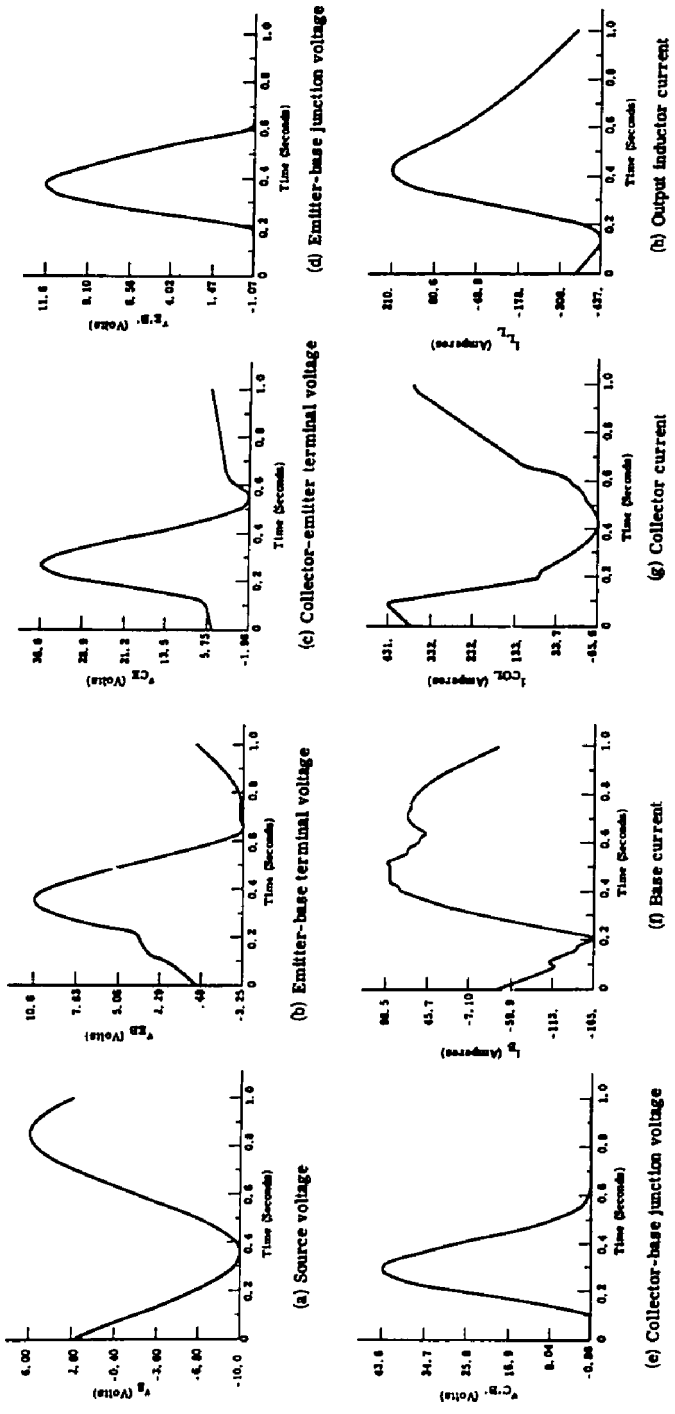

Fig. 5.19. Typical waveforms with extended model analysis

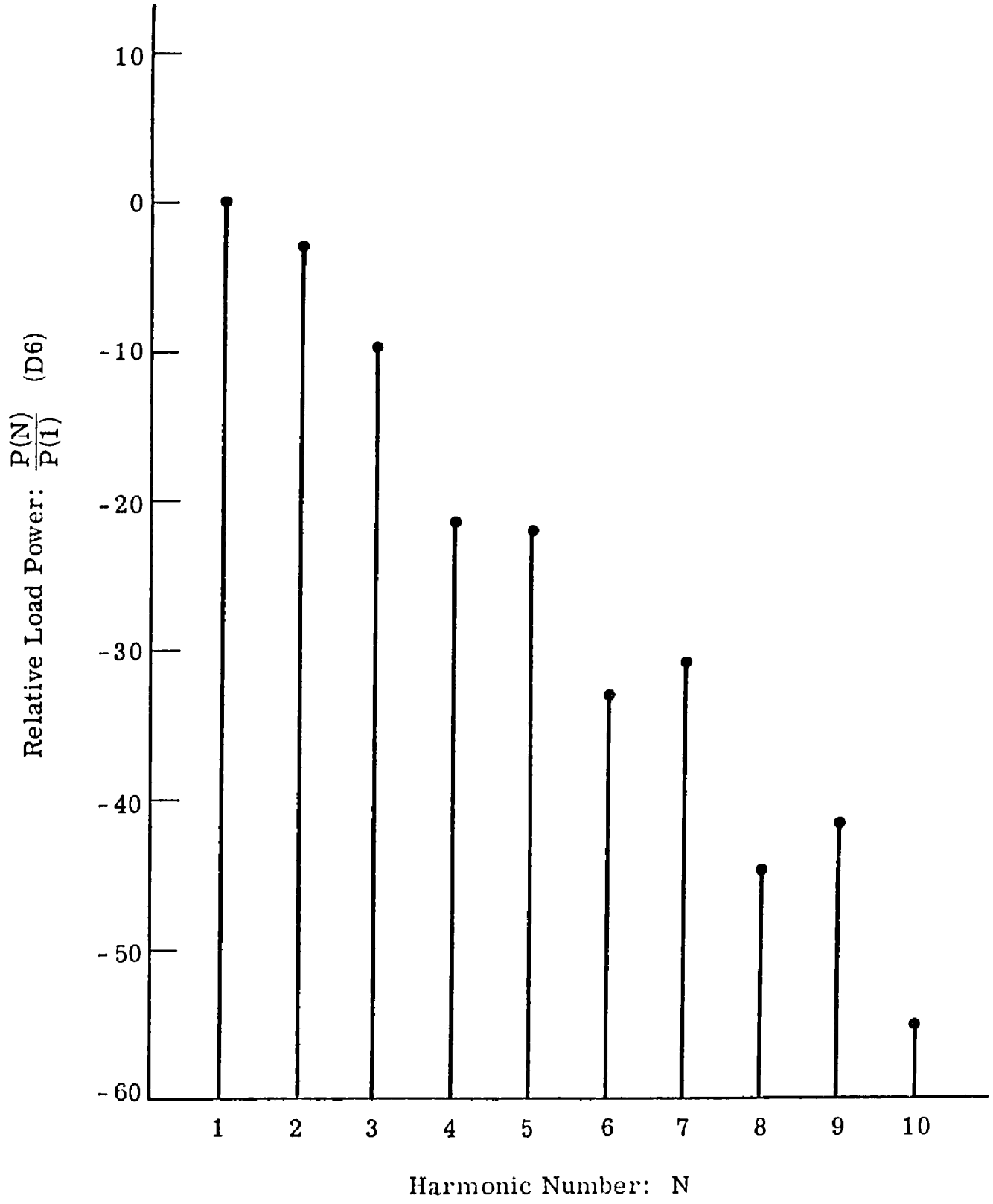

Fig. 5.20. Computed output power spectrum

through 5.14. These computed results appear to be in moderate agreement with those of the experimental amplifier except for load resistances larger than 300 ohms. In the load resistance region of 200 to 300 ohms, the computed collector current is observed to have two possible modes, with the mode of operation being determined by initial conditions. The waveshapes resulting from each of the two modes appear generally the same with the exception that operation in mode 2 causes the transistor to remain in saturation longer than it does in mode 1. The operating paths of the collector circuit for both modes are plotted in Fig. 5.21. From this plot we observe that the peak signal amplitudes are greater for mode 2, but the paths of the limit cycles for both modes are similar. The limit cycles of the junction potentials (Fig. 5.22) provide additional information about the differences between the two modes of operation. In mode 2 the transistor is driven into the inverse region for approximately 10 percent of the cycle. This does not occur in mode 1 where, as with most class C amplifiers, the collector potential does swing negative with respect to the base potential when the emitter-base junction is reverse biased. The possibility of operation in the inverse region increases with large collector voltabe amplitudes that result with very large load resistances.

Mode hopping was not observed experimentally in the range of load resistance investigated. However, such behavior is not unusual for tuned power amplifiers, and mode changes with frequency, source

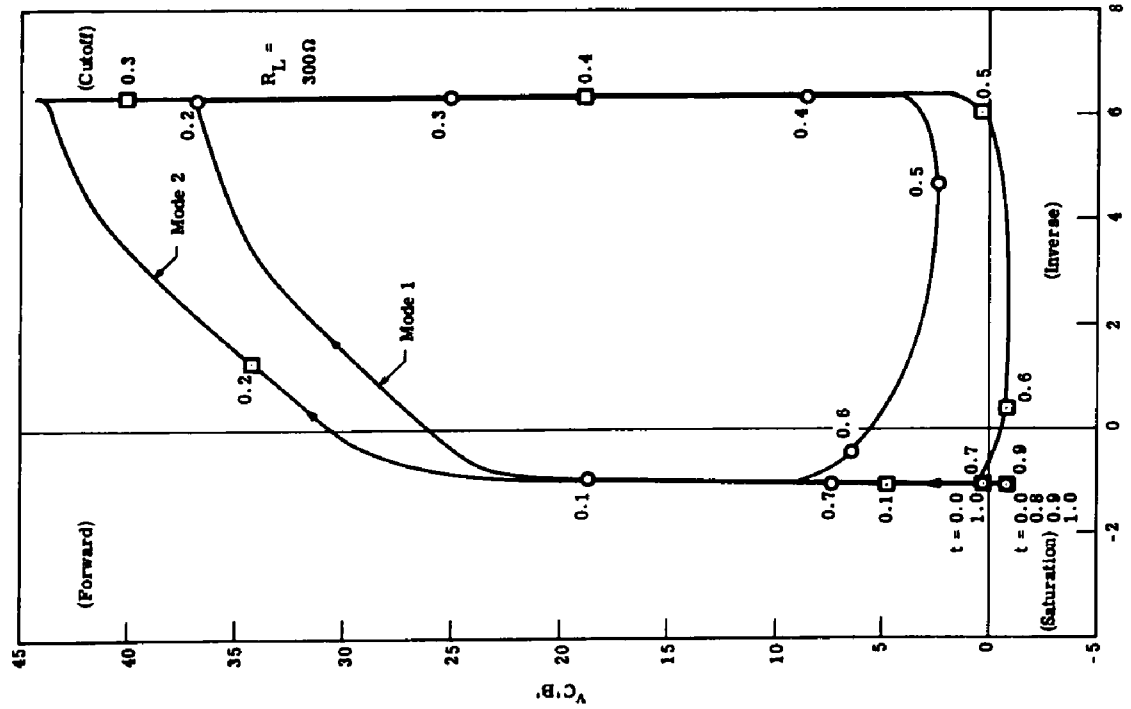

Fig. 5.22 Limit cycle of junction potentials

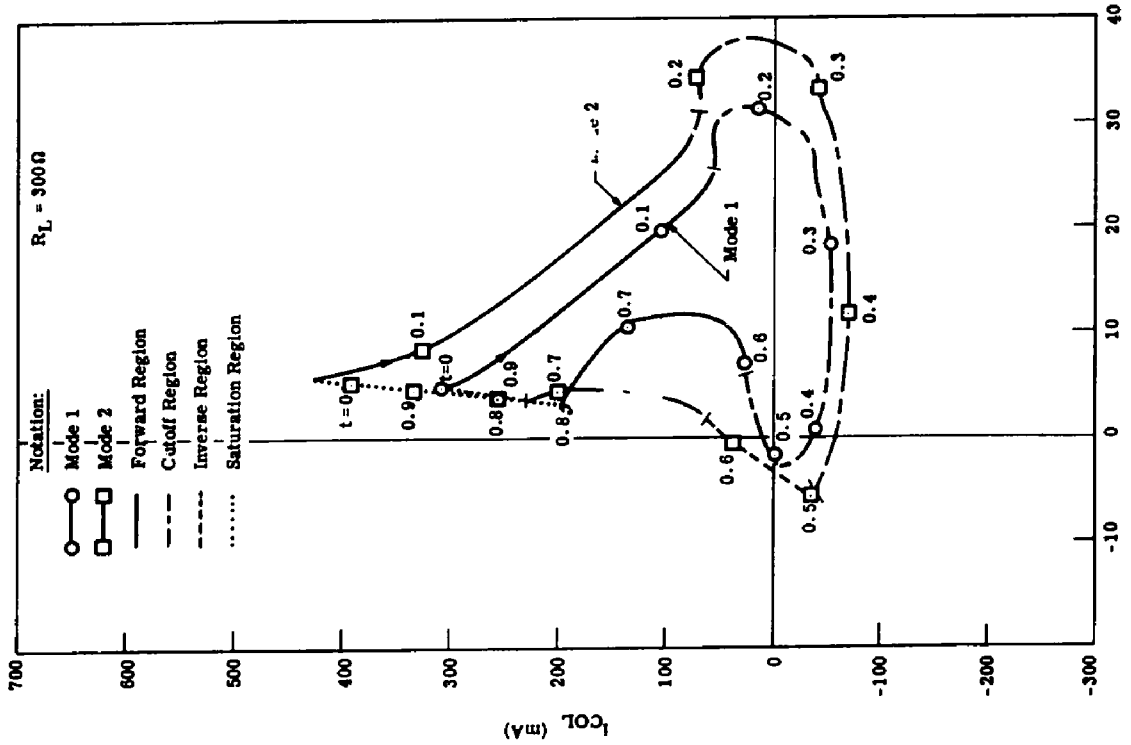

Fig. 5.21 Collector circuit limit cycle

amplitude, and supply voltage have been observed in similar amplifiers utilizing the 2N3866 at VHF frequencies. For example, the class A_1 amplifier circuit of Fig. 5.23 was developed as part of a wideband amplifier study.[1] The swept frequency response of the amplifier (Fig. 5.24) over a frequency range of 70 to 400 MHz was found to be dependent on the input signal power. The three response curves of Fig. 5.24 correspond to input powers of 4.23, 2.12, and 0.841 milliwatts. Relatively smooth response characteristics resulted for small input powers; but the response was found to "break up" at the higher signal levels, particularly for frequencies below 200 MHz.

A sampling oscilloscope was used to monitor the output voltage waveforms of the amplifier at fixed operating frequencies. The output waveforms of Fig. 5.25 were observed at a signal frequency of 190 MHz and illustrate the jump in operating mode that can result from changes in signal amplitude. As the signal amplitude is increased, the output signal remains nearly sinusoidal up to the level shown in the top trace which is 8.8 volts peak to peak. A slight further increase of the input amplitude causes the output waveform to jump to the one shown in the lower trace. In this new operating mode, substantial harmonic content is evident in the output waveform. This same hopping of mode produced the irregularities mentioned for the swept frequency response (Fig. 5.24).

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[1]This study was conducted by A. B. Macnee and Dennis Packard at The University of Michigan Cooley Electronics Laboratory.

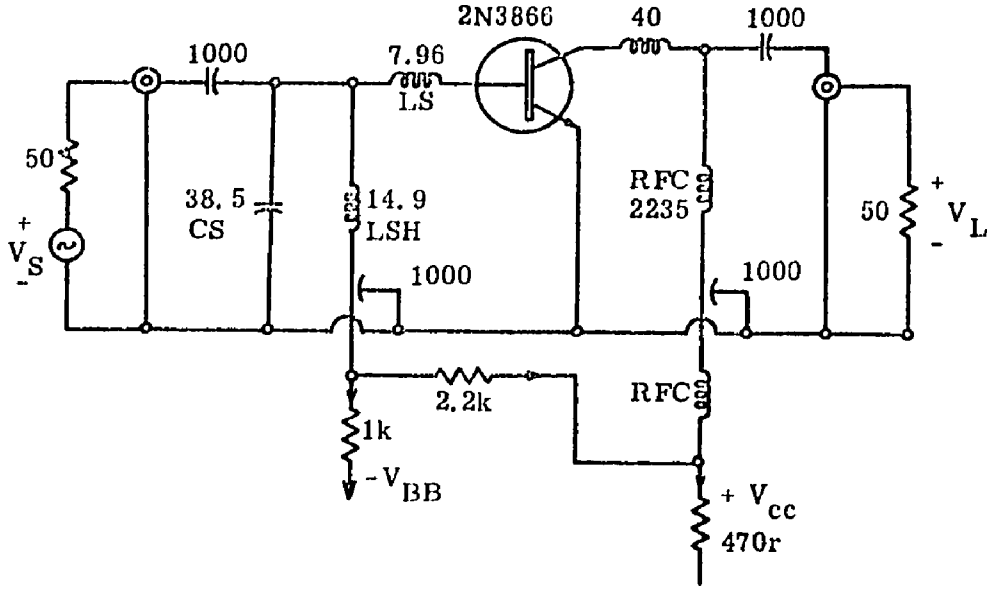


Fig. 5.23. Experimental class A_1 wideband amplifier circuit

The nonlinear mode hopping behavior is representative of the effects that can be investigated conveniently with computer simulations but not with analytical techniques. Various transistor parameters (depletion capacities, charge storage time constants, static current gain, emitter lead inductance, etc.) can be altered in the simulation, and their effects on circuit stability and performance can be evaluated. In this manner the simulation can be used to determine which device parameters are critical in the operation of a given circuit and thereby suggest optimum devices for such application.

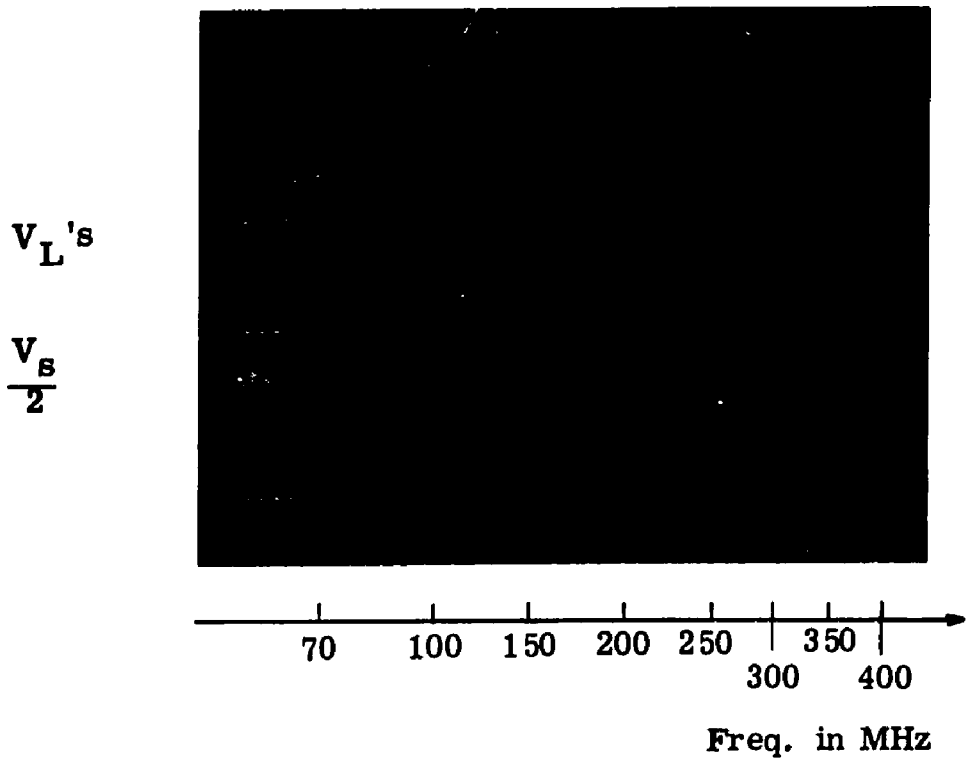


Fig. 5.24. Swept frequency response of experimental amplifiers; available input powers are 4.23, 2.12, and 0.841 mW

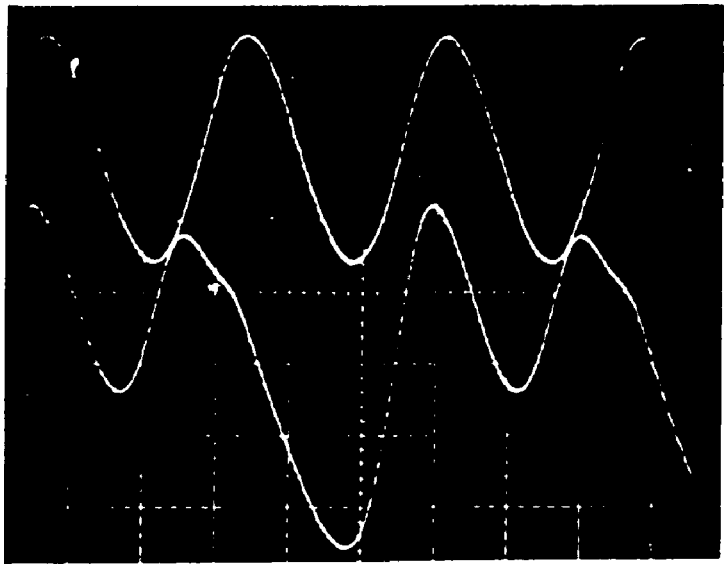


Fig. 5.25. Output waveform change associated with "mode jump" at 190 MHz. Vertical scale 3 V per division; horizontal scale 2 ns per division

5.4 Amplifier Sensitivities

In addition to guiding selection of transistor types, we can utilize the extended model representation of a tuned power amplifier to estimate how critical each circuit and device parameter is to the overall behavior of the amplifier. If we determine that some device parameter has a strong influence on computed performance, then the value of that parameter must be determined precisely to achieve accurate simulations. Less critical values need not be measured as precisely or in some simulations may be removed from the model.

The simulation circuit of the 100 MHz amplifier is representative of many power amplifier configurations. Thus, the sensitivity of this circuit behavior to the various transistor parameters should be representative of many applications. The sensitivity of a circuit behavior function to a change in a circuit parameter can be described briefly as

$$S_p^f = \frac{\partial f/f}{\partial p/p} \approx \frac{\Delta f/f}{\Delta p/p} = \frac{[f(p') - f(p)]/f(p)}{(p' - p)/p} \qquad (5.7)$$

where

f is a function of several parameters of which p is one

p is the parameter under investigation

$p' = p + \Delta p$

Δp is a small variation in p

In general, we wish to make as small a perturbation, Δp, in the parameter value, p, as possible. However, in numerical analyses, too small a perturbation may cause such small variations in the functions under consideration that the variations are lost in computational noise. For the computer-aided sensitivity analyses with the extended transistor model, parameter variations of 10 percent seem reasonable. By making such variations from the standard values (shown in Fig. 5.15) for each of the model and circuit parameters, the sensitivities of output power, efficiency, base current, and collector current have been determined (Table 5.1).

From these tabulated results we find, for example, that a 10 percent error in modeling the forward current transport factor, α_F, can lead to an error of 48.3 percent in the computation of the output power of the amplifier. This sensitivity to a change in transistor α_F can be expressed alternatively in terms of the common emitter static current gain of the transistor, β_F, by the manipulation

$$S^{P_L}_{\beta_F} = S^{P_L}_{\alpha_F} \cdot \frac{\partial\, \alpha_F/\alpha_F}{\partial\, \beta_F/\beta_F} = S^{P_L}_{\alpha_F} \cdot (1 - \alpha_F) = 0.0594$$

where

$$\beta_F = \frac{\alpha_F}{1 - \alpha_F}$$

Thus we find the sensitivity of output power to the directly measured

	Amplifier Functions			
Parameters	P_L	η_c	I_B	I_{COL}
VSA	3.88	0.321	+2.02	3.47
BSDC	-2.88	-0.125	+0.0490	-2.72
V_{cc}	0.874	-0.433	-0.316	0.370
T	-2.67	0.135	-1.04	-2.78
R_S	-1.52	-0.392	-0.792	-1.17
L_S	0.600	-0.125	-0.00646	0.798
C_S	0.0739	-0.117	-0.179	0.153
R_L	-0.236	-0.721	+0.291	0.440
L_L	1.50	0.715	-0.437	0.670
C_L	1.91	0.234	+0.131	1.52
C_{CB}	-0.0821	-0.0874	-0.170	0.0371
C_{BE}	0.00513	0.00330	+0.0889	-0.0137
C_{CE}	0.199	-0.0346	+0.0407	0.155
R_{CC}	-0.455	-0.228	-0.495	-0.190
R_{BB}	2.74	0.759	+0.899	1.70
R_{EE}	-0.00977	0.377	-0.246	-0.0844
L_{EE}	-0.0506	0.178	-0.131	-0.216
Q_{FS}	0.0724	-0.164	-0.219	0.204

Table 5.1. Sensitivities with extended transistor model analysis

	Amplifier Functions			
Parameters	P_L	η_c	I_B	I_{COL}
Q_{RS}	-0.107	0.0521	-0.330	-0.157
τ_F	-0.506	-0.251	-0.230	-0.250
τ_R	-0.0602	0.138	-0.335	-0.133
α_F	4.83	1.09	+5.24	4.24
α_R	-0.456	-0.325	-0.150	0.224
λ	1.40	-0.181	-0.0589	1.53
V_A	1.91	-0.131	-1.65	2.03
N_A	0.0759	-0.0595	+0.0961	0.0801
C_{JC}	-0.224	-0.294	-0.126	0.114
V_{ZC}	0.0975	-0.0525	-0.00972	0.0675
γ_C	-0.00308	0.0464	-0.471	0.0495
C_{FC}	-0.0350	-0.194	+0.00662	0.176
ACLIM	-0.0317	-0.0987	-0.150	0.0693
C_{JE}	-0.247	0.167	-0.440	-0.400
V_{ZE}	0.187	-0.0444	-0.152	0.196
γ_E	0.317	0.199	+0.118	0.0573
C_{FE}	0.118	-0.0550	+0.0555	0.0820
AELIM	0.139	-0.0526	+0.0184	0.108

Table 5.1. (Cont.)

model parameter, β_F, to be much less than the sensitivity of α_F, and in consideration of modeling accuracy requirements, the β_F dependence has the more direct significance. As a similar application of the tabulated sensitivities, we observe that using a 2N3866 transistor with an emitter-base avalanche potential, V_A, 10 percent greater than the 6.2 volts used in this simulation could lead to a 20.3 percent increase in the average collector current of the amplifier circuit.

5.5 Conclusions

The computations utilizing the extended transistor model have demonstrated the ability of the simulation to predict the behavior of VHF power amplifiers. The simulation provides the versatility and convenience of monitoring several functions that cannot be observed readily with experimental techniques. In addition the simulation can be used to predict how changes in transistor parameters will effect the amplifier behavior. Further comparisons of the extended model analyses to analyses with other model representations will be given in the following chapter.

CHAPTER 6

COMPARISON OF AMPLIFIER REPRESENTATIONS

6.1 Introduction

The ideal switch and intrinsic transistor model representations have been found to be useful for analysis and study of basic characteristics of low frequency tuned power amplifiers. In the high frequency analyses with the intrinsic transistor model, some of the behavior predictions were found to differ significantly from results obtained with a 100 MHz experimental amplifier. Consequently, the intrinsic model was augmented to include major extrinsic effects, and the resulting extended transistor model was used for calculations and comparisons with another 100 MHz experimental amplifier.

In order to provide a better comparison between the various models, all of them are used in this chapter to predict the fundamental characteristics of a common amplifier. The amplifier chosen for this comparison standard is the experimental 100 MHz amplifier presented in Chapter 5 and shown again in Fig. 6.1. Small signal measurements of the passive output network of the amplifier at a frequency of 100 MHz led to the equivalent output circuit of Fig. 6.2. Observation of the collector-emitter voltage waveform of the experimental amplifier indicated that the transistor was in saturation approximately 40.4 percent of the time which implies a switching duty

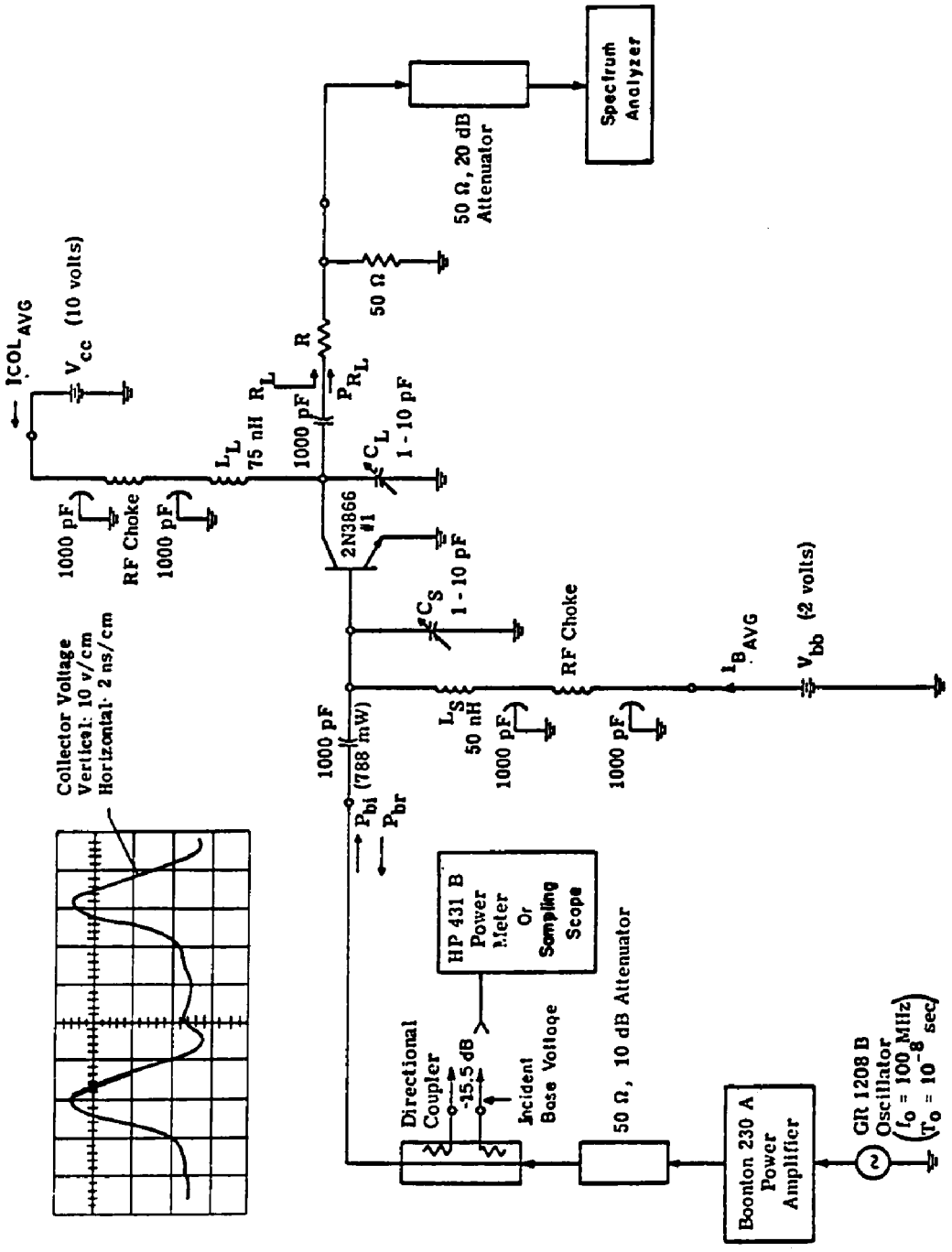


Fig. 6.1. 100 MHz experimental amplifier, measurement circuit and collector voltage waveform

factor of 0.404 for analyses with the ideal switch representations. Scaling the amplifier center frequency by a factor of 10^8 and scaling the network currents by 10^3 leads to the computational models illustrated in Figs. 6.3, 6.4, 6.5, and 6.6. The capacitance value chosen for the fixed capacitance-ideal switch model, C, represents the sum of the output tuning and stray capacitances of the amplifier and the net collector-base capacitance of the 2N3866 transistor evaluated at the average collector-base potential, $V_{cc} - V_{bb}$. Similarly, the capacitance parameters for the ideal switch-depletion capacitance representation were selected to match the collector-base depletion capacitance characteristics of the 2N3866. The intrinsic and extrinsic transistor model parameters were also chosen to match the 2N3866 characteristics as discussed in Chapter 2.

Analyses with each of the amplifier representations were conducted numerically as discussed in preceding chapters. The amplifier's behavior characteristics chosen for investigation and comparison were circuit waveforms, fundamental output power, collector efficiency, and where applicable, average base and collector currents. The circuit parameters used as variables were source driving period, load resistance, and collector supply voltage. The computed effects of input source amplitude on the intrinsic and extrinsic transistor model representations are also included but these effects were not verified experimentally.

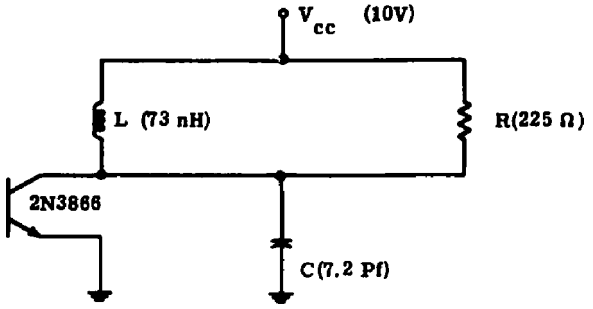


Fig. 6.2. Measured equivalent output circuit

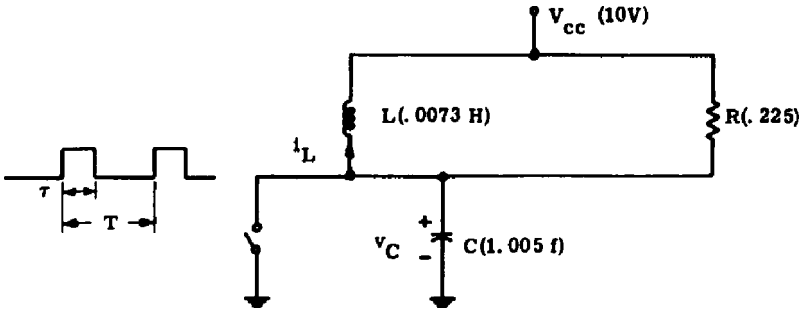
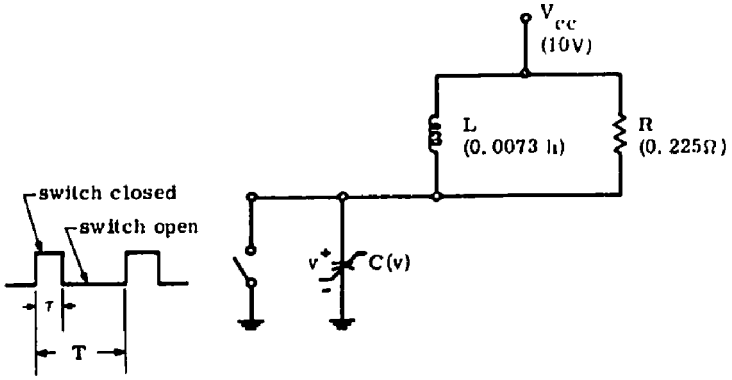


Fig. 6.3. Scaled equivalent output circuit for ideal switch analysis



$$C(v) = \frac{C_J}{(A)^{\gamma}} + C_F$$

$$A = \text{Supremum} \begin{Bmatrix} v + VZ \\ A_{LIM} \end{Bmatrix}$$

$$VZ = 0.5$$

$$A_{LIM} = 0.0625$$

$$\gamma = 0.474$$

$$C_J = 2.548$$

$$C_F = 0.17$$

Fig. 6.4. Scaled output circuit for analysis with ideal switch and depletion layer capacitance

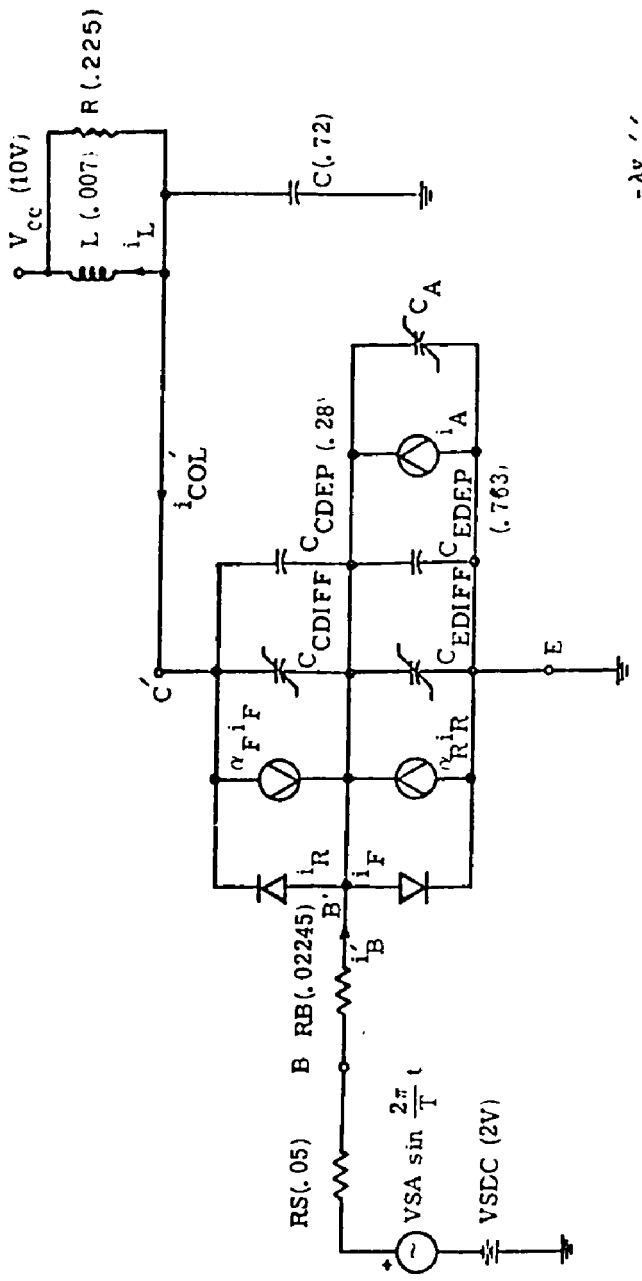
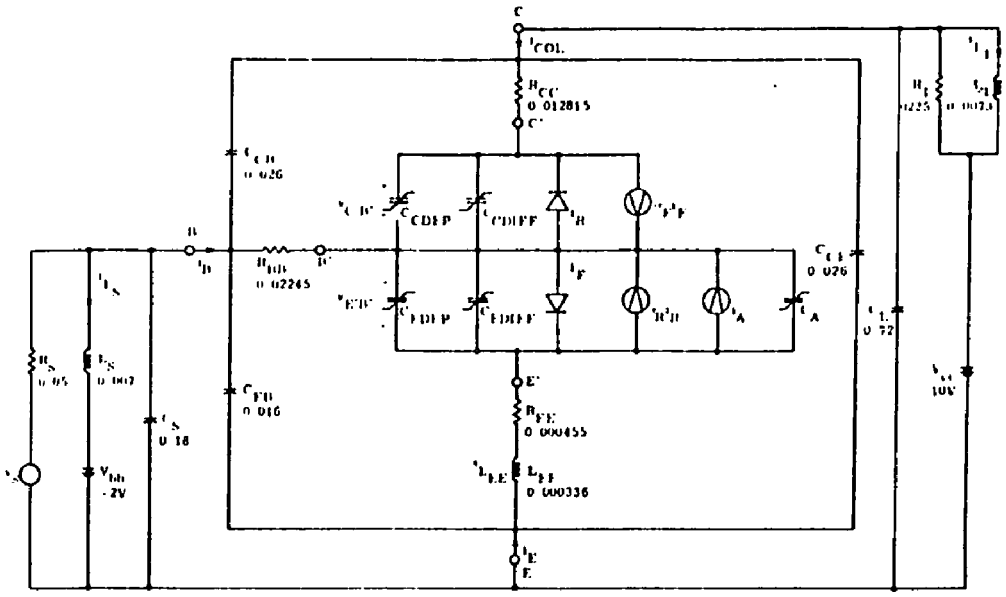


Fig. 6.5. Scaled equivalent amplifier representation with intrinsic transistor model



$$I_F = \frac{Q_{FS}}{\alpha_F \tau_F}\left(e^{-\lambda v_{E'B'}} - 1\right)$$

$$I_R = \frac{Q_{RS}}{\alpha_R \tau_R}\left(e^{-\lambda v_{C'B'}} - 1\right)$$

$$C_{EDIFF} = \lambda Q_{FS} e^{-\lambda v_{E'B'}}$$

$$C_{CDIFF} = \lambda Q_{RS} e^{-\lambda v_{C'B'}}$$

$$C_{EDEP} = \frac{C_{JE}}{(A_E)^{\gamma_E}} + C_{FE}$$

$$A_E = \text{Supremum}\left\{\begin{matrix} VZE + v_{E'B'} \\ A_{ELIM} \end{matrix}\right|$$

$$C_{CDEP} = \frac{C_{JC}}{(A_C)^{\gamma_C}} + C_{FC}$$

$$A_C = \text{Supremum}\left\{\begin{matrix} VZC + v_{C'B'} \\ A_{CLIM} \end{matrix}\right|$$

$$I_A = \frac{Q_{FS}}{\alpha_F \tau_F}\left[\frac{1}{1-(v_{E'B'}/V_A)^{N_A}} - 1\right]$$

$$C_A = \frac{\tau_F I_A}{V_A - v_{E'B'}}$$

$\alpha_F = 0.9877$

$\alpha_R = 0.6667$

$Q_{FS} = 4.66 \times 10^{-10}$

$Q_{RS} = 1.16 \times 10^{-7}$

$\tau_F = 0.011$

$\tau_R = 2.5$

$\lambda = 21.3$

$C_{JE} = 1.06$

$C_{FE} = 0.01$

$VZE = 0.8$

$\gamma_E = 0.316$

$A_{ELIM} = 0.06$

$C_{JC} = 0.341$

$C_{FC} = 0.17$

$VZC = 0.5$

$\gamma_C = 0.474$

$A_{CLIM} = 0.0625$

$V_A = 6.2$

$N_A = 4.0$

$V_S = VSIC + VSA \sin \frac{2\pi}{T} t$

$VSIC = -2$

Fig. 6.6. Scaled equivalent amplifier representation with extended transistor model

6.2 Waveform Comparisons

The output load voltage waveforms (Fig. 6.7) all have the general shape of one period of a damped sinusoid. The most predominant differences in the voltage waveforms are their amplitudes. The peak to peak amplitudes are:

Experimental ... 35V

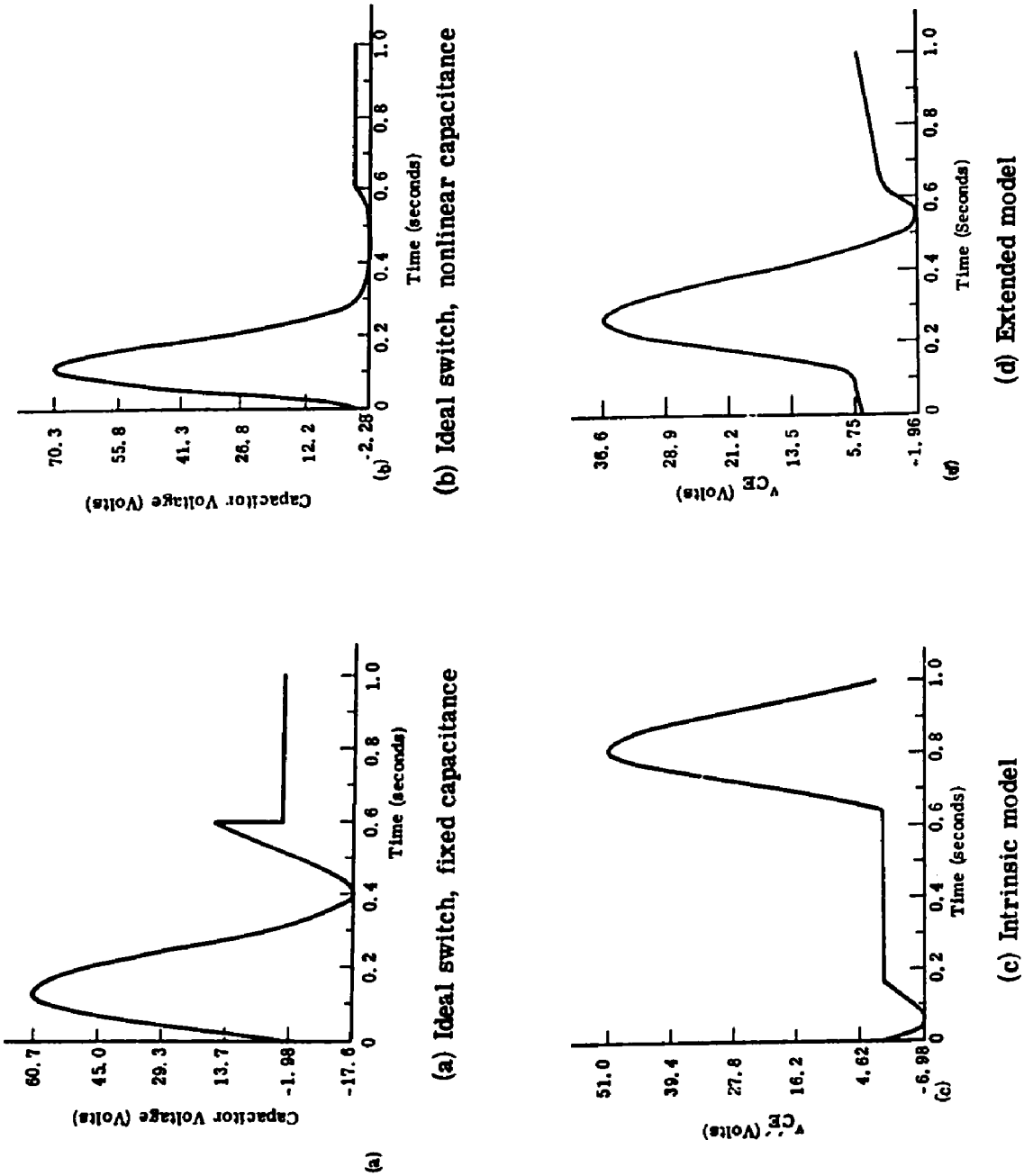
Ideal switch-fixed capacitance --- 75V

Ideal switch-depletion capacitance --- 65V

Intrinsic ... 59V

Extended --- 36V

In comparing the voltage waveforms for the ideal switch analyses we see that one effect of the nonlinear depletion capacitance is to narrow the waveform during the time that the capacitor voltage exceeds the supply voltage and to widen and limit the waveform when the voltage is small or negative. Such an effect is anticipated since the depletion capacitance value varies inversely with the capacitor voltage. Of the models considered the only form capable of producing a nearly linear change in output voltage with collector current during saturation is the extended transistor model. We see the need for adding series resistance to the output terminals of the other models if the saturation voltages are to be current dependent. The addition of such series resistance not only improves the "fit" of the saturation characteristics but also limits the rate of change of output inductor current



(a) Ideal switch, fixed capacitance

(b) Ideal switch, nonlinear capacitance

(c) Intrinsic model

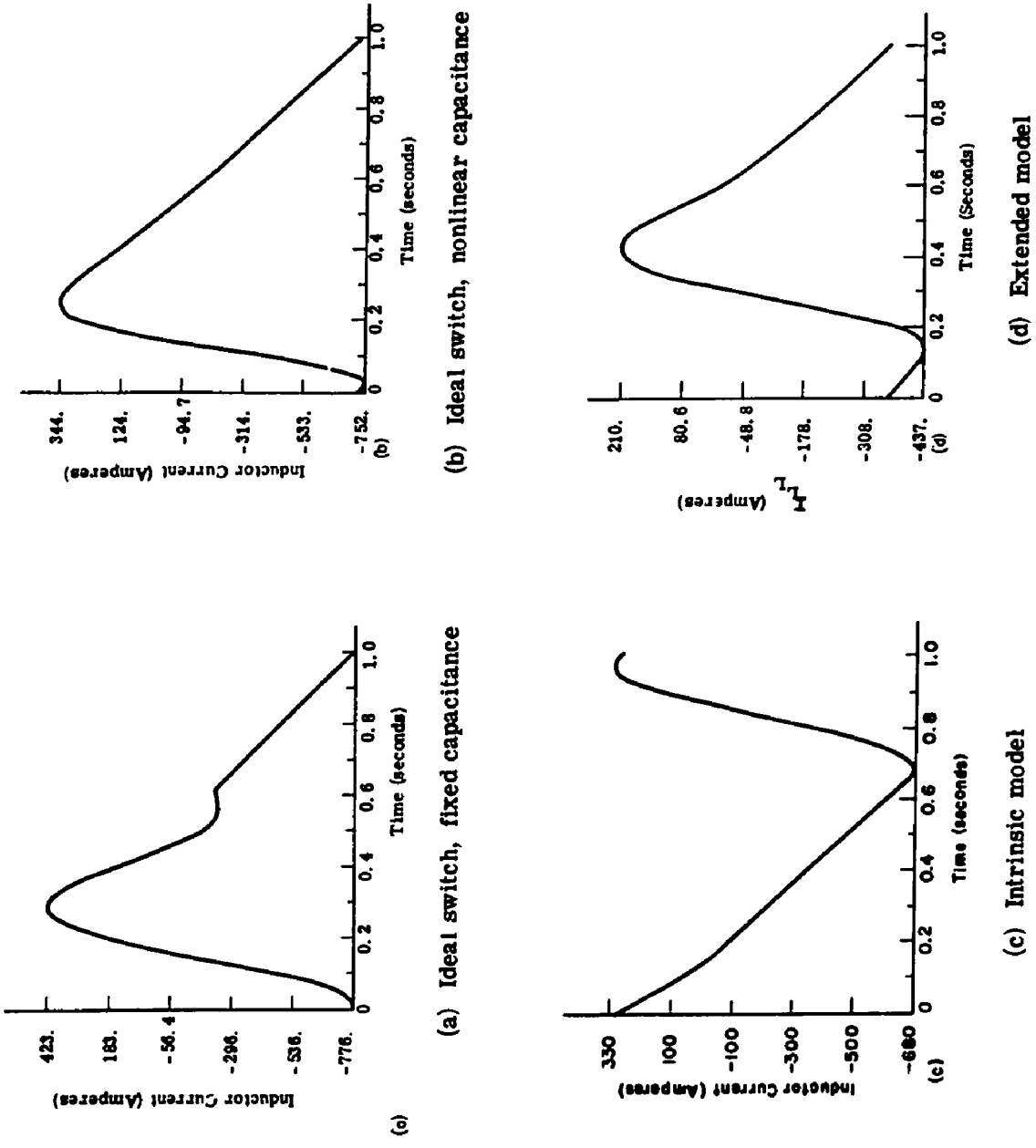
(d) Extended model

Fig. 6.7. Output voltage waveforms

during saturation. Thus adding series resistance reduces the amount of energy added to the output circuit during saturation; as a result, the output voltage amplitude is reduced. The waveforms of current in the output tuning inductors (Fig. 6.8) are proportional to the integral of output voltage, and except for amplitude differences, these waveforms are very similar to each other in appearance.

The emitter-base junction voltages resulting from analysis with the intrinsic and extended transistor models, $v_{E'B'}$, are very similar (Fig. 6.9), and as noted previously, cannot justifiably be assumed sinusoidal. The emitter-base terminal voltage of the extended model analysis (Fig. 6.9c) appears more nearly sinusoidal, which is in agreement with the experimentally observed waveform (Fig. 6.1).

The base current waveforms of the intrinsic and extended model analyses are of the same shape and amplitude, but their average values differ (Fig. 6.10). [The apparent phase shift between the intrinsic and extrinsic waveforms is produced by a shift in phase of the input signal (Fig. 6.10c) and not from differing delays in the models. This phase shift was added to improve convergence to a stable limit cycle of the numerical analysis with the extended model as described in Appendix C.] The collector currents also are of similar shape (Fig. 6.11); however, the peak amplitude calculated by intrinsic model analysis is almost twice that calculated with the



(a) Ideal switch, fixed capacitance

(b) Ideal switch, nonlinear capacitance

(c) Intrinsic model

(d) Extended model

Fig. 6.8. Inductor current waveforms

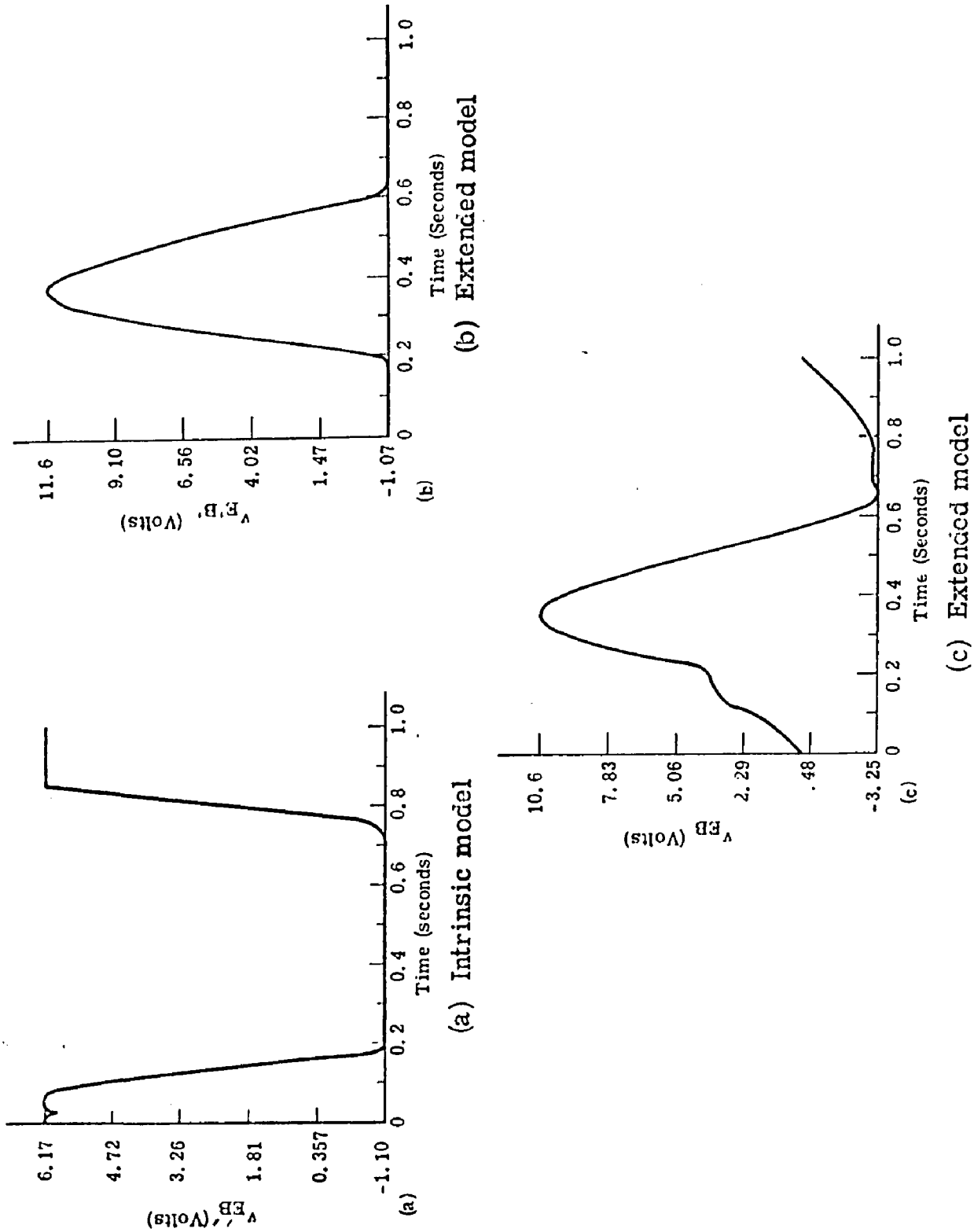
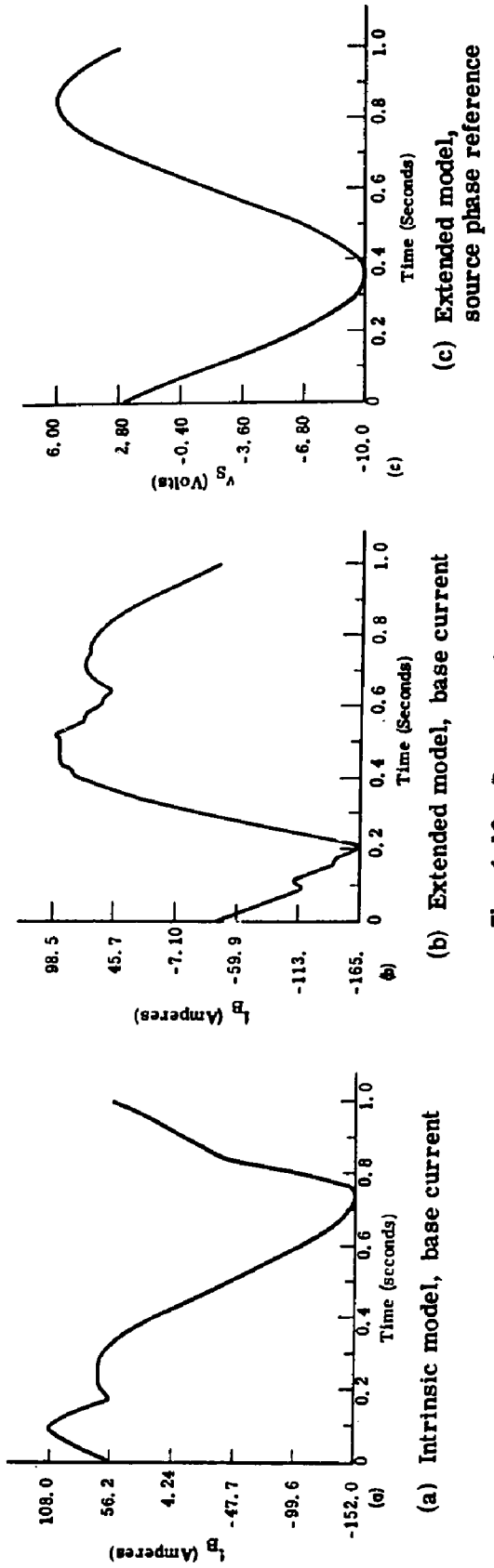


Fig. 6.9. Emitter-base voltage waveforms

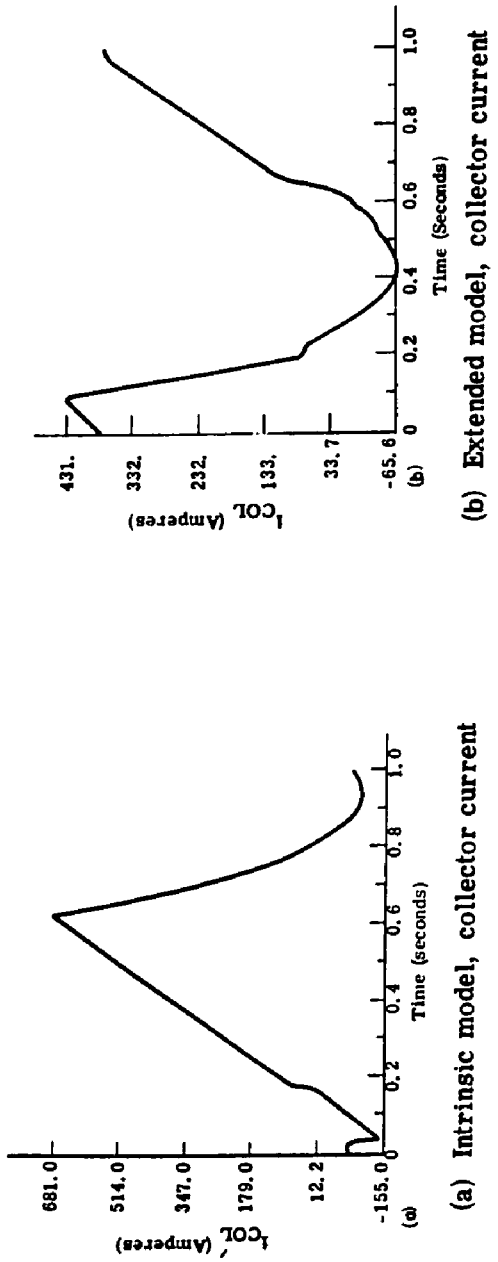


(a) Intrinsic model, base current

(b) Extended model, base current

Fig. 6.10. Base waveforms

(c) Extended model, source phase reference



(a) Intrinsic model, collector current

(b) Extended model, collector current

Fig. 6.11. Collector current waveforms

extrinsic model. Since the base and collector currents were not observed experimentally there is no direct verification of their waveform, but comparison of more easily verified characteristics (Sections 6.3, 6.4, and 6.5) will lead us to accept the extrinsic model predictions as the more accurate of the two.

6.3 Frequency Response Comparisons

Comparing the computed and measured effects of signal frequency, load resistance, and collector supply voltage on amplifier performance will allow us to evaluate the ability of the models to predict behavior over a range of operating conditions. The effects of signal frequency, or period, over a two octave bandwidth are presented in Figs. 6.12, 6.13, 6.14, and 6.15. The output powers predicted from computations with the ideal switch and intrinsic transistor models (Figs. 6.12a, b, and c) are about four times larger than the measured power. One noticeable difference in the two power responses computed with the ideal switch using (1) fixed and (2) nonlinear output capacitances (Figs. 6.12a and b) is that the nonlinear simulation predicts a slightly wider bandwidth with an abrupt roll-off for large switching periods and a more gradual roll-off for small switching periods.

With the extended model the maximum computed output power (Fig. 6.12d) is much closer to the measured power (about 40 percent greater), but the computed power peaks at a frequency of 125 MHz

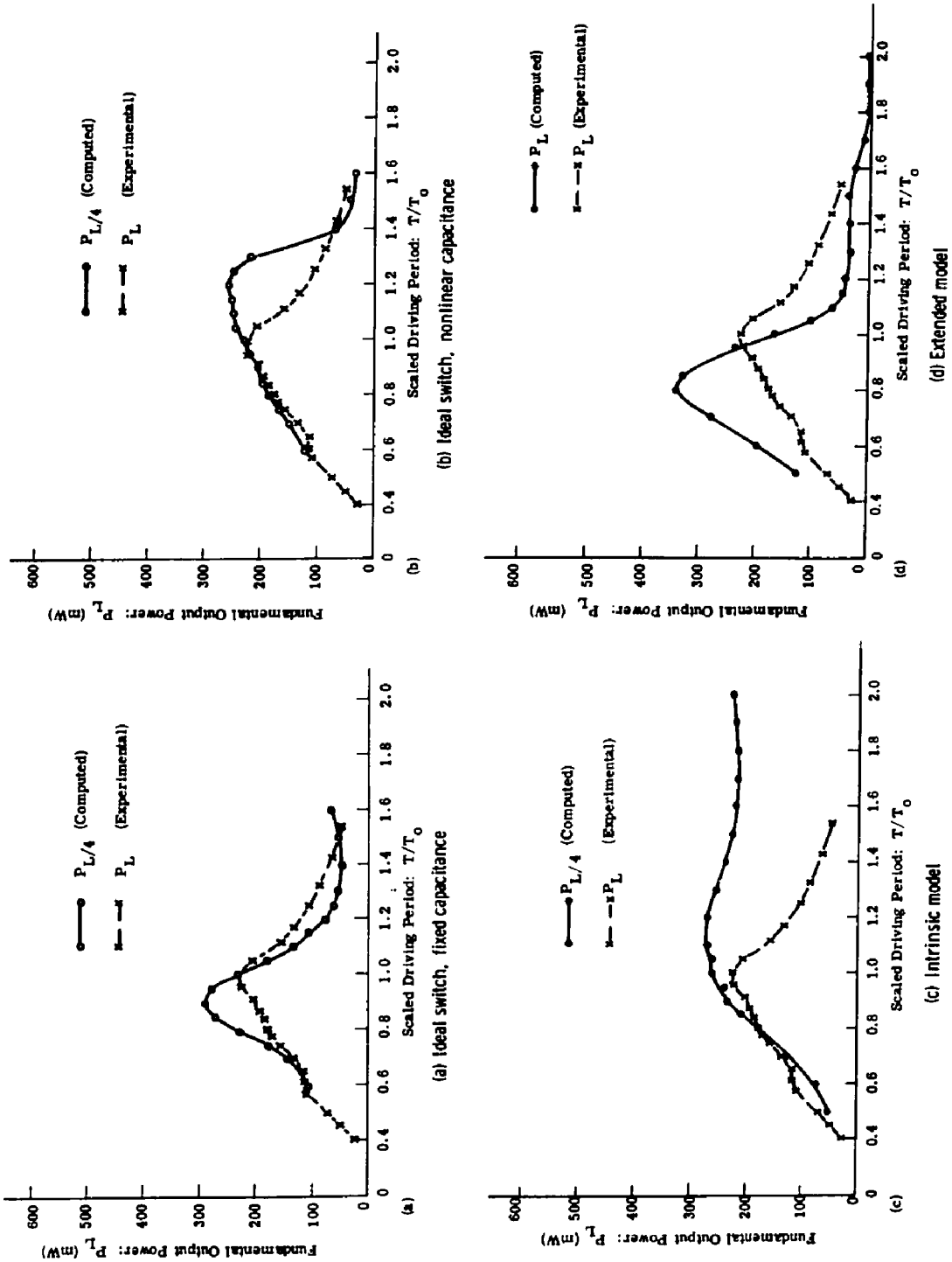


Fig. 6.12. Frequency response of output power

instead of the 100 MHz center frequency of the experimental amplifier. Although the results using the extended model are not in as close agreement to the measured amplifier performance as one would wish, the extended model does provide a significant improvement relative to the other simulations. Also, experimental measurement errors of the absolute power levels can be appreciable (about 20 percent) with the measurement techniques employed, and stray parameters in the passive tuning elements add to the measurement difficulties in the VHF range.

The efficiencies computed with the ideal switch and intrinsic model simulations (Figs. 6.13a and b) all exceed the efficiencies measured with the experimental amplifier For the extended model, the computed and measured efficiencies (Fig. 6.13d) agree quite well up to a frequency of 110 MHz ($T/T_0 \approx 0.9$). Above 110 MHz the experimental efficiency leveled off and then peaked slightly at 165 MHz ($T/T_0 \approx 0.6$). Computations with the extended model produced a peak at 165 MHz but did not exhibit the relatively flat efficiency curve between 110 and 165 MHz. As with the output power frequency response, we conclude that the extended model provides marked improvement in computations of the amplifier efficiency response.

The variations in the average base and collector currents due to changes in excitation frequency are shown in Figs. 6.14 and 6.15. Similarly to the output power and efficiency comparisons, the extended model is found to provide a better fit to the experimental amplifier than

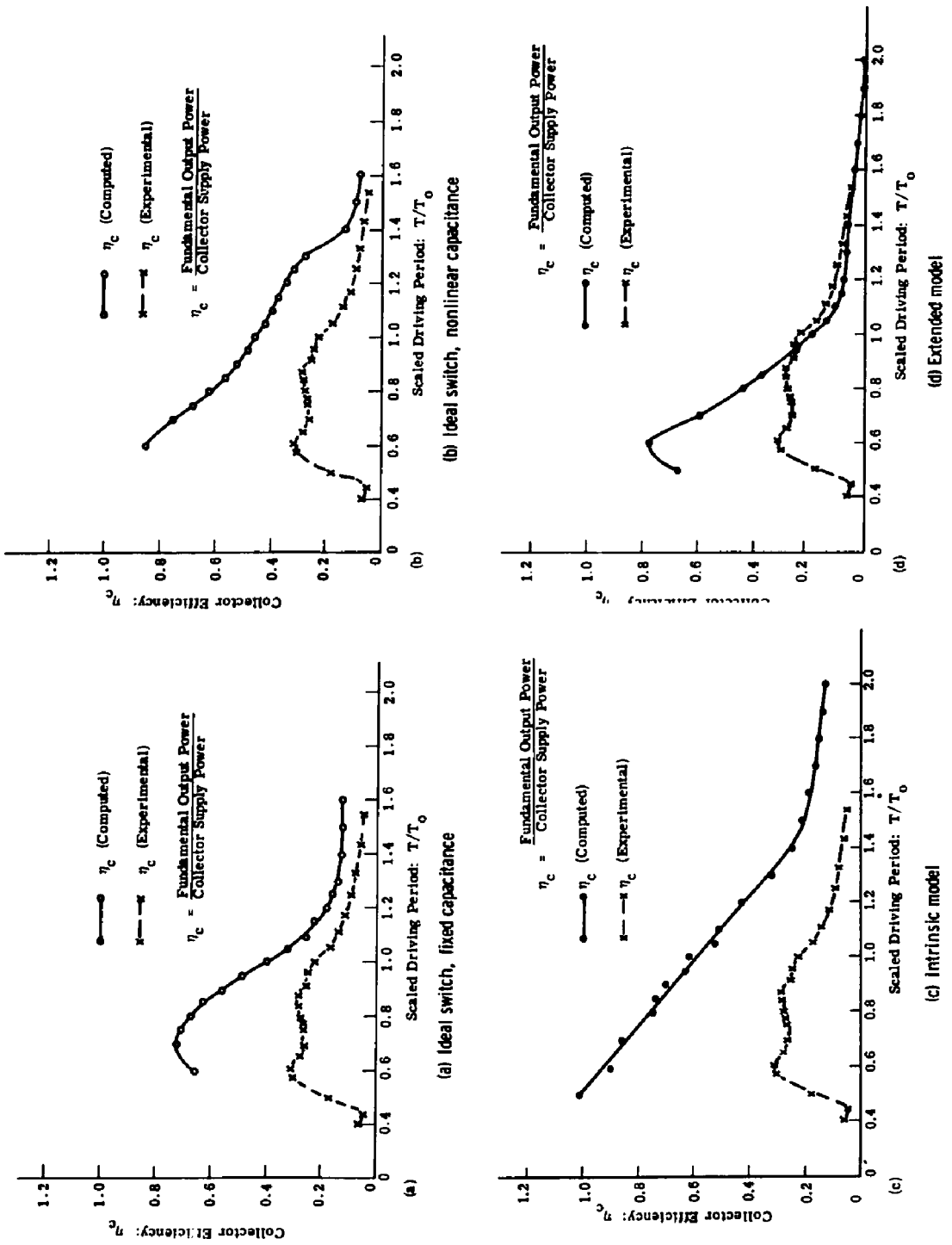


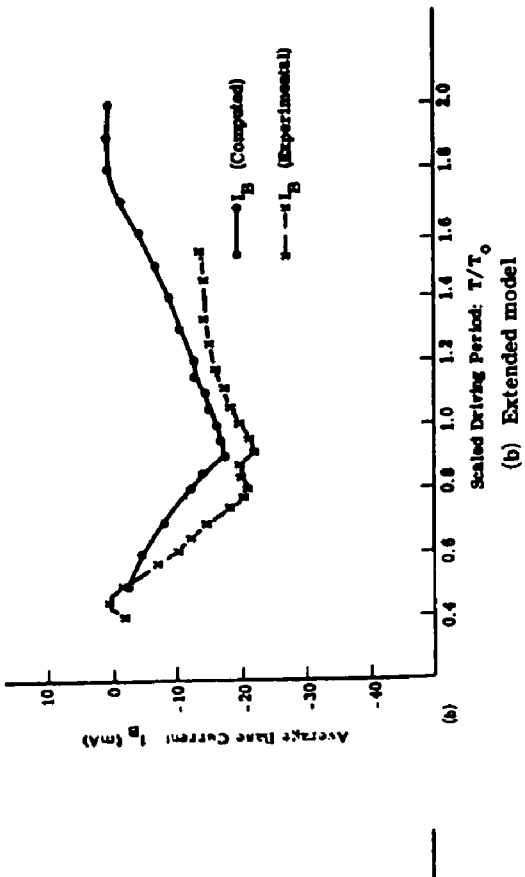
Fig. 6.13. Frequency response of efficiency

the intrinsic model.

6.4 Comparisons of Load Resistance Effects

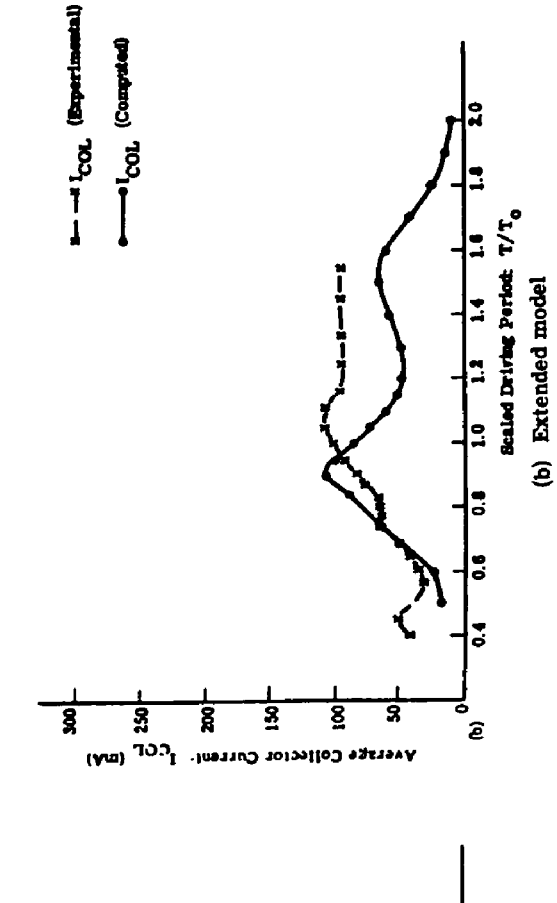
The influence of load resistance value on the amplifier output power is illustrated in Fig. 6.16. The lack of model resistance in the ideal switch and intrinsic transistor models results in predictions of increases in output power with load resistances less than 50 ohms. This deficiency is overcome with the extended model, and with the exception of the double mode predictions (Section 5.3.2), its behavior predictions very closely resemble the results obtained with the experimental amplifier (Fig. 6.16d). The dependence of efficiency on load resistance is also found to be well simulated with the extended transistor model (Fig. 6.17d).

The base current predictions obtained with the intrinsic transistor model agree with the experimental amplifier for load resistances less than 150 ohms but are unsatisfactory for larger load resistances (Fig. 6.18a). The extended model provides good simulation over the 30 to 550 ohm load resistance range (Fig. 6.18b). Average collector current computations stemming from the intrinsic model display greater fluctuation with load resistance than measured experimentally, and the computed current increases excessively with small load resistances (Fig. 6.19a). The extended model reduces the fluctuations and also provides good simulation for the entire load resistance range (Fig. 6.19b).



(a) Intrinsic model (b) Extended model

Fig. 6.14 Frequency response of base current



(a) Intrinsic model (b) Extended model

Fig. 6.15 Frequency response of collector current

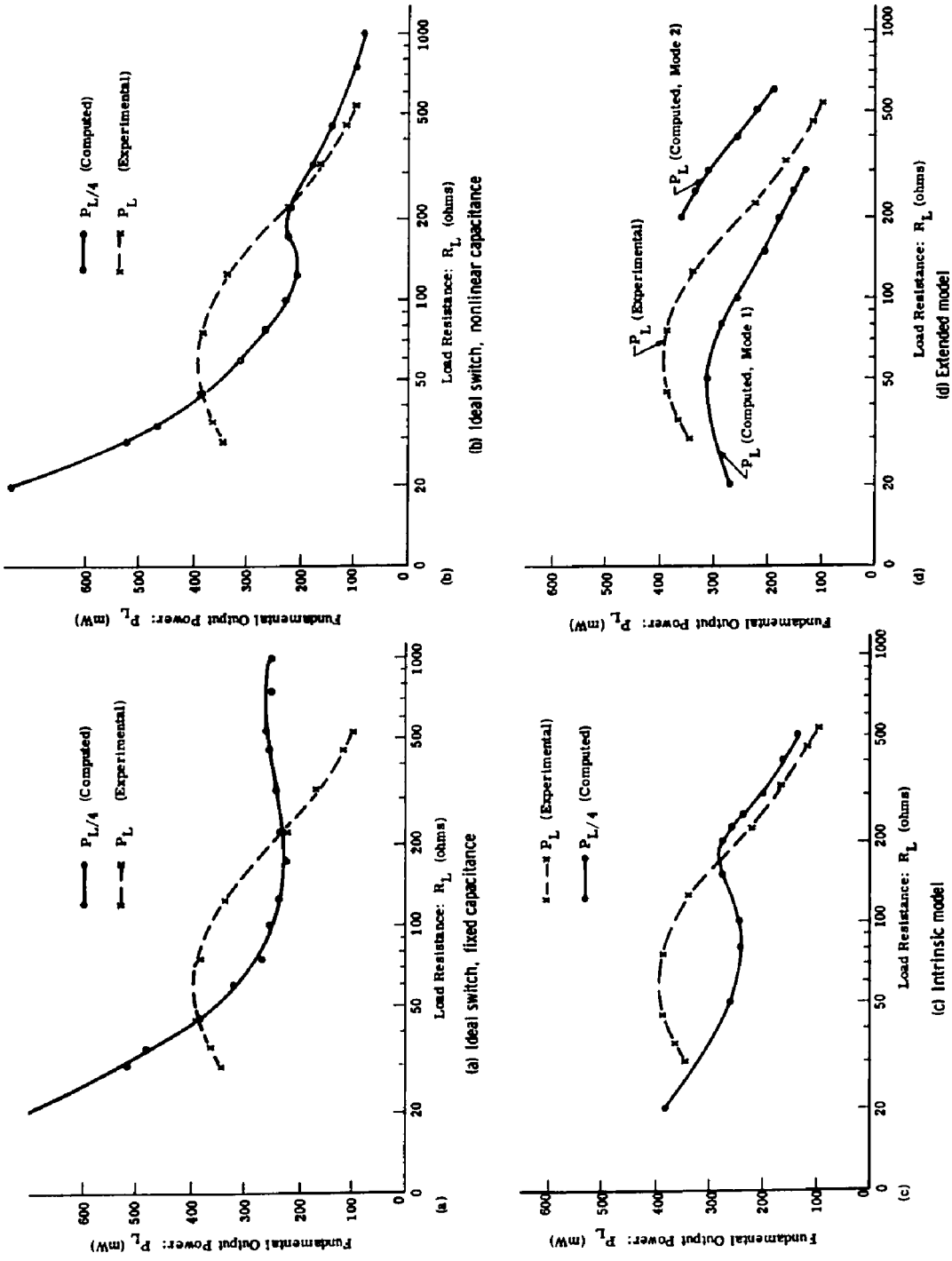


Fig. 6.16. Effect of load resistance on output power

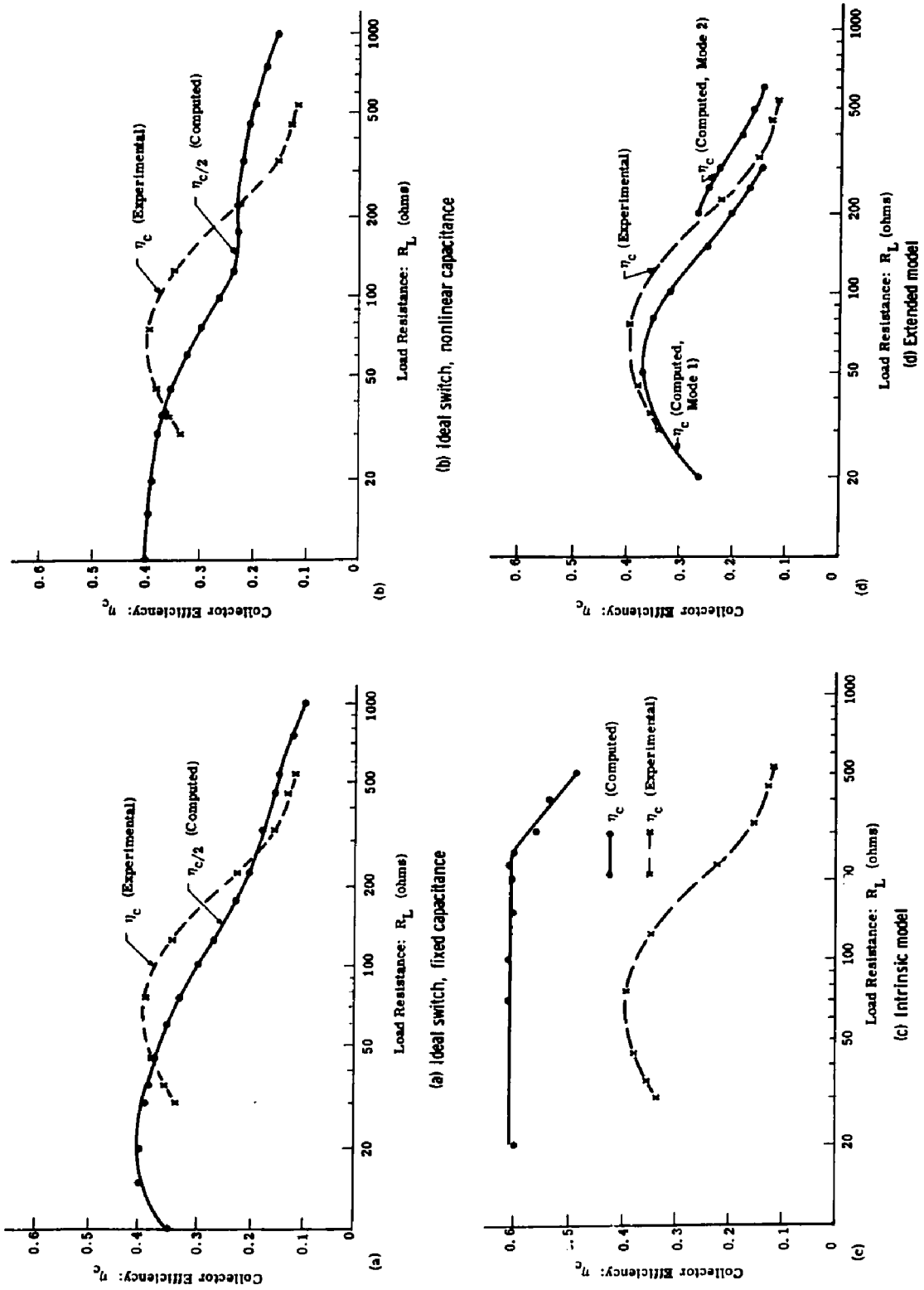


Fig. 6.17. Effect of load resistance on efficiency

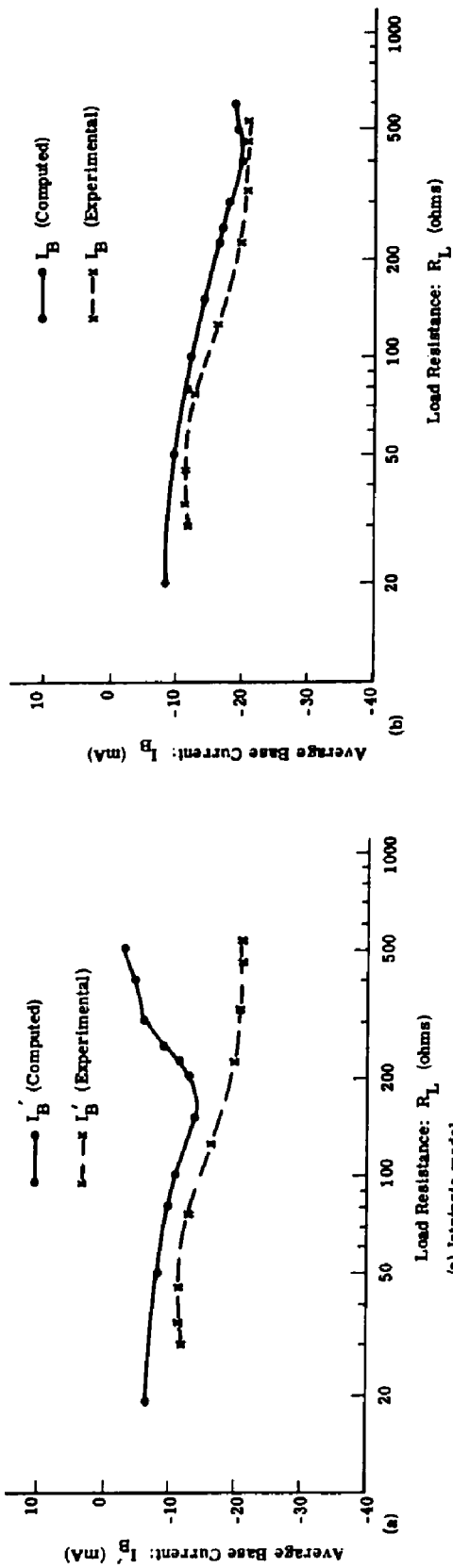


Fig. 6.18. Effect of load resistance on base current

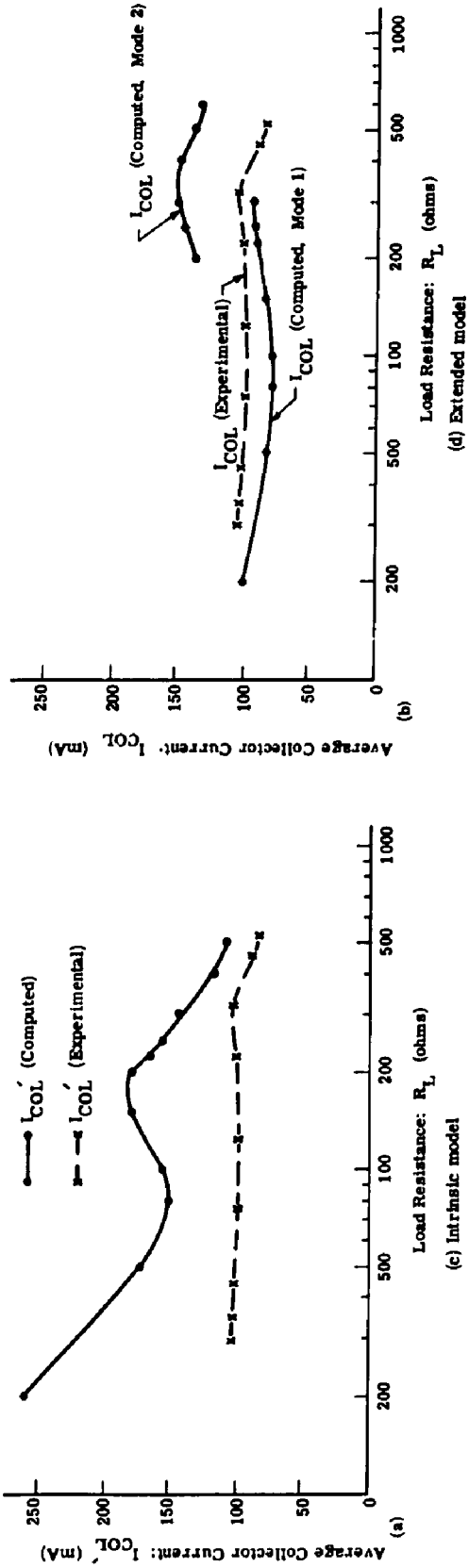


Fig. 6.19. Effect of load resistance on collector current

6.5 Comparisons of Supply Voltage Effects

When the transistor is modelled as an ideal switch with fixed output capacitance, the collector supply voltage has no effect on the computed efficiency, and the output power increases as V_{cc}^2 (Section 3.2.5). If the output capacitance is given a voltage dependency such as in Fig. 6.4, the output power no longer varies directly with V_{cc}^2 (Section 3.3). When modeling the 100 MHz amplifier as an ideal switch with nonlinear capacitance, the output power variations of Figs. 6.20a and b are predicted. For supply voltages less than 5 volts, the output power increase at a greater rate than V_{cc}^2. For supply voltages greater than 20 volts, the output power increases more slowly than V_{cc}^2; and in the range $5 < V_{cc} < 20V$ a dependency proportional to V_{cc}^2 is observed (Fig. 6.20a). In Figs. 6.20b, c, and d, the computed dependencies of output power on supply voltage are compared to experimentally measured amplifier performance. Computations involving the intrinsic model predicted output powers greater than observed experimentally as well as predicting output power proportional to V_{cc} up to 24 volts. For supply voltages greater than 24 volts, the output power computed with the intrinsic model is relatively constant corresponding to the limiting of output power by input signal power instead of supply voltage (Section 4.4.1).

The extended model simulation predicts the experimentally observed results with reasonable accuracy over the large supply

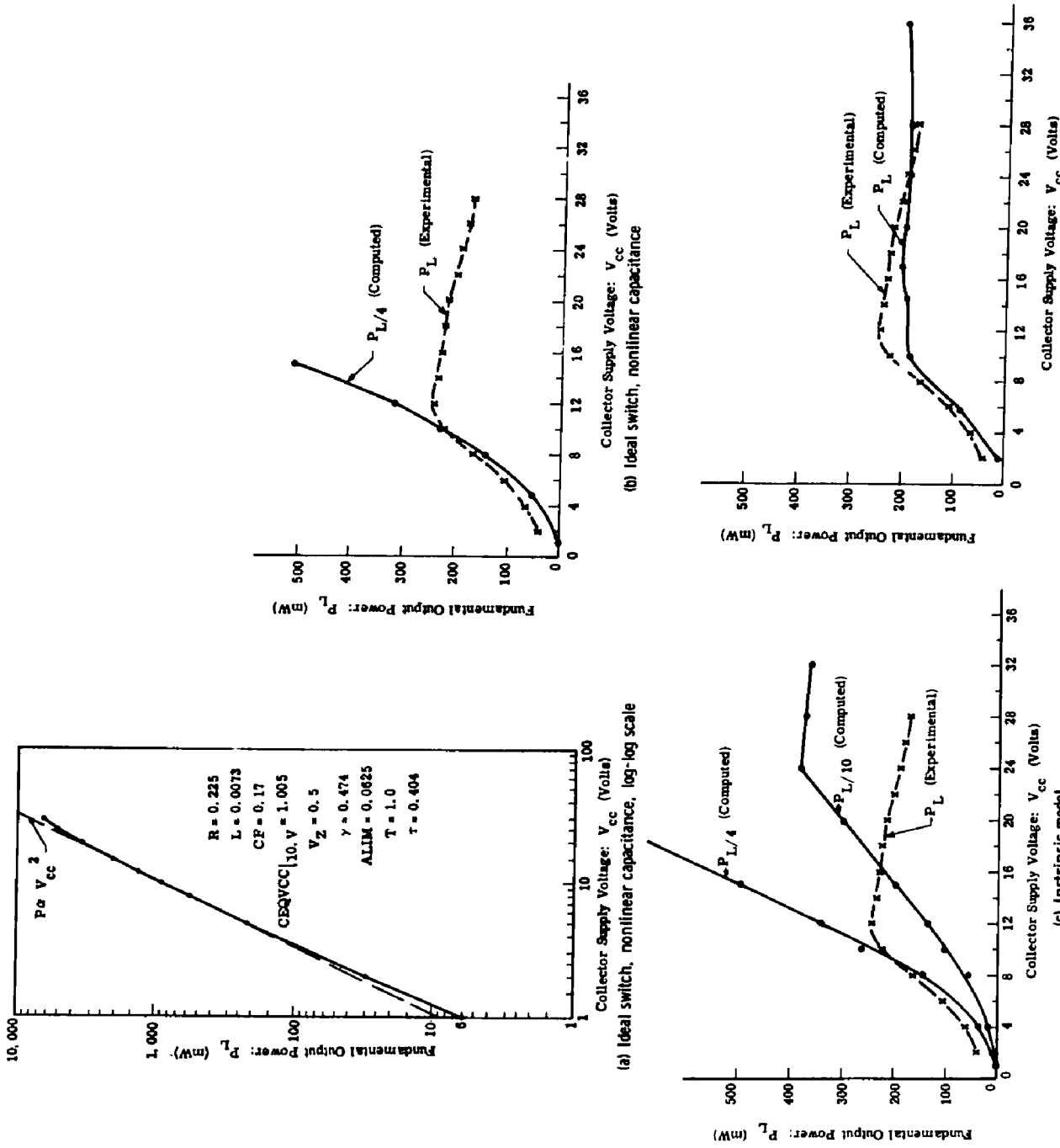


Fig. 6.20. Effect of supply voltage on output power

voltage range of 2 to 28 volts. The fact that the computed output power did not reduce for supply voltages above 12 volts as observed with the experimental amplifier, may be attributed to the fact that the computation was not performed at the frequency for maximum output power with V_{cc} = 10 volts. That is, the experimental amplifier was tuned for maximum output power with a signal frequency of 100 MHz and a supply voltage of 10 volts. Supply voltages greater than 10 volts apparently detuned the experimental amplifier slightly causing the observed decrease in output power. The simulation circuit was found to be tuned to 125 MHz for maximum power (Fig. 6.12d), and thus the detuning effect is not as noticeable when operating the simulation circuit at 100 MHz.

The dependencies of collector efficiency on supply voltage are illustrated in Fig. 6.21. The efficiencies predicted with the ideal switch and the intrinsic transistor model are twice as large as the measured efficiencies. Due to coupling of input circuit to output circuit through the transistor, it is possible to develop load power with zero collector supply voltage. Thus under conditions of small collector supply voltage it is possible for the efficiency

$$\left(\eta = \frac{P_L(1)}{P_{V_{cc}}}\right)$$

to exceed unity as predicted by the analysis with the intrinsic transistor model in Fig. 6.21b.

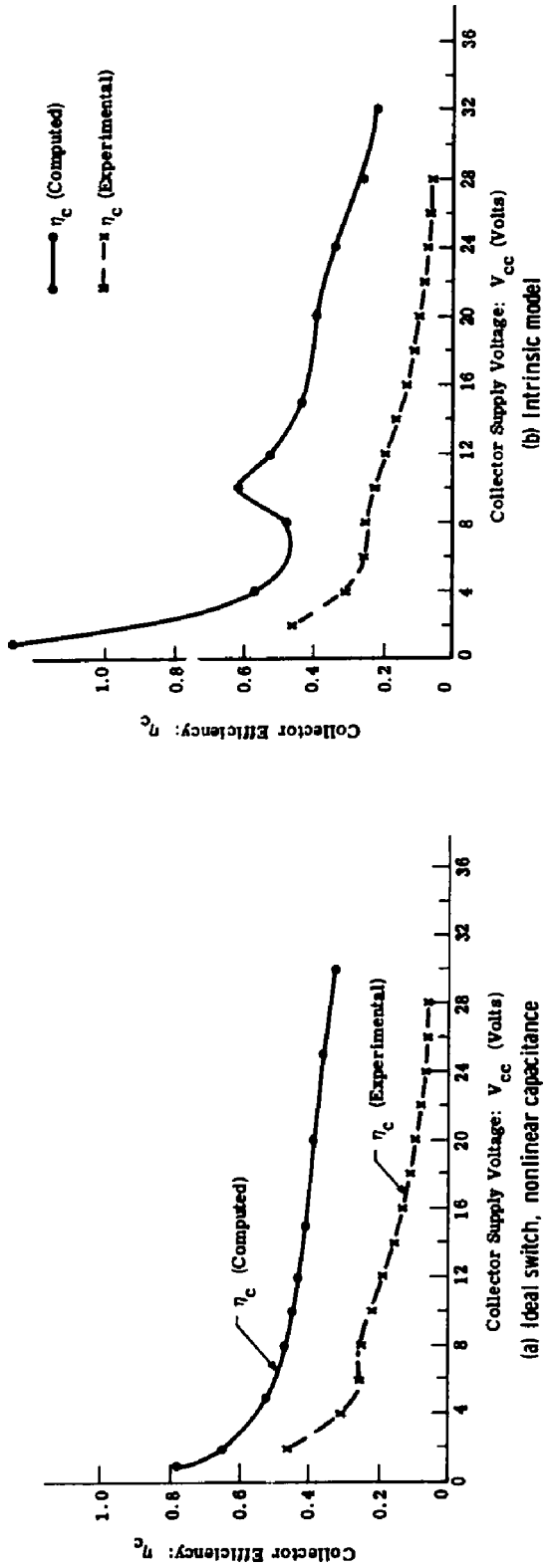


Fig. 6.21 Effect of supply voltage on efficiency

As with the load resistance variations, the base current variations with supply voltage (Fig. 6.22) are slight and are fairly well simulated by the intrinsic model for supply voltages in the range of 12 to 24 volts. The extended model offers improved simulation over the entire range of 2 to 28 volts. With the intrinsic model the calculated collector current increases linearly for V_{cc} up to 28 volts, but with the extended model and the experimental amplifier, the collector current remains relatively constant for V_{cc} greater than 10 volts (Fig. 6.23).

6.6 Computed Effects of Signal Amplitude

The effect of input signal amplitude on base and collector current, output power, and efficiency was not measured with the experimental amplifier. This behavior was computed with the intrinsic and extended transistor model simulations and the results are presented in Figs. 6.24 through 6.26 for comparison. As illustrated, the general behaviors are the same for both simulations.

6.7 Conclusions

Modeling a VHF power amplifier with the ideal switch, intrinsic, and extended transistor representations has demonstrated the necessity of the more complex extended model for achieving accurate simulations over wide ranges of operating conditions. A major deficiency of the ideal switch and intrinsic transistor models is their

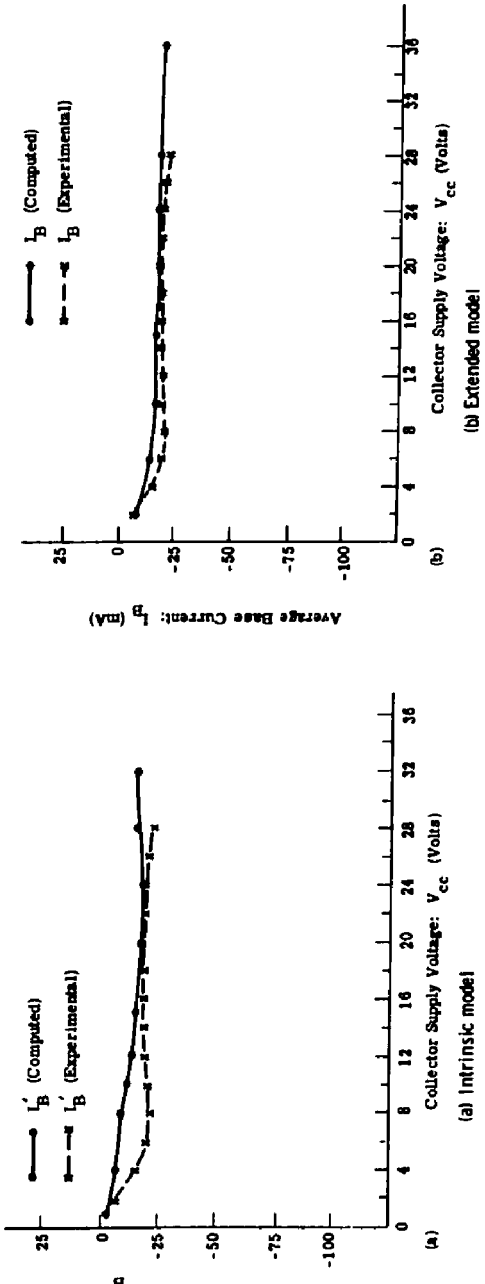


Fig. 6.22 Effect of supply voltage on base current

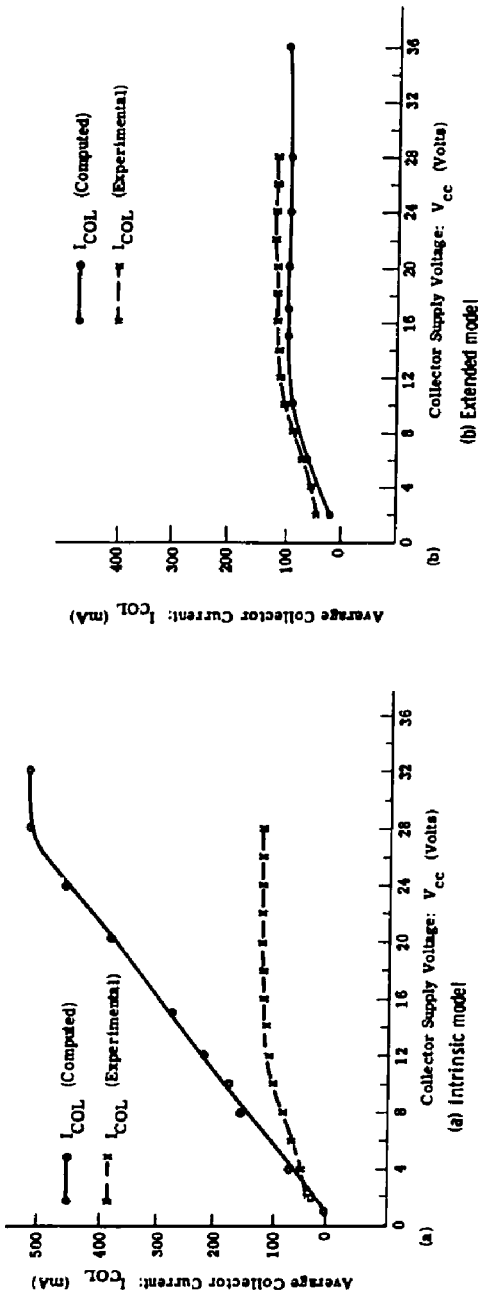


Fig. 6.23. Effect of supply voltage on collector current

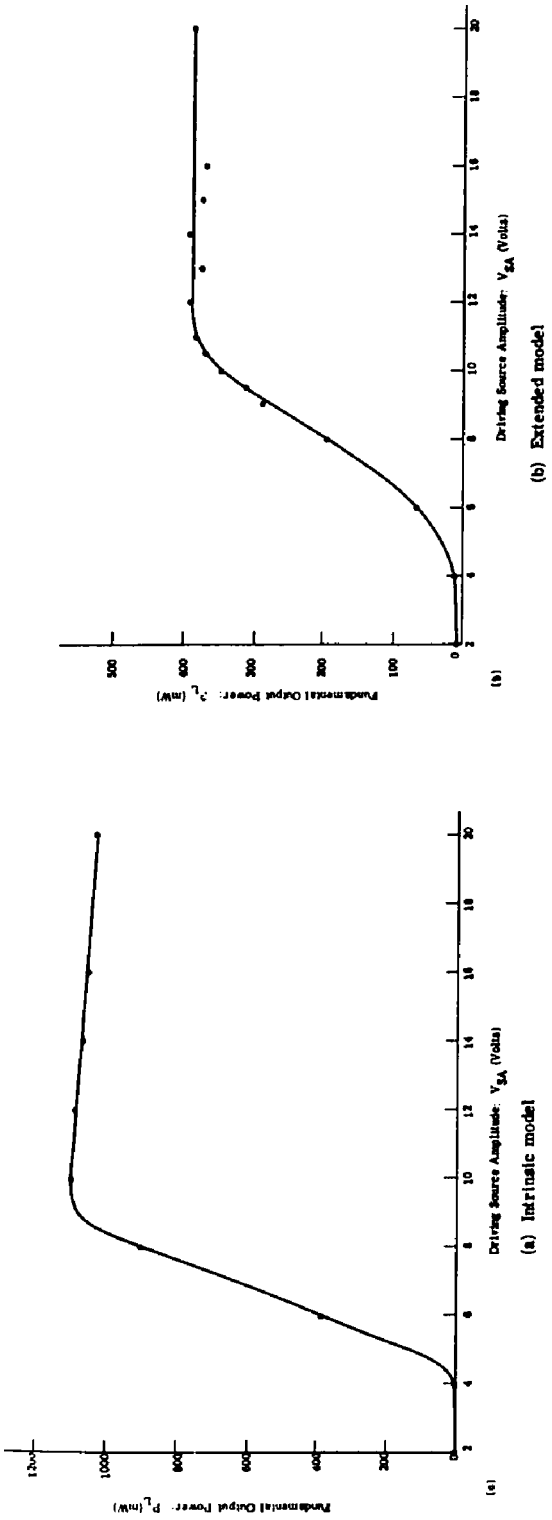


Fig. 6.24. Effect of source amplitude on output power

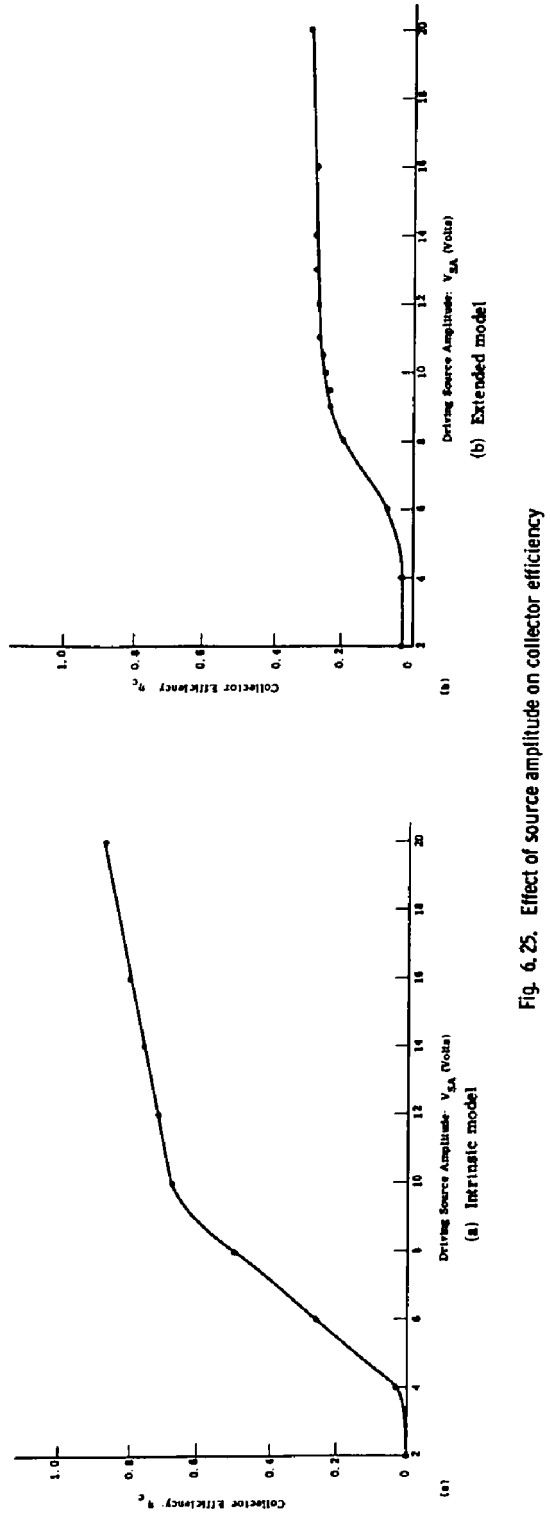
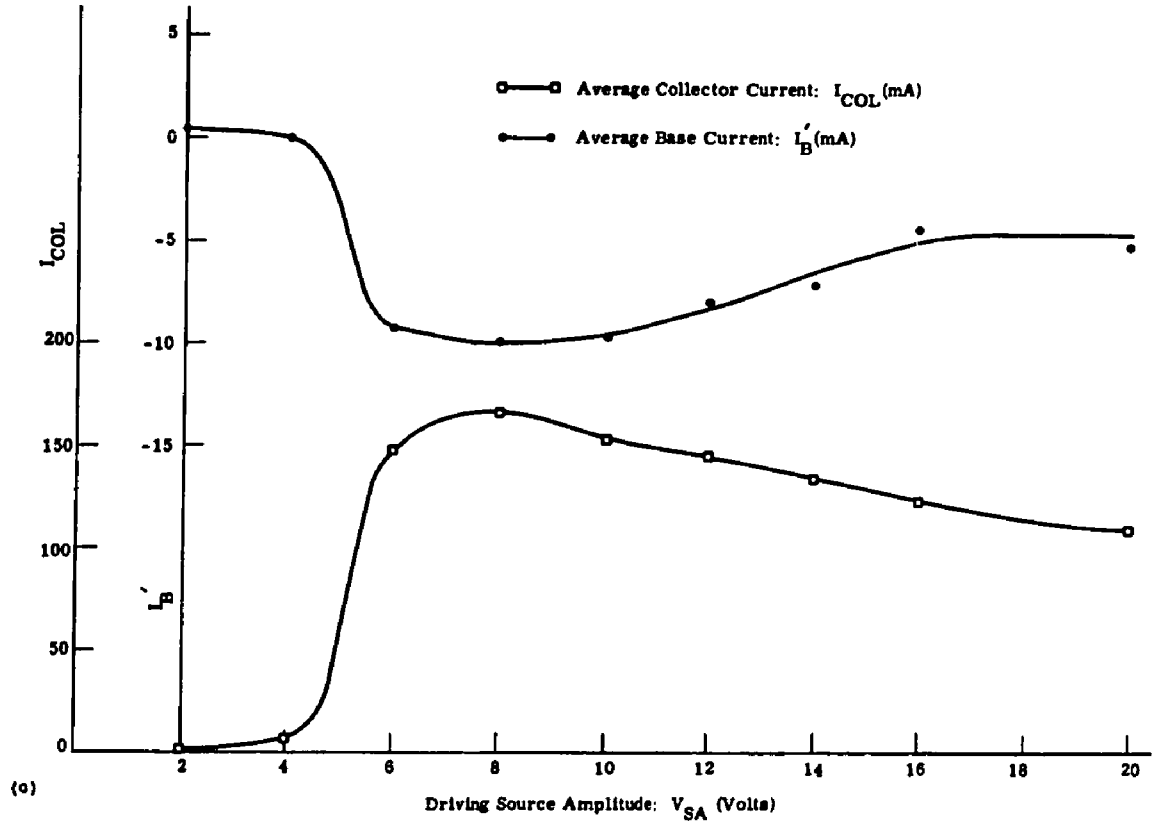
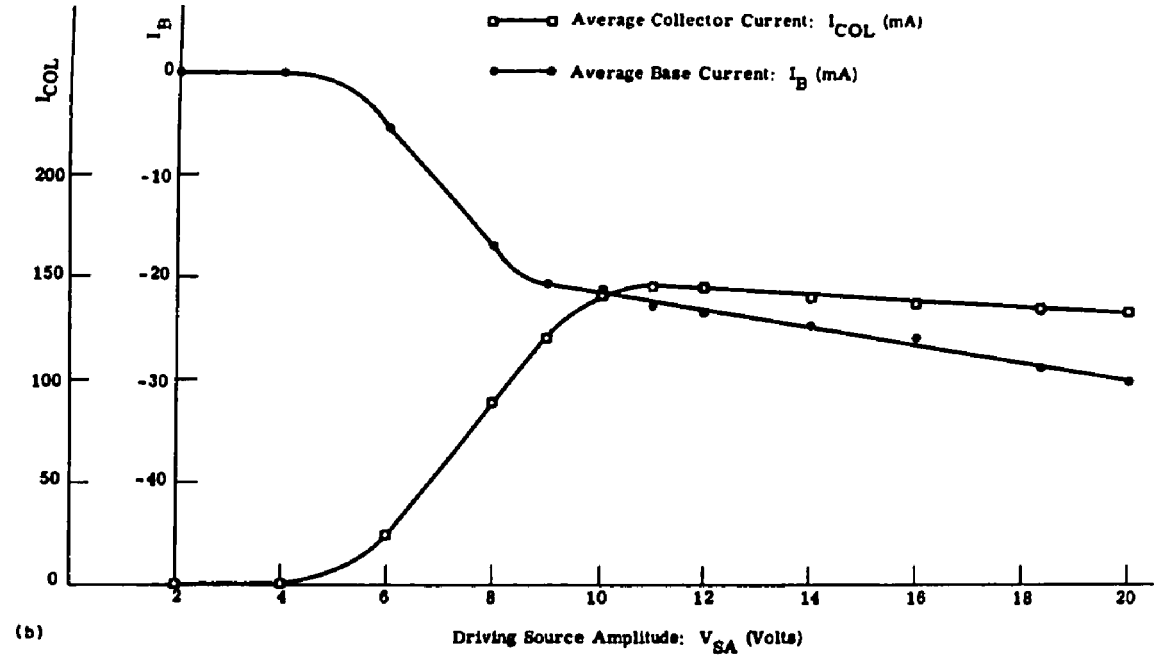


Fig. 6.25. Effect of source amplitude on collector efficiency



(a) Intrinsic model



(b) Extended model

Fig. 6.26. Effect of source amplitude on base and collector current

failure to account for resistive potential drops that occur when a transistor is in saturation for short time durations (Section 2.5.3.5). Due to insufficient output resistance, the ideal switch and intrinsic transistor simulations predict output powers and efficiencies that are larger than those measured with the corresponding experimental amplifier. In lower frequency simulations (Sections 3.5 and 4.3) and in applications with small peak collector currents, the need for a collector saturation resistance is not so strong.

The base current simulation afforded by the intrinsic transistor model is adequate for many engineering applications. However, for large load resistances, the base currents predicted with the intrinsic model do not agree with those measured experimentally (Fig. 6.18a). It has also been noted (Sections 4.4.1 and 4.6) that the internal gain of the intrinsic transistor model is unrealistically large, predicting output circuit saturation even with large supply voltages. This difficulty cannot be corrected by adding collector resistance alone. The emitter circuit elements of the extended model, L_{EE} and R_{EE}, do reduce the transistor gain, and their inclusion in the transistor model improves the simulations of supply voltage effects. Thus we may conclude that the effort required to determine values for the additional parameters of the extended transistor model is necessary to insure proper simulation of VHF power amplifiers.

CHAPTER 7

REVIEW, SUGGESTIONS, AND CONCLUSIONS

7.1 Introduction

We have used several transistor models to simulate class C/D amplifiers at low and high frequencies over wide ranges of operating conditions. The modeling procedures introduced in Chapter 2 were successfully coupled with numerical analysis techniques to investigate the essential characteristics of the transistor models as well as the characteristics of tuned power amplifiers. Effects of nonlinear capacities, avalanche breakdown, saturation resistances, and emitter inductance require complex transistor models for proper characterization. Digital computations are required for analyses when such complexities are included in amplifier simulations.

The results of computational studies of several amplifiers with the various models are summarized in this chapter. The importance of the elements of the extended transistor model were investigated in Chapter 6, and the results are reviewed in this chapter. The costs of computation with each of the models are also compared. Improvements are suggested for future use of the models, and the conclusions of the study are then summarized.

7.2 Summary of Models

7.2.1 Ideal Switch Models. The ideal switch models of Chapter 3 were found to be useful for studying class D amplifiers at low frequencies. They provided the basic transistor output characteristics in studies relating output power and efficiency to frequency (Section 3.2.1), load resistance (Section 3.2.2), conduction angle (Section 3.2.3), supply voltage (Section 3.2.5), tuning configuration (Section 3.4), nonlinear output capacitance (Section 3.3), and harmonic tuning (Section 3.5). These investigations have allowed us to examine many fundamental characteristics of tuned power amplifiers. We have observed that circuit conditions for obtaining maximum outout power are generally different than those for obtaining maximum conversion efficiency (Section 3.2.3). In some circumstances where output power is limited by transistor power dissipation or breakdown voltage, it is possible to obtain greater output power by tuning to a condition for maximum efficiency rather than direct tuning for maximum output power (Section 3.2.3).

The calculated effects of making the output capacitance of the ideal switch model nonlinear, with a moderate output circuit Q (~ 10), were not as pronounced as originally suspected. Even with 5:1 capacitance variations, over the operating period, T, the output waveforms were found to be very similar to those calculated for the fixed capacitance case. The major differences between the results

with fixed and nonlinear output capacitances were that with the nonlinear capacitance, the signal amplitudes were slightly less and the harmonic content was slightly greater.

With fixed output capacitance the ideal switch models yield output power computations predicting power that is proportional to the square of the supply voltage. However, with the nonlinear output capacitance simulations, the output power dependency does not adhere to the square law relationship (Sections 3.3 and 6.5). This variation from square law is due to the voltage dependent tuning effect of the nonlinear output capacitance.

The configurations of the input and output tuning circuits of a large signal transistor amplifier influence the way in which the harmonic voltage and current components interact. If equivalent input and output admittances for the transistor are determined by laboratory measurements on an operating amplifier (Section 1.2), the admittance values obtained will be dependent on the tuning circuit utilized. A brief look at the effect of output tuning circuit on amplifier operating characteristics such as optimum load resistance, harmonic content, and bandwidth was conducted with the ideal switch model. For moderate Q output circuits ($5 \leq Q \leq 20$), the change from parallel RLC tuning to a series RL load tuning resulted in slight increases in output power, efficiency, and bandwidth with an attendant reduction in harmonic content of the load power.

Another modification to the parallel RLC output tuning circuit that was investigates was the addition of a series LC branch that could be adjusted to short-circuit harmonic voltage components. With both the computations and an equivalent low frequency (500 kHz) laboratory experiment, the harmonic tuning network was found to increase output power at some frequencies but greatly increased the frequency sensitivity of the amplifier. It was also determined that the observed increases in output power could not be attributed to the harmonic pumping of the nonlinear output capacitance; similar increases in output power were calculated and measured when the capacitance was constant.

In general, the ideal switch simulations are adequate for class D amplifiers in which dynamic effects and saturation impedances of the transistor are negligible. Neither of these effects should be neglected in typical VHF power amplifiers, and complete characterization of such amplifiers requires more detailed transistor models.

7.2.2 Intrinsic Voltage Controlled Transistor Model. The use of an intrinsic voltage controlled transistor model allowed both input and output properties of tuned power amplifiers to be investigated (Chapter 4). Initial studies conducted with this model illustrated the need for altering the numerical computation of device terminal currents depending on the operating region of the device (Section 4.2.1). It was found to be advantageous to determine the currents from external

circuit constraints when the transistor is in saturation and from the transistor equations when the transistor is cutoff. In the active region one should determine the base current from the external circuit and the collector current from the device equations. For the inverse region, both base and collector currents should again be determined from the external circuit elements.

Preliminary computations utilizing the intrinsic transistor model showed an unexpected double-peaked collector current waveshape. An experimental amplifier was constructed for operation at 5 kHz and provided verification of the predicted waveshape. This experiment confirmed that this model was satisfactory for low frequency amplifiers* with output circuitry of moderate to high Q ($Q > 5$).

The intrinsic voltage controlled model of a 2N3866 transistor was used to simulate a 100 MHz amplifier without input tuning. At the nominal operating condition, the computed gain was approximately 30 percent greater than that measured experimentally, and the computed efficiency exceeded the experimental efficiency by 8 percent. The frequency response predictions were similar in shape to those

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*By "low frequency amplifier" we imply that the time constants associated with the transistor are much smaller than those associated with the passive tuning circuitry so that the dynamic response is essentially determined by the passive tuning elements. For convenience, we may use $f \leq f_T/10$ as a definition of "low frequency" where f is the operating frequency of the amplifier and f_T is the current-gain-bandwidth product of the transistor.

measured; the computed frequency for maximum power was 8 percent lower than that measured, and the computed frequency for maximum efficiency was 40 percent higher than measured. The computed and measured effects of supply voltage were in agreement for voltages less than 15 volts. For higher voltages the experimental amplifier was not driven into saturation, but the simulation erroneously predicted that saturation continued over the computational supply voltage range of 2 to 24 volts. Over the range of load resistances considered (20 - 550 Ω), the output power behavior was predicted correctly only for resistances greater than 100 Ω . For the smaller resistances the model did not properly simulate the device losses.

The general conclusion reached with the intrinsic model studies was that the model is suitable for simulation of low and high frequency tuned power amplifiers ($f \leq f_T/4$) in which computational accuracies of 30 percent are acceptable. In addition, the accuracy can be severely degraded (see Fig. 4.9) if the output circuit Q is low ($Q < 2$) or if the range of external circuit parameters is large. The model should be modified if such conditions are not satisfied.

7.2.3 Extended Voltage Controlled Transistor Model. An extended voltage controlled transistor model was used in Chapter 5 to investigate its ability to provide improved characterization of VHF power amplifiers. It has been demonstrated that the extended model is capable of simulating a high frequency (50 - 200 MHz) class C

amplifier adequately for wide ranges of operating conditions and was found to be superior to the other models for this simulation (Chapter 6).

In addition to using the extended model to predict the behavior of a VHF amplifier, it was used to study the sensitivities of several of the amplifier performance characteristics (output power, efficiency, base current, and collector current) to changes in external circuit and model parameters (Table 5.1). We can use the information from this study to estimate the importance of each model parameter and the accuracy to which each parameter should be determined for future simulations. For example, averaging the magnitudes of the sensitivities of the output power, efficiency, average base current, and average collector current given in Table 5.1 leads to a simplified tabulation (Table 7.1). In Table 7.1 the parameters are listed in order of decreasing sensitivity and are arbitrarily separated into four groups for comparison. We observe that the first group is largely composed of the external circuit parameters. Of the transistor parameters in that group (α_F, R_{BB}, V_A, λ), the base resistance, R_{BB}, should be considered the most significant since α_F is actually determined from a β_F measurement and β_F is in a less sensitive Group 4. Values for V_A and λ can be determined with reasonable precision by simple static measurements leaving R_{BB} as the most serious modeling task for accurate simulation. The value used for the amplifier representation ($R_{BB} = 22.45\,\Omega$) was established in Section

Parameter	Averaged Sensitivity	Sensitivity Group
α_F	3.85	
VSA	2.42	
T	1.66	
R_{BB}	1.52	
VSDC	1.44	
VA	1.43	1
R_S	0.968	
C_L	0.949	
L_L	0.831	
λ	0.792	
V_{CC}	0.498	
R_L	0.422	
LS	0.382	2
R_{CC}	0.342	
CJE	0.314	
τ_F	0.309	
CJC	0.190	
α_R	0.186	
R_{EE}	0.179	
γ_E	0.173	
τ_R	0.166	
Q_{FS}	0.165	3
Q_{RS}	0.161	
VZE	0.145	
L_{EE}	0.144	
γ_C	0.142	
C_S	0.131	
CCE	0.107	
CFC	0.103	
CCB	0.0942	
ACLIM	0.0874	
AELIM	0.0795	
NA	0.0779	4
CFE	0.0776	
VZC	0.0568	
β_R	0.0508	
β_F	0.0462	
CBE	0.0278	

Table 7.1. Averaged sensitivities

2.5.3.7 but was estimated very closely ($R_{BB} = 20.0\,\Omega$) in Section 2.5.3.1. Assuming that $22.45\,\Omega$ is the better value for R_{BB}, the $20.0\,\Omega$ estimate is 10.9 percent too low; and from Table 7.1 we find* that utilization of the estimated value could lead to "average" computational errors of 16.7 percent. Thus, determination of R_{BB} value requires close attention for accurate simulations.

The elements in Group 2 are equally split between external circuit and transistor parameters. The amplifier sensitivities to these transistor parameters (R_{CC}, C_{JE}, τ_F) imply that amplifier simulation accuracies of 5 percent can be provided by determining the Group 2 element values to a 15 percent accuracy. The measurement techniques suggested for evaluating R_{CC} (Section 2.5.3.7), C_{JE} (Section 2.5.1.4), and τ_F (Section 2.3.2) are satisfactory for providing this level of accuracy. The relatively small sensitivities to the parameters in Groups 3 and 4 suggest that these values can be estimated from a knowledge of device size and geometry without the necessity of laboratory measurements.

Consideration of the intended transistor application is of course required to assess the true importance of each model parameter. For example, in many applications, input drive and collector tuning conditions will preclude the possibility of emitter-base avalanche. In such

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*From Section 5.4,

$$\%\ \text{error in}\ f = S_p^f \times \%\ \text{error in}\ p$$

applications, the computed performance is clearly insensitive to the avalanche parameters, and those elements need not be included in the model. The low sensitivity to the depletion capacitance parameters with both the extended model studies and the ideal switch studies with output Q's on the order of 10 suggests that their nonlinear behavior need not be simulated closely and that they may be replaced with fixed capacities representing the total depletion capacitance occurring at the average junction potential.

7.3 Computational Costs

The decision to make digital simulations of a power amplifier is influenced by the availability and computational costs of suitable transistor models. Our experience with the models investigated suggests that a large model such as the extended voltage controlled model is capable of predicting amplifier behavior more accurately than the smaller models, although the smaller models are satisfactory in many situations. Accuracy considerations alone may not be enough for deciding which model to choose for an analysis. Analysis with the larger models is computationally more expensive than with the smaller models. Also, for example, the difficulty of determining the extrinsic elements values of the extended transistor model makes this model undesirable for low frequency, high Q applications in which the extrinsic elements will have little effect on the predicted amplifier behavior.

The computational analysis technique of this study (Section 3.2, Appendix C) employs numerical iteration to establish the limit cycles of the various amplifier circuits. The number of iterations required is dependent on the proximity of the estimated initial conditions to the correct limit cycle values, the time constants of the passive circuits, and the operating conditions; however for the particular VHF amplifier simulated, there were no observable differences in the convergence rates of the various simulations. Figures 7.1 and 7.2 illustrate convergence behaviors that are typical of all the simulations with the various models. These figures show the number of iterations required in the analysis with the extended model as the driving period and load resistance were varied in discrete steps. Interpretation of the plots is explained by the following example:

In moving from a driving period of 1.4 to 1.5 (Fig. 7.1), the final limit cycle conditions for the T = 1.4 solution were used as the estimate for the initial conditions in the T 1.5 analysis. With this estimate, 5 iterations were required to achieve convergence* to the

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*The convergence criteria for this analysis was defined as:

$$\sum_{j=1}^{7} \left(x_{F_j} - x_{I_j} \right)^2 \leq 0.007$$

where x_{I_j} = The value of the jth state variable at the beginning of the period.

x_{F_j} = The value of the jth state variable at the end of the period.

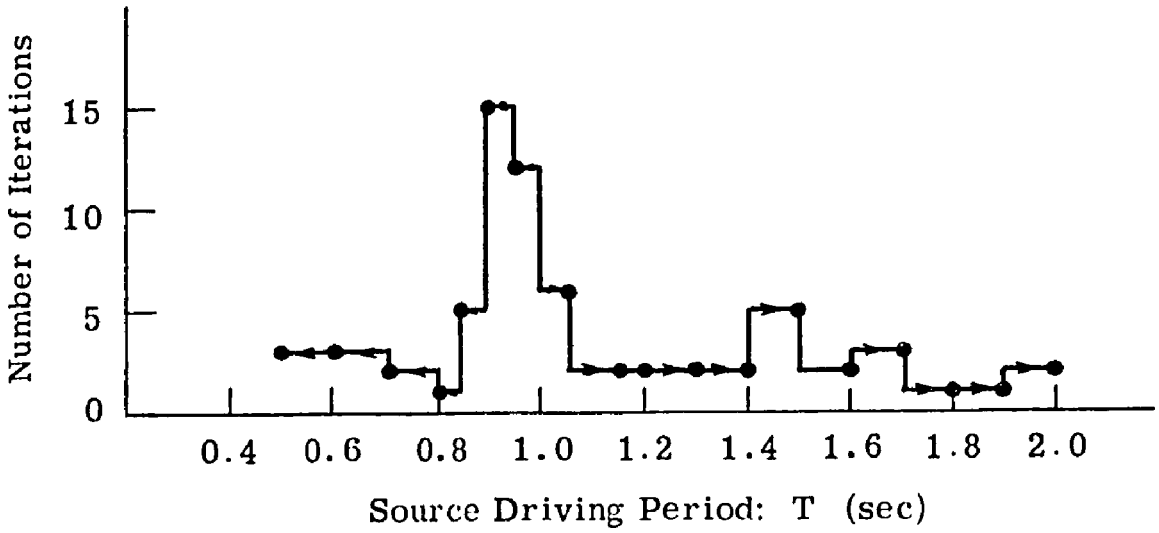

Fig. 7.1. Convergence behavior with changing excitation period

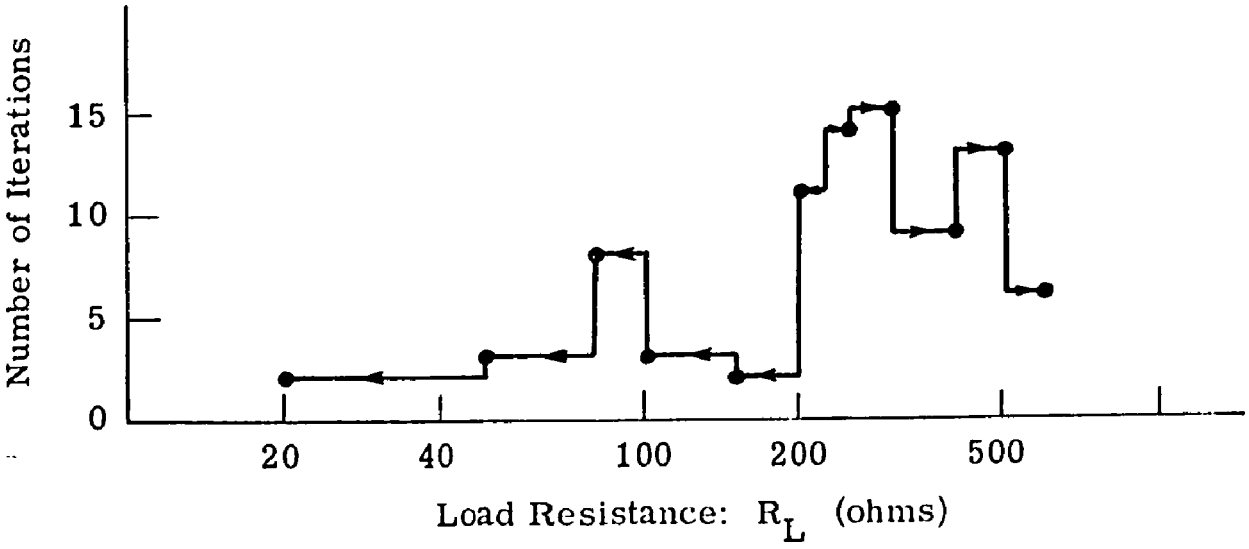

Fig. 7.2. Convergence behavior with changing resistance

$T = 1.5$ limit cycle.

It is not practical to compare total computation times of the different simulations because the total number of iterations vary in the unpredictable manner illustrated in Figs. 7.1 and 7.2. From the analyses performed, all of the simulations exhibited similar nondeterministic convergence characteristics. However, as an overall average, each of the simulations was found to require about the same number of iterations for convergence. Thus, in comparing computational costs, it is reasonable to compare the time per iteration of each simulation instead of the total times. The computation time required for each iteration is dependent on the operating conditions of the amplifier, but over the ranges of this study (e.g., $20 \leq R_L \leq 550$, $\frac{T_0}{2} \leq T \leq 2T_0$, $2 \leq V_{CC} \leq 30$), the machine time required per iteration can be estimated for each model as:

Transistor Model	CPU Time, Cost/Iteration*
Ideal Switch, Fixed Capacitance	0.5 Sec, 4¢
Ideal Switch, Nonlinear Capacitance	0.5 Sec, 4¢
Intrinsic Voltage Controlled	2.0 - 3.0 Sec, 17¢ - 25¢
Extended Voltage Controlled	4.0 - 5.0 Sec, 33¢ - 42¢

*These figures are based on speed and present costs of the IBM 360/67 system used in this study at The University of Michigan.

The ideal switch representations were described by a second order system of differential equations; whereas the intrinsic and extended model representations required third and seventh order systems respectively. The computation time appears to be roughly proportional to the order of the system of equations with some dependence on the complexity of the differential equations. We can estimate that an analysis with the extended transistor model will be about ten times as expensive as a corresponding analysis with the ideal switch representations and twice as expensive as with the intrinsic model. Thus it is desirable to use the smaller models whenever such models provide sufficient accuracy. The decision of model size to be selected for adequate accuracy is often difficult. If several models are available, an effective way to check accuracy is to compare computed results with all the models using operating conditions at the extremes of the desired ranges of investigation. Given that several of the models predict the same amplifier behavior within desired tolerance limits, then the appropriate model for the investigation is taken as the simplest of those predicting the same behavior. Table 7.2 is provided as a guide to the choice of transistor model, however, the circuit designer/analyst is still faced with the task of selecting the appropriate model for each application.

Type Circuit To Be Analyzed	Suggested Transistor Model
Output Tuning and Matching Networks $Q > 5, \quad f < f_T/10$	Ideal Switch
Class C Amplifier $f \leq f_T/4$ $Q > 2$ Accuracy ~ 30%	Intrinsic Model
Class C Amplifier $f \leq f_T/4$ $.5 \leq Q \leq 20$ Accuracy ~ 20%	Extended Model With Fixed Depletion Capacities and Without Case Capacities
Class C Amplifier $f \leq f_T/2$ $.5 \leq Q \leq 20$ Accuracy ~ 10%	Extended Model

Table 7.2. Guide to model selection

7.4 Improvement to Ideal Switch Models

The ideal switch models of transistor output characteristics do not provide for device power loss during saturation. As a result, output power and efficiency predicted by computations utilizing the ideal switch models were larger than those observed with experimental

amplifiers. The departure of computed results from experimental results was particularly evident in situations yielding high switch currents. In these situations the addition of a series output resistance to the switch model would be helpful to account for device losses during saturation. Although not tried in this study, such an addition does not increase the order of the corresponding system of equations and thus should improve the modeling capability with only a slight increase in computational effort.

7.5 Improvements to Intrinsic Model

As with the ideal switch models, the addition of a series collector resistance to the intrinsic voltage controlled transistor model would improve the simulations of the saturation characteristics. This collector resistance should be added to amplifier simulations in which the transistor is expected to be driven into saturation during portions of the operating cycle.

7.6 Improvements to Extended Model

The extended voltage controlled transistor model was capable of simulating the behavior of a VHF amplifier with reasonable accuracy (Chapter 5). Of course, this model could be enlarged to include higher order effects for improved accuracy. For example, a one-lump approximation to the diffusion equation has been used as the basis for the transistor models of this study. Higher order approximations, as

suggested in Ref. K1, could be utilized. The parameters of such multi-lump models can be estimated by physical principals with a knowledge of device geometry, doping profiles, and construction techniques. Such information is seldom available and techniques for extracting the model parameters from experimental measurements are desirable.

The extended voltage controlled model can be improved without much additional effort. A base lead inductance value was established in Section 2.5.4, and this element can easily be added to the model. The nonlinear depletion capacitances are distributed along the junctions. Instead of representing these capacities as single elements across each junction, they can be conveniently split into two capacities--one across the active junction and one outside the extrinsic base resistance (Fig. 7.3). The ratio of the two portions of the depletion capacities is suggested by device geometry. A photomicrograph of a 2N3866 transistor is illustrated in Fig. 7.4a. Recalling the high frequency current distribution in the 2N3866 (Fig. 2.26b), we can associate a portion of the depletion capacitance with the active part of a junction and the remainder with an inactive part. For a 2N3866, the ratio of the inactive to active areas of the collector-base junction is approximately the same as the ratio of the base area to the emitter area as viewed from the surface of the planar device (Fig. 7.4b). For a 2N3866 we estimate

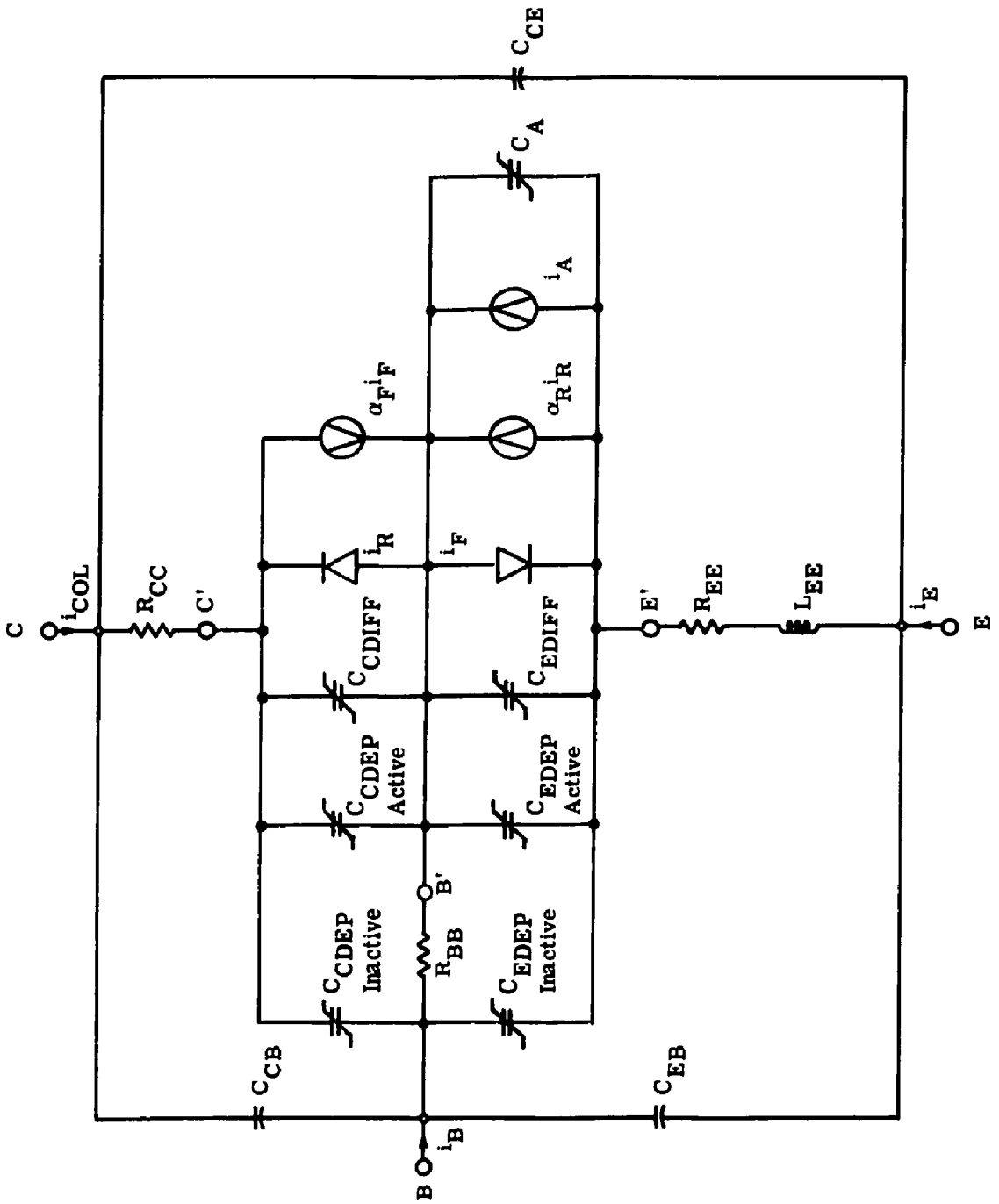

Fig. 7.3. Model with split of depletion capacities

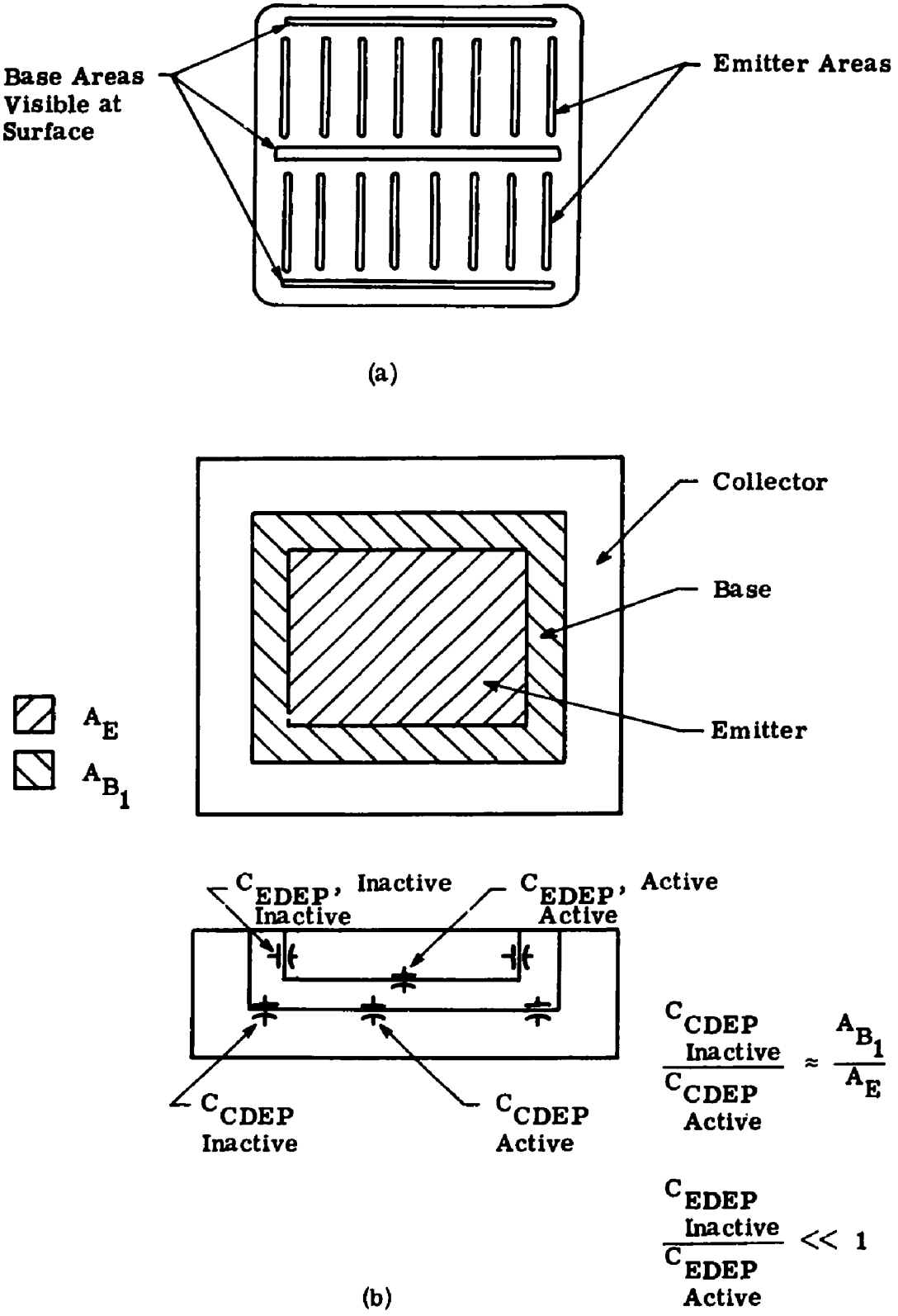

Fig. 7.4. (a) Photomicrograph of 2N3866 before metallization (from Ref. C4)
(b) Example for estimating capacitance split by surface areas of planar device

$$\frac{C_{CDEP_{INACTIVE}}}{C_{CDEP_{ACTIVE}}} \approx \frac{A_{B_1}}{A_E} \approx 3 - 4 \ ,$$

and we can split the collector depletion capacitance (Section 2.5.1) accordingly.

For the emitter-base junction, the area outside the active portion depends on the diffusion depth of the emitter and is much smaller than the active area. Therefore,

$$\frac{C_{EDEP_{INACTIVE}}}{C_{EDEP_{ACTIVE}}} << 1 \ ,$$

and the emitter depletion capacitance need not be separated into two parts.

A capacity from collector to emitter may also be added to the model. This capacitance is expected to be independent of the junction potentials. Its value can be determined from small-signal, low-frequency measurements in a manner analogous to the method used for determining the three terminal inductances (Section 2.5.4).

The dependence of α_F and α_R on junction potentials and terminal current is measured routinely (Section 2.3.1). Instead of approximating α_F and α_R as constants, their behaviors may be represented by polynomial expressions determined from the

experimental data or may be stored in tabular form for the numerical calculations. Another alternative is to employ an expandable representation as suggested by Ref. G5.

Many extensions to the electrical model of the transistor in its package are possible (Ref. H4). The necessity of each model element depends on operating frequency, signal amplitudes, and methods of operation.

7.7 Amplifier and Device Optimization

The ability to analyze tuned power amplifiers numerically provides a potential for applying numerical optimization methods to improve operating characteristics. Constrained optimization of external circuit elements and bias conditions is a desirable extension of the analysis methods developed in this study. We can also consider optimizing device characteristics. Since many device parameters are interrelated, transistor design involves many compromises in these parameters. For those device relationships that can be approximated mathematically, an optimum device can be designed for desired power levels and frequency ranges. Such optimizations are indeed desirable; however, the actual optimization technique requires careful consideration. Suppose, for example, that the numerical optimization procedure (e.g., Fletcher-Powell, Ref. F1) requires gradient computations in order to minimize some chosen amplifier performance function. The number of directional components of the gradient is equal to

the number of parameters to be adjusted. Each gradient component can be determined by independent perturbation of each of the parameters. For each perturbation one or more analysis iterations will be required to establish the perturbed limit cycle. After the gradient is established, the performance function must be repeatedly evaluated as the parameters are varied to achieve a minimum. A total computation time for such a procedure can be estimated roughly as:

$$\text{CPU Time} \geq \left[\begin{array}{c}\text{Number of Optimizer Iterations}\end{array}\right] \times \left\{\left[\left(\begin{array}{c}\text{Time For One Amplifier Analysis Iteration}\end{array}\right) \times \left(\begin{array}{c}\text{Number of Iterations To Establish Limit Cycle}\end{array}\right)\right] \times \left[\left(\begin{array}{c}\text{Number of Parameters Or Gradient Components}\end{array}\right) + \left(\begin{array}{c}\text{Number of Function Evaluations During Parameter Variation}\end{array}\right)\right]\right\}$$

$$\approx \left[20\right] \times \left\{\left[(5\ \text{sec}) \times (2)\right] \times \left[(5) + (10)\right]\right\}$$

$$\approx 3000\ \text{sec} = 50\ \text{min} \gtrapprox \$250.00$$

Such computation time requirements are large, and alternative techniques are desirable. The ability to determine network sensitivities to all adjustable parameters with only two analyses, one for the original network and one for an adjoint network, plus a back substitution may provide an alternative optimization method (Ref. D1). However, such methods become quite complex for nonlinear dynamic circuits and may not be practical for this application. In any case, numerical optimization of tuned power amplifiers is desirable, but implementation of optimization methods will require a large effort.

7.8 Conclusions

This study of tuned power amplifiers required the development of suitable transistor models and experimental techniques for determining the model parameters. These models have been successfully coupled with numerical analysis methods to study many characteristics of tuned power amplifiers.

The use of digital computations has removed the need for many assumptions (low frequency, high Q, sinusoidal potentials, no saturation, no extrinsic model parameters, zero or constant depletion capacitance, no avalanche breakdown, etc.) which have limited previous analyses. These assumptions are generally not valid for VHF power amplifiers. Although the costs of the modeling process and the digital computations can be appreciable, they are necessary for typical problems involving design, analysis, and optimization of VHF power amplifiers.

APPENDIX A

EXPERIMENTAL MEASUREMENT OF CHARGE PARAMETERS

The method used for determining the forward and reverse charge time constants of a transistor, τ_F and τ_R, was outlined in Section 2.3.2. The technique for determining τ_F requires measurement of transient base and collector currents resulting from an emitter excitation. The base current is measured by monitoring the potential developed across a small resistor, R_b, inserted in the base circuit (Fig. A.1). For accurate measurements the collector-base potential must be held relatively constant; therefore, R_b should be small enough for the developed base potential to remain much less than the collector potential. For collector potentials on the order of a few volts, the base potential must be limited to a few millivolts. In the experimental procedure used, R_b is provided by the 50 input impedance of a sampling oscilloscope. The capabilities of the sampling scope provide the key to the charge measurement. The scope is required to monitor base potentials of a few millivolts in amplitude and a few nanoseconds in duration (Fig. A.2); such performance is well within the capabilities of most sampling scopes. However, the greatest advantage in using a sampling oscilloscope to monitor the base voltage is its ability to provide an output voltage that is a time and amplitude scaled replica of the base voltage. Because of the

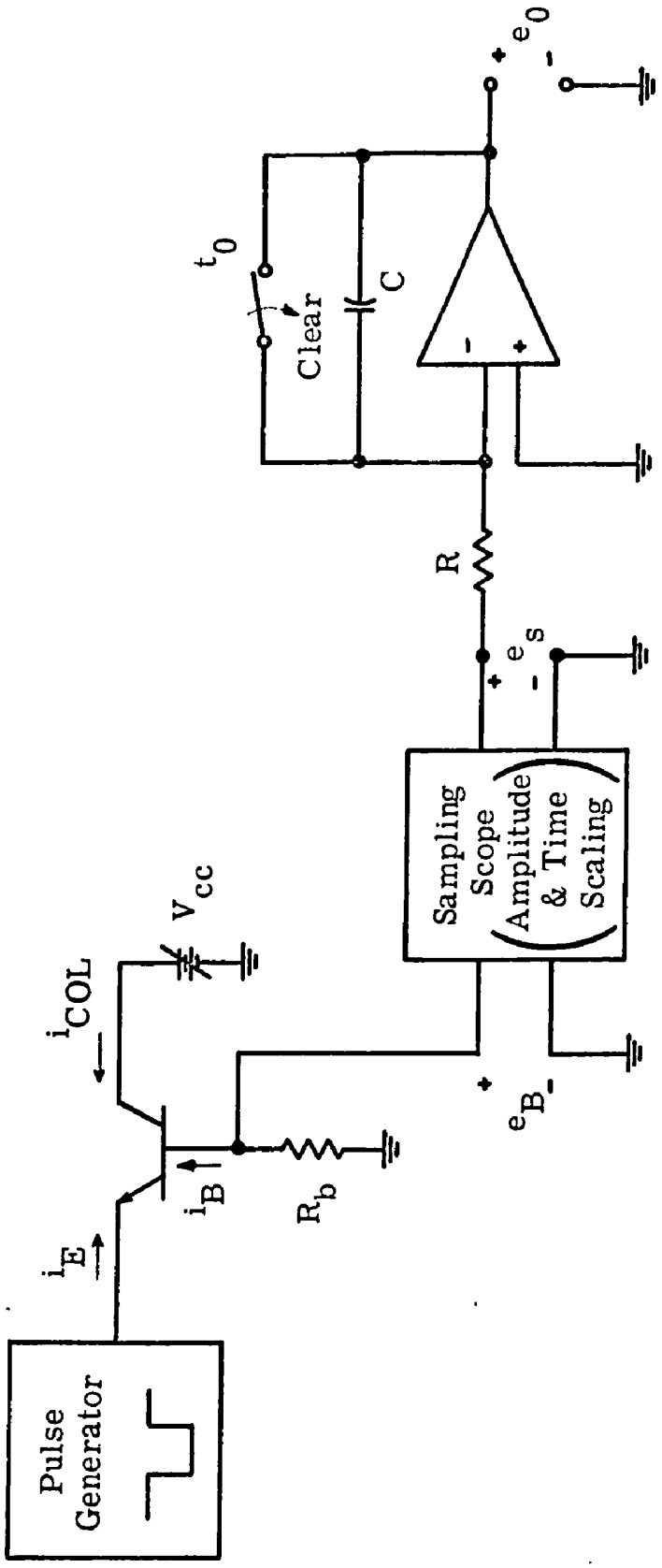

Fig. A.1. Basic circuit for charge storage measurement

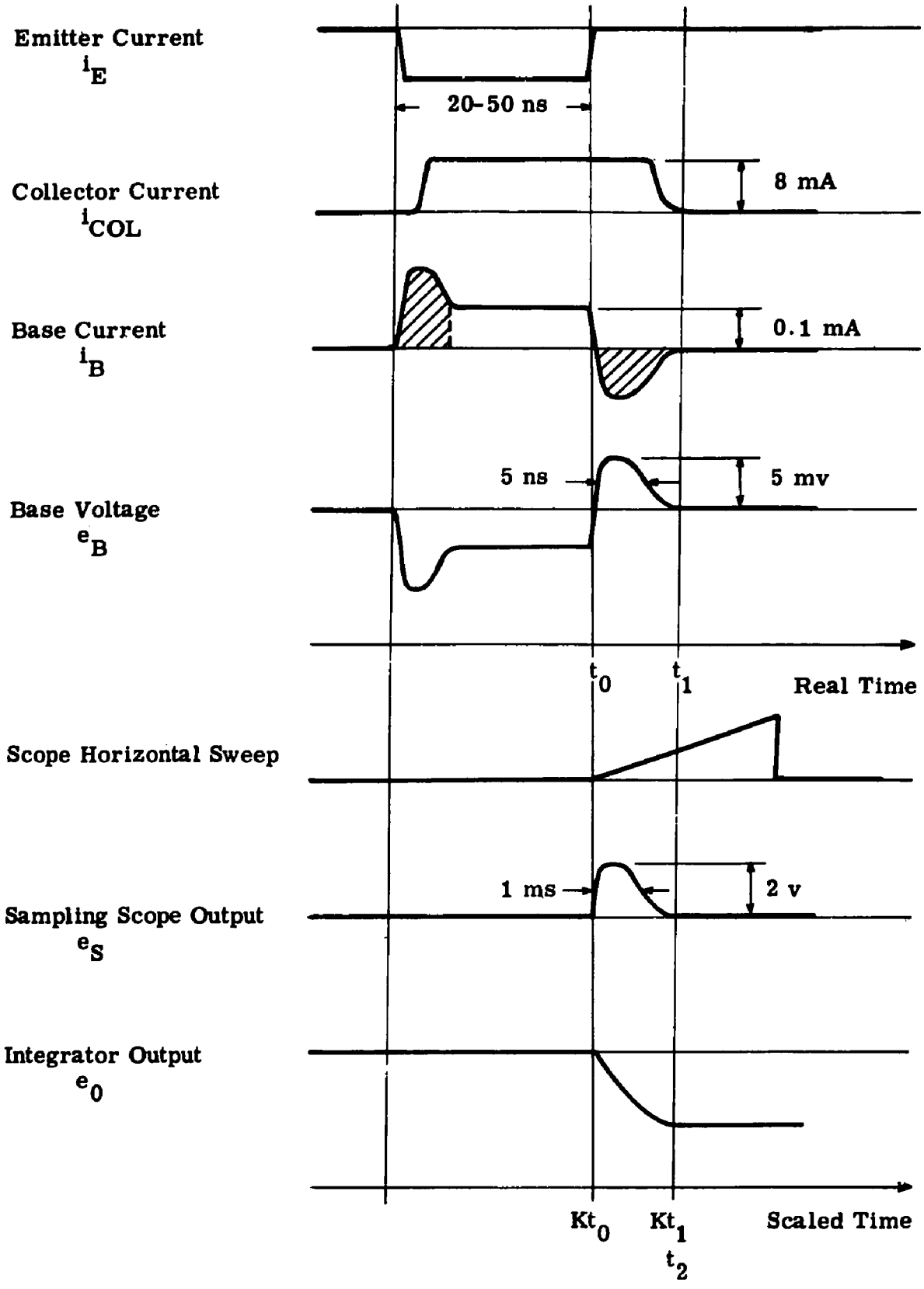

Fig. A.2. Typical waveshapes for charge storage measurement

sampling nature of the scope, the reconstructed waveform displayed and provided as an output assumes the time period of the horizontal sweep and can be independent of the time period of the original signal. The amplitude of the displayed signal is dependent on the gain setting of the vertical amplifier of the scope.

The oscilloscope delay and triggering circuits (Fig. A.3) can be adjusted such that the scope will display only the negative transient of the base potential (Fig. A.2). This waveform is thus available as an output signal from the oscilloscope. An integral of this negative transient can then be performed and used to determine the amount of stored base charge:

E.g., referring to Figs. A.1 and A.2,

$$G = \text{gain of vertical channel of oscilloscope}$$

$$= \frac{\text{amplitude of scope output signal, } |e_S|}{\text{amplitude of scope input signal, } |e_B|}$$

$$= \frac{1.0 \text{ (volt/cm)}}{\text{vertical sensitivity (volt/cm)}} \qquad \text{(for the scope used)}$$

$$K = \text{time scaling factor}$$

$$= \frac{t_2 - kt_0}{t_1 - t_0}$$

Thus,

$$e_S(Kt) = Ge_B(t)$$

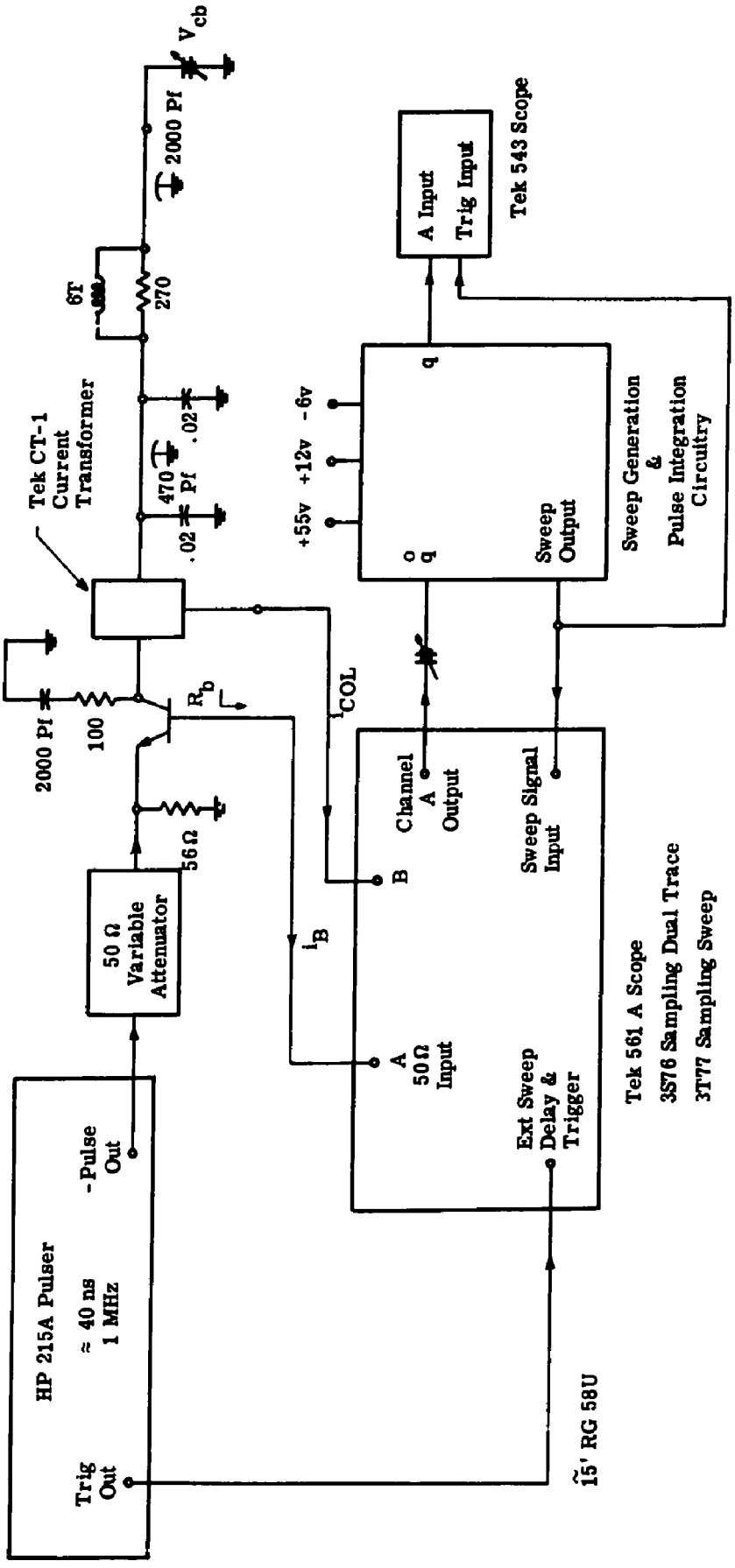

Fig. A.3. System for τ_F charge storage measurements

and the stored charge, $Q_{B_{stored}}$, can be related to the output of the integrator, e_0, as follows;

Let $t_0 = 0$

$$Q_{B_{stored}} = \int_{t=0}^{t_1} i_B(t)\, dt$$

$$= \int_{t=0}^{t_1} - \frac{e_B(t)}{R_b}\, dt$$

$$= - \frac{1}{G R_b} \int_{t=0}^{t_1} e_S(Kt)\, dt$$

Let $\tau = Kt$

$$Q_{B_{stored}} = - \frac{1}{G R_b} \int_{\tau=0}^{Kt_1} e_S(\tau)\, \frac{d\tau}{K}$$

$$= - \frac{1}{KGR_b} \int_{\tau=0}^{t_2} e_S(\tau)\, d\tau$$

Now with $e_0(0) \overset{set}{=} 0$

$$e_0(t_2) = - \frac{1}{RC} \int_{\tau=0}^{t_2} e_S(\tau)\, d\tau$$

Hence

$$Q_{B_{stored}} = \frac{RC}{KGR_b}\, e_0(t_2)$$

The control and measurement circuitry used for the charge measurements is shown in Figs. A.3, A.4, A.5 and A.6. For the 2N3866 transistor, a much wider excitation pulse is required for the τ_R measurement than for the τ_F measurement. For that reason, the pulse driver and delay circuits of Figs. A.5 and A.6 differ slightly from those of the τ_F measurement (Fig. A.4). The actual details are not as important as might be implied by the circuits given. Many circuit variations and measurement automation are possible. The circuits shown were largely determined by the performance characteristics of the available measurement equipment and components.

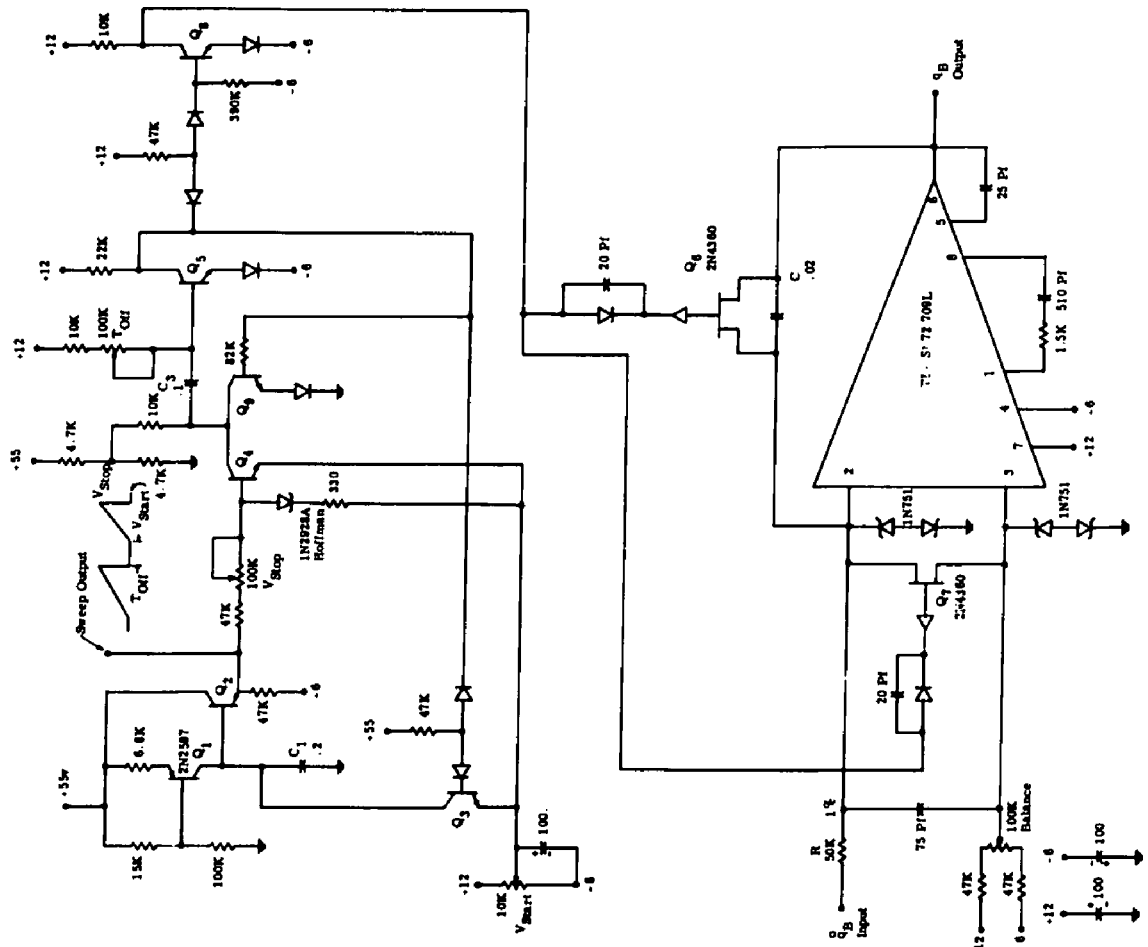

Fig. A.4. Sweep generation and pulse integration circuitry for charge storage measurement

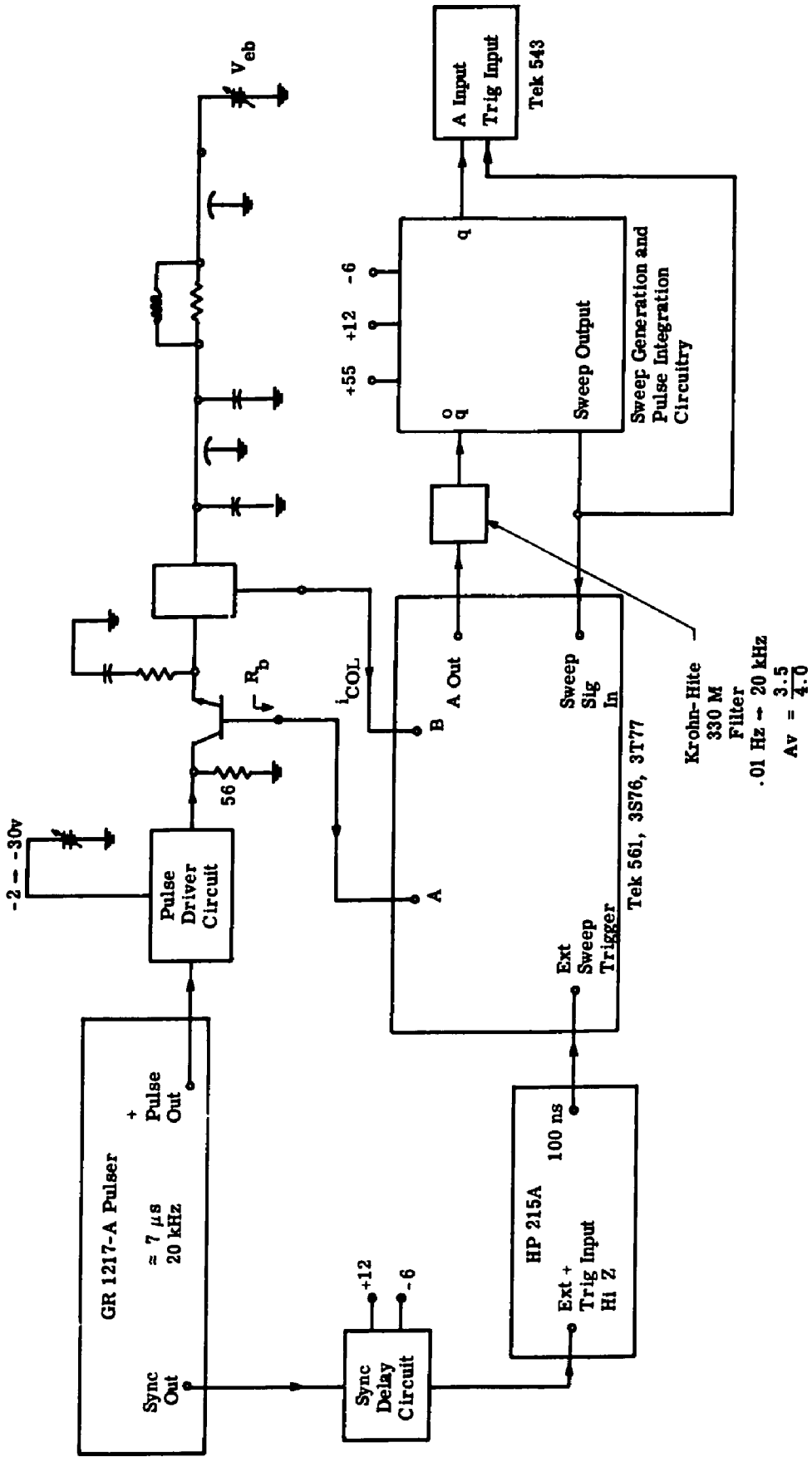

Fig. A.5. System for τ_R charge storage measurement

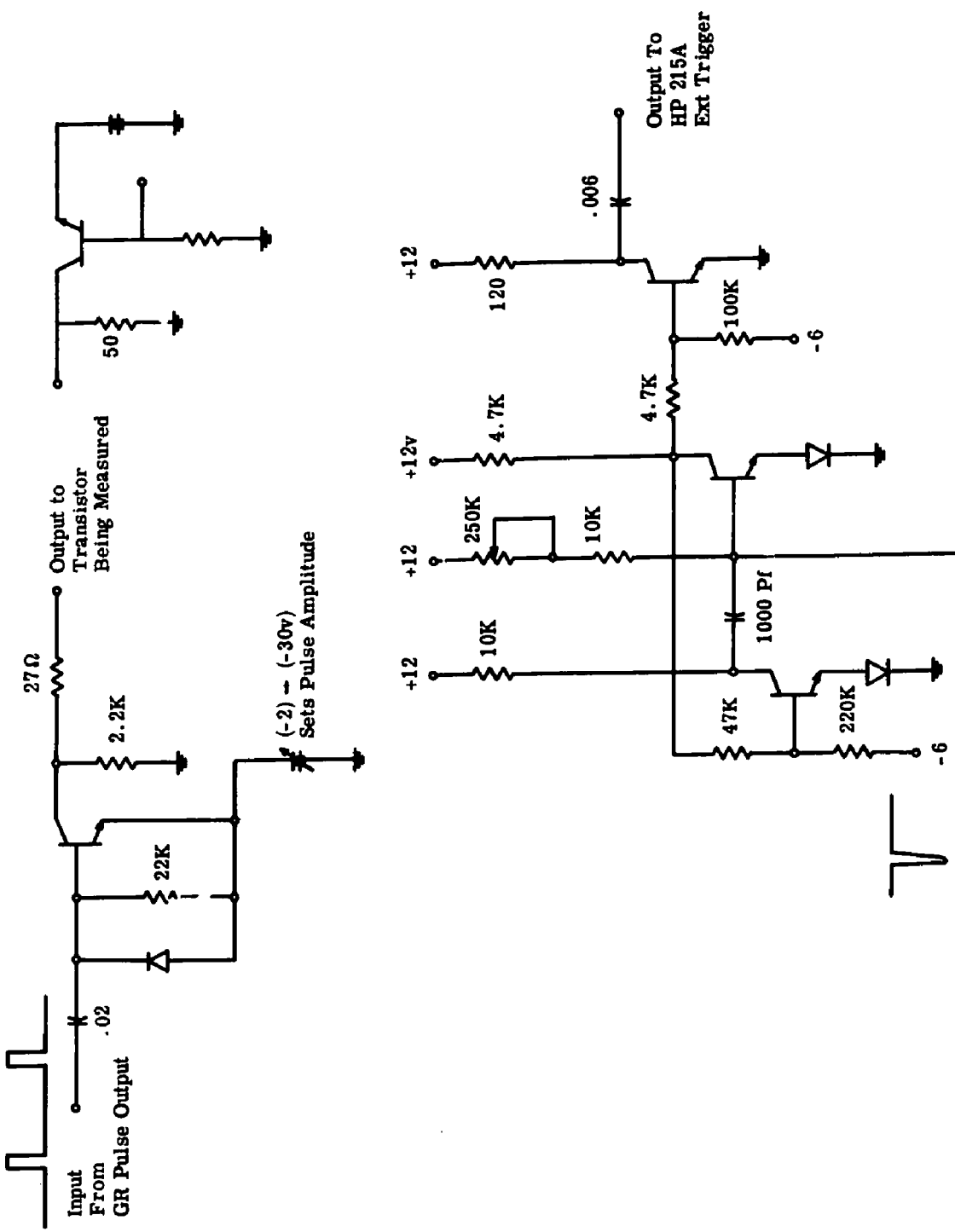

Fig. A.6. Pulse driver and sync delay circuits used for T_R charge storage measurement

APPENDIX B

TRANSFORMATION FROM CHARGE CONTROL TO VOLTAGE CONTROL

The voltage controlled intrinsic transistor model (Fig. 2.12) is mathematically identical to the charge controlled model (Fig. 2.1). If we take the differential equation description of the charge control model (Eqs. 2.1 - 2.2)

$$i_B' = \frac{q_F}{\tau_F \beta_F} + \dot{q}_F + \frac{q_R}{\tau_R \beta_R} + \dot{q}_R - C_{EDEP}\,\dot{v}_{E'B'} - C_{CDEP}\,\dot{v}_{C'B'}$$

$$i_{COL}' = \frac{q_F}{\tau_F} - \frac{q_R}{\tau_R} - \dot{q}_R - \frac{q_R}{\tau_R \beta_R} + C_{CDEP}\,\dot{v}_{C'B'}$$

$$= \frac{q_F}{\tau_F} - \frac{q_R}{\alpha_R \tau_R} - \dot{q}_R + C_{CDEP}\,\dot{v}_{C'B'}$$

and remove the charge variables by utilizing the nonlinear charge constraints (Eqs. 2.3 - 2.4)

$$q_F = Q_{FS}\left(e^{-\lambda v_{E'B'}} - 1\right)$$

$$q_R = Q_{RS}\left(e^{-\lambda v_{C'B'}} - 1\right)$$

where

$$Q_{FS} = \frac{\alpha_F \tau_F I_{EBO}}{1 - \alpha_F \alpha_R}$$

$$Q_{RS} = \frac{\alpha_R \tau_R I_{CBO}}{1 - \alpha_F \alpha_R} \quad ,$$

we get a system of voltage controlled equations.

$$i_B' = \frac{Q_{FS}(1 - \alpha_F)}{\tau_F \alpha_F} \left(e^{-\lambda v_{E'B'}} - 1 \right) + \frac{Q_{RS}(1 - \alpha_R)}{\tau_R \alpha_R} \left(e^{-\lambda v_{C'B'}} - 1 \right)$$

$$- \lambda Q_{FS} \left(e^{-\lambda v_{E'B'}} \right) \dot{v}_{E'B'} - C_{EDEP} \dot{v}_{E'B'}$$

$$- \lambda Q_{RS} \left(e^{-\lambda v_{C'B'}} \right) \dot{v}_{C'B'} - C_{CDEP} \dot{v}_{C'B'}$$

$$i_{COL}' = \frac{Q_{FS}}{\tau_F} \left(e^{-\lambda v_{E'B'}} - 1 \right) - \frac{Q_{RS}}{\alpha_R \tau_R} \left(e^{-\lambda v_{C'B'}} - 1 \right)$$

$$+ \lambda Q_{RS} \left(e^{-\lambda v_{C'B'}} \right) \dot{v}_{C'B'} + C_{CDEP} \dot{v}_{C'B'}$$

We can associate the current terms dependent on the time derivatives of voltage with capacitances and separate the nonlinear capacitive and resistive effects. With the definitions

$$i_F \triangleq \frac{Q_{FS}}{\alpha_F \tau_F}\left(e^{-\lambda v_{E'B'}} - 1\right) = I_{FS}\left(e^{-\lambda v_{E'B'}} - 1\right)$$

$$i_R \triangleq \frac{Q_{RS}}{\alpha_R \tau_R}\left(e^{-\lambda v_{C'B'}} - 1\right) = I_{RS}\left(e^{-\lambda v_{C'B'}} - 1\right)$$

$$C_{EDIFF} \triangleq \lambda Q_{FS} e^{-\lambda v_{E'B'}}$$

$$C_{CDIFF} \triangleq \lambda Q_{RS} e^{-\lambda v_{C'B'}}$$

the voltage control equations can be expressed conveniently as

$$i_{B'} = (1 - \alpha_F) i_F + (1 - \alpha_R) i_R - (C_{EDIFF} + C_{EDEP}) \dot{v}_{E'B'}$$

$$- (C_{CDIFF} + C_{CDEP}) \dot{v}_{C'B'}$$

$$i_{COL'} = \alpha_F i_F - i_R + (C_{CDIFF} + C_{CDEP}) \dot{v}_{C'B'}$$

This system of equations has the circuit representation used for the voltage controlled transistor model.

APPENDIX C

ALGORITHM FOR CLASS C AMPLIFIER ANALYSIS

A flow chart describing the computer algorithm used for analyzing the 100 MHz amplifier simulated with the extended transistor model (Section 5.3) is shown in Fig. C.1. The numbers presented beside the blocks of the chart refer to the line numbers in the related Fortran IV program listing (Table C.1).

A typical data set for use with the program is illustrated in Table C.2. In this example the external circuit parameters are contained in data Lines 2 through 12. The parameter PHI is the phase angle of the sinusoidal input excitation. Experience has indicated that convergence to the limit cycle is facilitated by selecting PHI such that the system state variables are relatively smooth at the endpoints of the period. Such selection normally requires one solution to be found from an arbitrary choice of PHI in order to aid the selection for successive runs.

The transistor parameters for the example are entered in Lines 13 through 38. Estimates of the initial conditions for the seven state variables are contained in Lines 39 through 45, and again, experience gained from preceding runs guides the selection of these values.

Maximum step size in the independent variable (time) in the integration subroutine and the allowable cumulative integration error

are specified by Lines 46 and 47. The maximum number of total iterations allowable for each solution is declared by JMAX (Line 48), and the squared error convergence criterion is given by SLOP (Line 49). Lines 50 through 59 are used to determine which of the computed waveforms are to be plotted.

Data for successive runs will be the same as for the preceding run unless specifically altered in the data set. For example, in the second run of Table C.2 (Lines 61 through 71) the value of the excitation period T is changed from 1.05 to 1.15, and some of the waveform plot requests are negated. The initial conditions for this second analysis will be the final values determined for the state variables in the first analysis. This retention of final values reduces the input data required and provides a reasonable estimate of initial conditions when small parameter increments are made between analyses.

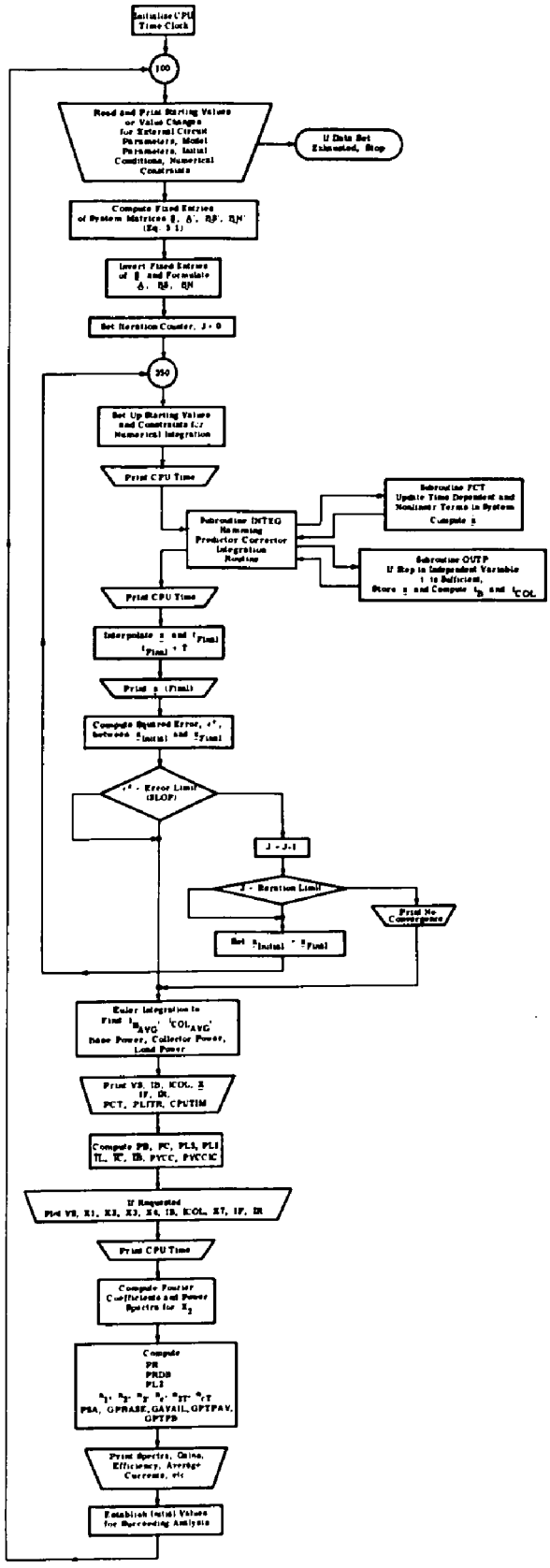

Fig. C.1. Flow chart for class C amplifier analysis algorithm

Table C.1. Program listing for class C amplifier analysis

```
      C*****CLASS C AMPLIFIER ANALYSIS WITH EXTENDED VOLTAGE-CONTROL MODEL
      C*****  S*XDOT = AP*X + BNP*UN + BSP*US
      C*****  XDOT = A*X + BN*UN + BS*US
      C*****  X1=VBB, X2=VCE, X3=VB'B', X4=VC'B'
      C*****  X5=ILS, X6=ILEE, X7=ILL
      C*****  UN1=IF, UN2=ALPHAF*IF, UN3=IR, UN4=ALPHAR*IR, UN5=IA
      C*****  US1=VST, US2=VCC, US3=VSAVG
      C
            DIMENSION S(7,7),SINV(7,7),AP(7,7),A(7,7),
           1BNP(7,5),BN(7,5),BSP(7,3),BS(7,3),
           2X1(300),X2(300),X3(300),X4(300),X5(300),X6(300),X7(300),
           3VST(300),IB(300),ICOL(300),TYME(300),CPUTIM(300),
           4Y(7),DERY(7),PRM(5),AUX(16,7),IMAGE(9999)
           5,CBE(11),CBC(11),CMAGSQ(11),CMAG(11),P(11),PR(11),PRDB(11)
           6,IF(300),IR(300)
      C
            COMMON NS,PHI,VSDC,VSA,I,LAMBDA,
           1IBFS,ALPHAF,IF,IBRS,ALPHAR,IR,
           2CJE,VJE,GAMMAE,CFE,A3LIM,
           3CJC,VJC,GAMMAC,CFC,A4LIM,
           4LS,CS,LL,CL,CCB,CCE,LEE,CBE,
           5A,BN,BS,
           6T,X1,X2,X3,X4,X5,X6,X7,VST,IB,ICOL,IF,IR,CE,CC,RL
           7,TYME,PS,VCC,CPUTIM,VA,NA
           8,BSUS12,BSUS22,BSUS53,BSUS72,AP14,AP46
      C
            REAL LAMBDA,ILSIV,ILLIV,IB,ICOL,ICZERO,IEZERO,LS,LL,LEE,IF,IR
           1,ILEEIV,IA,NA
      C
            DOUBLE PRECISION Y,DERY,AUX,PRM,ZT
```

Table C.1. (Cont.)

```
      C
            NAMELIST/DATA/VSA,PHI,VSDC,VCC,T,RS,LS,CS,RL,LL,CL,
     1CCB,CBE,CCE,RCC,RBB,REE,LEE,
     2QFS,QRS,TF,TR,ALPHAF,ALPHAR,LAMBDA,VA,NA,
     3CJC,VJC,GAMMAC,CFC,A4LIM,
     4CJE,VJE,GAMMAE,CFE,A3LIM,
     5VFBIV,VCEIV,VFBBPI,VCBBPI,ILSIV,ILEEIV,ILLIV,
     6PCSTEP,PCEBR,JMAX,SLOP,
     7PLTVFB,PLTVCE,PVFBBP,PVCBBP,PLTIB,PLTIC,
     8PLTILL,PLTVS,PLTIE,PLTIR
     1/DRIVE/T1,T2,DUTYCY
     2/OUT/PSA,PB,PC,PVCC,PL1,PL2,PL3,
     3EFF1,EFF2,EFF3,EFFC,EFF3T,EFFCT,
     4GAVAIL,GPBASE,GPTPAV,GPTPB,AVGIB,AVGIC
     5,PVCCIC
      C
            EXTERNAL FCT,OUTP
      C
      C
            CALL TIME(0)
  100 READ(5,DATA,END=1000,ERR=105)
            WRITE(6,2000)
            WRITE(6,DATA)
      104   GO TO 107
      105   WRITE(6,106)
      106   FORMAT('ERROR IN INPUT DATA---DATA SET OMITTED')
            GO TO 100
      107   FS=1./T
            WS=6.28318*FS
            ARG1=VSDC/VSA
            T1=(ARSIN(ARG1))/WS
            T2=T/2.-T1
            TAU=T2-T1
            DUTYCY=TAU/T
            WRITE(6,DRIVE)
```

Table C.1. (Cont.)

```
      DO 120 IROW=1,7
      DO 112 ICOLMN=1,7
      S(IROW,ICOLMN)=0.
      SINV(IROW,ICOLMN)=0.
      AP(IROW,ICOLMN)=0.
112   A(IROW,ICOLMN)=0.
      DO 114 ICOLMN=1,5
      PNP(IROW,ICOLMN)=0.
114   BN(IROW,ICOLMN)=0.
      DO 116 ICOLMN=1,3
      PSP(IROW,ICOLMN)=0.
116   BS(IROW,ICOLMN)=0.
120   CONTINUE
      AP(1,4)=1./(RBB+RCC)
      AP(1,1)=-1./RS-AP(1,4)
      AP(1,2)=-AP(1,4)
      AP(2,1)=AP(1,2)
      AP(2,2)=AP(1,2)-1./RL
      AP(2,4)=AP(1,4)
      AP(4,1)=AP(1,4)
      AP(4,2)=AP(1,4)
      AP(4,4)=AP(1,2)
      AP(5,1)=-1.
      AP(6,1)=-RCC/(RCC+RBB)
      AP(6,2)=1.+AP(6,1)
      AP(6,3)=1.
      AP(6,4)=-AP(6,2)
      AP(7,2)=1.
      AP(6,6)=-REF-(RBB*RCC)/(RBB+RCC)
      AP(1,5)=1.
      AP(1,6)=RCC/(RBB+RCC)
      AP(2,6)=-RBB/(RBB+RCC)
      AP(2,7)=-1.
      AP(3,6)=-1.
```

Table C.1. (Cont.)

```
100             AP(4,6)=-AP(2,4)
101             BNP(3,1)=1.
102             BNP(3,4)=-1.
103             BNP(3,5)=-1.
104             BNP(4,2)=-1.
105             BNP(4,3)=1.
106             BSP(1,1)=-1./RS
107             BSP(2,2)=1./RL
108             BSP(5,3)=-1.
109             BSP(7,2)=-1.
110             S(1,1)=CS+CBE+CCB
111             S(1,2)=CCB
112             S(2,1)=CCB
113             S(2,2)=CL+CCE+CCB
11              S(3,3)=CE
115             S(4,4)=CC
116             S(5,5)=LS
117             S(6,6)=LEE
118             S(7,7)=LL
119             D=S(1,1)*S(2,2)-S(1,2)*S(2,1)
120             SINV(1,1)=S(2,2)/D
121             SINV(1,2)=-S(2,1)/D
122             SINV(2,1)=-S(1,2)/D
1               SINV(2,2)=S(1,1)/D
124             SINV(3,3)=0.
125             SINV(4,4)=0.
126             SINV(5,5)=1./S(5,5)
127             SINV(6,6)=1./S(6,6)
128             SINV(7,7)=1./S(7,7)
129             DO 300 NR=1,7
130             DO 200 NC=1,7
131             A(NR,NC)=0.
132             DO 200 NI=1,7
133     200     A(NR,NC)=A(NR,NC)+SINV(NR,NI)*AP(NI,NC)
```

Table C.1. (Cont.)

```
134             DO 240 NC=1,5
135             BN(NR,NC)=0.
136             DO 240 NI=1,7
137       240   BN(NR,NC)=BN(NR,NC)+SINV(NR,NI)*BNP(NI,NC)
138             DO 280 NC=1,3
139             BS(NR,NC)=0.
140             DO 280 NI=1,7
141       280   BS(NR,NC)=BS(NR,NC)+SINV(NR,NI)*BSP(NI,NC)
142       300   CONTINUE
143       C
144             BSUS12=BS(1,2)*VCC
145             BSUS22=BS(2,2)*VCC
146             BSUS53=-BS(5,3)*VSDC
147              BSUS72=BS(7,2)*VCC
14              AP14=AP(1,4)
15              AP46=AP(4,6)
150             TYME(9)=-1.
151             TYME(10)=0.
152             X1(10)=VBBIV
153             X2(10)=VCEIV
154             X3(10)=VFBBI
155             X4(10)=VCBBI
156             X5(10)=ILSIV
157             X6(10)=ILEEIV
158             X7(10)=ILLIV
159             VST(9)=-VSDC+VSA*SIN(PHI)
160             TBF=(TF*ALPHAF)/(1.-ALPHAF)
161             TBR=(TR*ALPHAR)/(1.-ALPHAR)
162             ICZERO=(ORS*(1.-ALPHAF*ALPHAR))/(TBR*(1.-ALPHAR))
163             IEZERO=(OFS*(1.-ALPHAF*ALPHAR))/(TBF*(1.-ALPHAF))
164             ICOL(9)=ICZERO
165             IB(9)=-ICZERO-IEZERO
166             DT=PCSTEP*T
167             J=0
```

Table C.1. (Cont.)

```
168       350     Y(1)=X1(10)
169               Y(2)=X2(10)
170               Y(3)=X3(10)
171               Y(4)=X4(10)
172               Y(5)=X5(10)
173               Y(6)=X6(10)
17                Y(7)=X7(10)
175               PRM(1)=0.
176               PRM(2)=T
177               PRM(3)=DT
178               PRM(4)=DCERR*VCC
179               PRM(5)=0.
180               NDIM=7
181               IHLF=5
1                 DERY(1)=.15
1                 DERY(2)=.15
184               DERY(3)=.2
185               DERY(4)=.2
186               DERY(5)=.1
187               DERY(6)=.1
188               DERY(7)=.1
189               I=10
190       C
191               WRITE(6,444)J
192       444     FORMAT(' READY TO ENTER INTEG   J=',I2)
193               CALL TIME(1,1)
194       500     CALL INTEG(PRM,Y,DERY,NDIM,IHLF,FCT,OUTP,AUX)*
195               CALL TIME(1,1)
196               IMAX=I-1
197               IMIX=IMAX-1
198       C
```

*From IBM Scientific Subroutine Package (Subroutine DHPCG).

Table C.1. (Cont.)

```
C*****ADJUST ENDPOINTS OF COMPUTATION
      TADJ=(TYME(IMAX)-T)/(TYME(IMAX)-TYME(IMIX))
      X1(IMAX)=X1(IMAX)-TADJ*(X1(IMAX)-X1(IMIX))
      X2(IMAX)=X2(IMAX)-TADJ*(X2(IMAX)-X2(IMIX))
      X3(IMAX)=X3(IMAX)-TADJ*(X3(IMAX)-X3(IMIX))
      X4(IMAX)=X4(IMAX)-TADJ*(X4(IMAX)-X4(IMIX))
      X5(IMAX)=X5(IMAX)-TADJ*(X5(IMAX)-X5(IMIX))
      X6(IMAX)=X6(IMAX)-TADJ*(X6(IMAX)-X6(IMIX))
      X7(IMAX)=X7(IMAX)-TADJ*(X7(IMAX)-X7(IMIX))
      TYME(IMAX)=T
C
      WRITE(6,610)IHLF,TYME(IMAX),X1(IMAX),X2(IMAX),X3(IMAX),X4(IMAX),
     1X5(IMAX),X6(IMAX),X7(IMAX)
610   FORMAT(' IHLF,T,Y: ',I3,8(1X,G10.3))
      EPSISO=
     1(((X1(IMAX)-X1(10))/X1(IMAX))**2)+
     2(((X2(IMAX)-X2(10))/X2(IMAX))**2)+
     3(((X3(IMAX)-X3(10))/X3(IMAX))**2)+
     4(((X4(IMAX)-X4(10))/X4(IMAX))**2)+
     5(((X5(IMAX)-X5(10))/X5(IMAX))**2)+
     6(((X6(IMAX)-X6(10))/X6(IMAX))**2)+
     7(((X7(IMAX)-X7(10))/X7(IMAX))**2)
      IF(EPSISO-SLOP)800,800,700
700   J=J+1
      IF(J-JMAX)710,710,720
710   X1(10)=X1(IMAX)
      X2(10)=X2(IMAX)
      X3(10)=X3(IMAX)
      X4(10)=X4(IMAX)
      X5(10)=X5(IMAX)
      X6(10)=X6(IMAX)
      X7(10)=X7(IMAX)
      GO TO 350
720   WRITE(6,721)IMAX
```

Table C.1. (Cont.)

```
      721   FORMAT(' NO CONVERGENCE WITH ',I2,' ITERATIONS')
      C
      C*****EULER INTEGRATION
      800   AVGILT=0.
            AVGICT=0.
            AVGIBT=0.
            PBT=0.
            PCT=0.
            PLITR=0.
            INTLIM=IMAX-1
            DO 820 II=1,INTLIM
            JJ=II+1
            PBT=PBT-IB(II)*X1(II)-IB(JJ)*X1(JJ)
            PCT=PCT+ICOL(II)*X2(II)+ICOL(JJ)*X2(JJ)
            PLITR=PLITR+((X2(II)-VCC)**2)+((X2(JJ)-VCC)**2)
            AVGILT=AVGILT+X7(II)+X7(JJ)
            AVGICT=AVGICT+ICOL(II)+ICOL(JJ)
            AVGIBT=AVGIBT+IB(II)+IB(JJ)
      C
      820   WRITE(6,811)II,TYPE(II),VST(II),IB(II),ICOL(II),
           1X1(II),X2(II),X3(II),X4(II),X5(II),X6(II),X7(II)
           2,PCT,PLITR,CPUTIM(II),IE(II),IB(II)
      811   FORMAT(' I=',I3,'  TIME=',G10.3,'  VS=',G10.3,'  IB=',G10.3,
           1'  ICOL=',G10.3,'  VB=',G10.3,'  VC=',G10.3,'  VBBP=',G10.3/
           2'  VCBP=',G10.3,'  ILS=',G10.3,'  ILEE=',G10.3,'  ILI=',
           3G10.3,'  PCT=',G10.3,'  PLITR=',G10.3,'  CPUTIM=',G12.5/
           4'  IE=',G10.3,'  IB=',G10.3)
            WRITE(6,811)IMAX,TYPE(IMAX),VST(IMAX),IB(IMAX),ICOL(IMAX),
           1X1(IMAX),X2(IMAX),X3(IMAX),X4(IMAX),X5(IMAX),X6(IMAX),X7(IMAX)
           2,PCT,PLITR,CPUTIM(IMAX),IE(IMAX),IB(IMAX)
            PB=PBT/((IMAX-1)*2.)
            PC=PCT/((IMAX-1)*2.)
            PL3=PLITR/(PL*(IMAX-1)*2.)
            PI1=PL3+PC
```

Table C.1. (Cont.)

```
267                AVGIL=AVGILT/((IMAX-10)*2.)
2                  AVGIC=AVGICT/((IMAX-10)*2.)
2.                 AVGIB=AVGIBT/((IMAX-10)*2.)
270                PVCC=-AVGIL*VCC
271                PVCCIC=AVGIC*VCC
272                NDATA=I-10
273          C
274          2000  FORMAT(1H1)
275                IF(PLTVS)1800,1800,1700
276          1700  WRITE(6,2000)
277                CALL STPLT2(IMAGE,TYME(10),VST(10),NDATA,4,'0',11,'VST VS TIME')
278          1800  CONTINUE
279                IF(PLTVEB)2200,2200,2100
280          2100  WRITE(6,2000)
281                CALL STPLT2(IMAGE,TYME(10),X1(10),NDATA,4,'0',11,'VEB VS TIME')
282          2200  IF(PLTVCE)2400,2400,2300
283          2300  WRITE(6,2000)
284                CALL STPLT2(IMAGE,TYME(10),X2(10),NDATA,4,'0',11,'VCE VS TIME')
285          2400  IF(PVEPBP)2600,2600,2500
286          2500  WRITE(6,2000)
287                CALL STPLT2(IMAGE,TYME(10),X3(10),NDATA,4,'0',13,'VEPBP VS TIME')
288          2600  IF(PVCPBP)2800,2800,2700
289          2700  WRITE(6,2000)
290                CALL STPLT2(IMAGE,TYME(10),X4(10),NDATA,4,'0',13,'VCPBP VS TIME')
291          2800  IF(PLTIB)3000,3000,2900
292          2900  WRITE(6,2000)
293                CALL STPLT2(IMAGE,TYME(10),IB(10),NDATA,4,'0',10,'IB VS TIME')
2            3000  IF(PLTIC)3200,3200,3100
295          3100  WRITE(6,2000)
296                CALL STPLT2(IMAGE,TYME(10),ICOL(10),NDATA,4,'0',12,'ICOL VS TIME')
297          3200  IF(PLTILI)3400,3400,3300
298          3300  WRITE(6,2000)
```

Table C.1. (Cont.)

```
299               CALL STPLT2(IMAGE,TYME(10),X7(10),NDATA,4,'O',11,'ILL VS TIME')
300         3400  IF(PLTIF)3600,3500,3500
301         3500  WRITE(6,2000)
302               CALL STPLT2(IMAGE,TYME(10),IF(10),NDATA,4,'O',10,'IF VS TIME')
303         3600  IF(PLTIR)3800,3800,3700
304         3700  WRITE(6,2000)
305               CALL STPLT2(IMAGE,TYME(10),IR(10),NDATA,4,'O',10,'IR VS TIME')
306         3800  CONTINUE
307         C
308               WRITE(6,2000)
309               CALL TIME(1,1)
310               IMAXEV=IMAX/2
311               IMAXEV=IMAXEV*2
312               N=(IMAXEV-10)/2
313               M=10
314               CALL FORIT(X2(10),N,M,CRE,CIM,IER) *
315               IF(IER)6800,6900,6800
316         6800  WRITE(6,6050)IER
317         6050  FORMAT(' IER=',I1)
318         C*****CMAG(1)=DC COMPONENT, CMAG(2)=FUNDAMENTAL, CMAG(3)=2ND HARMONIC, ETC.
319         6900  K2=M+1
320               DO 7000 I2=1,K2
321               CMAGSQ(I2)=(CRE(I2)**2)+(CIM(I2)**2)
322               CMAG(I2)=SQRT(CMAGSQ(I2))
323         C
324         7000  P(I2)=CMAGSQ(I2)/(2.*PL)
325               P(1)=((CMAG(1)-VCC)**2)/PL
326               PL2=PC
327               DO 7200 I3=1,K2
328               PR(I3)=P(I3)/P(2)
329               PRDB(I2)=10.*(ALOG10(PR(I3)))
```

*From IBM Scientific Subroutine Package.

Table C.1. (Cont.)

```
330      7200   PL2= PL2+P(I3)
331             EFF1=P(2)/PL1
332             EFF2=P(2)/PL2
333             EFF3=P(2)/(PB+PVCC)
334             EFFC=P(2)/PVCC
335             EFF3T=(PL1-PC)/(PB+PVCC)
336             EFFCT=(PL1-PC)/PVCC
337             PSA=(VSA**2)/(8.*RS)
338             GPBASE=P(2)/PB
339             GAVAIL=P(2)/PSA
340             GPTPAV=PL3/PSA
341             GPTPB=(PL1-PC)/PB
342             WRITE(6,7500)
343      7500   FORMAT('4 N',6X,'CMAG(N)',6X,'P(N) WATTS',5X,
344            1'PRATIO(N/1)',4X,'PRATIO(DB)')
345             DO 7600 I4=1,K2
346             I5=I4-1
347      7600   WRITE(6,7700)I5,CMAG(I4),P(I4),PR(I4),PRDB(I4)
348      7700   FORMAT(1HC,I2,4(3X,1PE12.5))
349      C
350              WRITE(6,7850)
351      7850   FORMAT(1H-)
352             WRITE(6,OUT)
353             VERIV=X1(IMAX)
354             VCEIV=X2(IMAX)
355             VERBPI=X3(IMAX)
356             VCBBPI=X4(IMAX)
357             ILSIV=X5(IMAX)
358             ILECIV=X6(IMAX)
359             ILLIV=X7(IMAX)
360             GO TO 100
361      1000   STOP
362             END
363      C
```

Table C.1. (Cont.)

```
      C
      C
      C
            SUBROUTINE FCT(ZT,Y,DERY)
      C
            DIMENSION A(7,7),BN(7,5),BS(7,3),
           2X1(300),X2(300),X3(300),X4(300),X5(300),X6(300),X7(300),
           3VST(300),IB(300),ICOL(300),TYME(300),CPUTIM(300),
           4Y(7),DERY(7),IF(300),IR(300)
      C
            COMMON WS,PHI,VSDC,VSA,T,LAMBDA,
           1QFS,ALPHAF,TF,QPS,ALPHAR,TR,
           2CJE,VZE,GAMMAF,CFE,A3LIM,
           3CJC,VZC,GAMMAC,CFC,A4LIM,
           4LS,CS,LL,CL,CCB,CCE,LFE,CBE,
           5A,BN,BS,
           6T,X1,X2,X3,X4,X5,X6,X7,VST,IB,ICOL,IF,IR,CE,CC,RL
           7,TYME,RS,VCC,CPUTIM,VA,NA
           8,BSUS12,BSUS22,BSUS53,BSUS72,AP14,AP46
      C
            REAL LAMBDA,IF,IR,LS,LFE,LL,IB,ICOL,IA,NA
      C
            DOUBLE PRECISION Y,DERY,ZT
      C
      C
      C
            WST=WS*ZT
            VST(I)=-VSDC+VSA*SIN(WST+PHI)
            A1=-LAMBDA*Y(3)
            A2=-LAMBDA*Y(4)
            IF(A1-100.)21,21,20
      20    A1=100.
      21    IF(A2-100.)31,31,30
      30    A2=100.
```

Table C.1. (Cont.)

```
      31    CONTINUE
            IF(I)=(QFS*(EXP(A1)-1.))/(ALPHAF*TF)
            IR(I)=(QRS*(EXP(A2)-1.))/(ALPHAR*TR)
            A3=VZF+Y(3)
            A4=VZC+Y(4)
            IF(A3-A3LIM)40,40,41
      40    A3=A3LIM
      41    IF(A4-A4LIM)42,42,43
      42    A4=A4LIM
      43    CTF=CFF+CJF/(A3**GAMMAF)
            CTC=CFC+CJC/(A4**GAMMAC)
            IF(Y(3).GT.(.9*VA)) GO TO 49
            IA=0.
            CA=0.
            GO TO 52
      49    IF(Y(3)-VA-(1.E-6))51,50,50
      50    IA=(QFS*1.E-6)/(ALPHAF*TF)
            CA=TF*IA*1.E6
            GO TO 52
      51    IA=(QFS/(ALPHAF*TF))*((1./(1.-(Y(3)/VA))**NA)-1.)
            CA=(TF*IA)/(VA-Y(3))
      52    CF=LAMBDA*QFS*EXP(A1)+CTF+CA
            CC=LAMBDA*QRS*EXP(A2)+CTC
            DERY(1)=A(1,1)*Y(1)+A(1,2)*Y(2)+A(1,4)*Y(4)+A(1,5)*Y(5)+
           .A(1,6)*Y(6)+A(1,7)*Y(7)+BS(1,1)*VST(I)+BSUS12
            DERY(2)=A(2,1)*Y(1)+A(2,2)*Y(2)+A(2,4)*Y(4)+A(2,5)*Y(5)+
           .A(2,6)*Y(6)+A(2,7)*Y(7)+BS(2,1)*VST(I)+BSUS22
            DERY(3)=(IF(I)-ALPHAR*IR(I)-IA-Y(6))/CF
            DERY(4)=(AP14*(Y(1)+Y(2)-Y(4))+AP46*Y(6)+IR(I)-ALPHAF*IF(I))/CC
            DERY(5)=A(5,1)*Y(1)+BSUS53
            DERY(6)=A(6,1)*Y(1)+A(6,2)*Y(2)+A(6,3)*Y(3)+
           .A(6,4)*Y(4)+A(6,6)*Y(6)
            DERY(7)=A(7,2)*Y(2)+BSUS72
            RETURN
            END
```

Table C.1. (Cont.)

```
      C
      C
      C
      C
            SUBROUTINE OUTP(ZT,Y,DERY,IHLF,NDIM,PRM)
      C
            DIMENSION A(7,7),BN(7,5),
           1BS(7,3),
           2X1(300),X2(300),X3(300),X4(300),X5(300),X6(300),X7(300),
           3VST(300),IB(300),ICOL(300),TYME(300),CPUTIM(300),
           4Y(7),DERY(7),PRM(5),IF(300),IR(300)
      C
            COMMON WS,PIT,VSDC,VSA,I,LAMBDA,
           1DFS,ALPHAF,TF,QRS,ALPHAP,TP,
           2CJE,VJE,GAMMAE,CEE,A3LIM,
           3CJC,VJC,GAMMAC,CEC,A4LIM,
           4LS,CS,LL,CL,CCB,CCE,LEE,CBE,
           5A,BN,BS,
           6T,X1,X2,X3,X4,X5,X6,X7,VST,IB,ICOL,IF,IR,CE,CC,RL
           7,TYME,BS,VCC,CPUTIM,VA,NA
           8,BSUS12,BSUS22,BSUS53,BSUS72,AP14,AP46
      C
            REAL LAMBDA,LS,LL,LEE,IB,ICOL,IF,IR,IA,NA
      C
            DOUBLE PRECISION Y,DERY,PRM,ZT
            IF(ZT-TYME(I-1)-.000999*T)70,63,63
   63       TYME(I)=ZT
            X1(I)=Y(1)
            X2(I)=Y(2)
            X3(I)=Y(3)
            X4(I)=Y(4)
            X5(I)=Y(5)
            X6(I)=Y(6)
            X7(I)=Y(7)
```

Table C.1. (Concluded)

```
467                 IB(I)=(VST(I)+Y(1))/RS-XS(I)+CS*DERY(1)
468                 CALL TIMF(1,0,IME)
469                 CPUTIM(I)=IME*1.E-3
470                 IF((Y(3)+Y(4)).LT.0.)GO TO 120
471                 ICOL(I)=ALPHAF*IF(I)-IB(I)+CCB*(DERY(1)+DERY(2))+CC*DERY(4)
472       110       I=I+1
473       70        RETURN
4         120       ICOL(I)=-Y(7)+(VCC-Y(2))/RL-CL*DERY(2)
474                 GO TO 110
476                 END
```

Table C.2. Sample data set for class C amplifier analysis

```
1       $DATA
2       VSA=8.,
3       PHI=2.51324,
4       VSDC=2.,
5       VCC=10.,
6       T=1.05,
7       RS=.05,
8       LS=.007,
9       CS=.16,
10      RL=.225,
11      LI=.0073,
12      CI=.72,
13      CCB=.026,
14      CBE=.016,
15      CCE=.026,
16      RCC=.012815,
17      RBB=.02245,
18      REE=.000455,
19      LEE=3.36E-4,
20      QFS=4.66E-10,
21      QRS=1.16E-7,
22      TF=.011,
23      TR=2.56,
24      AIPHAN=.9877,
25      AIPHAI=.66667,
26      LAMBDA=21.3,
27      VA=6.2,
28      NA=4.,
29      CJC=.341,
30      VJC=.5,
31      GAMMAC=.474,
32      CEC=.17,
33      A4LIM=.0625,
34      CJE=1.04,
35      VJE=.8,
36      GAMMAE=.319,
37      CJE=.01,
38      A3LIM=.06,
39      VEBIV=.211,
40      VCEIV=4.56,
41      VEPBPI=-1.058,
42      VCPBPI=-.362,
43      IISIV=110.,
44      ILEEIV=253.,
45      ILLIV=-298.,
46      PCSTEP=.01,
47      PCERR=1.E-4,
48      JMAX=15.,
```

Table C.2. (Cont.)

```
      SLOP=.004375,
      PITVEB=1.,
      PITVCB=1.,
      PITIB=1.,
      PLTIC=1.,
      PLTILL=1.,
      PVEBTP=1.,
      PVCTBP=1.,
      PITVS=1.,
      PLTIP=1.,
      PITIR=1.,
      &END
      &DATA
      T=1.15,
      PITVS=-1.,
      PITVB=-1.,
      PVBTP=-1.,
      PVCTBP=-1.,
      PLTIC=-1.,
      PLTIP=-1.,
      PITIP=-1.,
      PLTILL=-1.,
      &END
      &DATA
      T=1.2,
      &END
      &DATA
      T=1.3,
      &END
      &DATA
      T=1.4,
      &END
      &DATA
      T=1.5,
      &END
      &DATA
      T=1.6,
      &END
      &DATA
      T=1.7,
      &END
      &DATA
      T=1.8,
      &END
      &DATA
      T=1.9,
      &END
      &DATA
      T=2.00,
      &END
      &DATA
      T=.95,
```

Table C.2. (Concluded)

```
101       VFBIV=.211,
102       VCEIV=4.56,
103       VEPBPI=-1.058,
104       VCPBPI=-.362,
105       IISIV=119.,
106       ILEPIV=253.,
107       ILLIV=-298.,
108       &END
109       &DATA
110       T=.9,
111       &END
112       &DATA
113       T=.85,
114       &END
115       &DATA
116       T=.8,
117       &END
118       &DATA
119       T=.7,
120       &END
121       &DATA
122       T=.6,
123       &END
124       &DATA
125       T=.5,
126       &END
```

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