DOCTORAL DISSERTATION SERIES

Publication No.: 11,304

AUTHOR: Branch Price Kerfoot, Jr., Ph. D., 1955
University of Michigan

TITLE: TRANSISTORS IN ANALOGUE COMPUTING

University Microfilms, Ann Arbor, Michigan

TRANSISTORS IN ANALOGUE COMPUTING

by

Branch Price Kerfoot, Jr.

A dissertation
submitted in partial fulfillment of
the requirements for the degree of
Doctor of Philosophy in the University of Michigan

1955

Doctoral Committee:

Professor L. N. Holland, Chairman
Professor S. S. Attwood
Associate Professor C. L. Dolph
Professor W. G. Dow
Professor G. Hok
Mr. N. I. Korman, Radio Corporation of America

TRANSISTORS IN ANALOGUE COMPUTING

Abstract

A revised system of electronic analogue computing is outlined in detail in which current is used as the variable. This computing method is referred to as Current Computing. The current-computing system employs operational amplifiers which have low input impedances, high output impedances, and high current gains. Transistor amplifiers can conveniently be designed to meet these conditions. The thesis investigates and evaluates the use of transistors in this system of computing.

Suitable transistor amplifiers for a demonstration of current computing have been built and tested. Arrangements of the amplifier and suitable precision passive elements to perform the operations of isolation, multiplication by a constant, summation, integration, and differentiation are presented and studied in the dissertation. Experimental tests with a three-stage direct-coupled junction transistor amplifier have produced waveforms which demonstrate the principles of current computing in these operations. The development of the transistor amplifier is discussed, along with an outline of the method of phase and gain

response control to assure stability with the use of 66 decibels of inverse feedback. The amplifier itself and the overall unit which performs each type of operation are considered as modified four-terminal networks in order to express analytically the manner in which they operate on the current variable.

Errors in this computing system are similar to the errors in any analogue system and are due to the use of physically realizable elements, both active and passive. The most significant sources of error have been resolved and their effects may be expressed in terms of known and measurable system quantities for each computing operation.

The accuracy of the computing unit is calculated from a comparison of actual signal output to the ideal output when an appropriate ideal input signal waveform is assumed. This comparison yields an instantaneous fractional error which is averaged over a chosen period of time, usually the interval over which the computer solution is observed. The averaging process yields a single root-mean-square error figure for that interval. Typical numerical values are found for the particular transistor amplifier developed here. Other analogue systems, such as one using vacuum-tube amplifiers, may use this same procedure to find

the RMS error over an interval of special interest.

Current computing is described as an effective method of utilizing the advantages and peculiar impedance properties of transistors in the field of electronic analogue computing.

Preface

The purpose and historical background of the thesis work is presented in the Introduction along with an explanation of the new approaches to analogue computing which make up the dissertation itself. It remains to make a matter of record the fiscal origin of the engineering project involved and to express appreciation to those who have done most to help bring it to the present conclusion.

The work described in the dissertation has been performed while the author was employed by the Radio Corporation of America in its Electronic Products Division in Moorestown, New Jersey. It has been sponsored by RCA as a circuit development project within the Radar Engineering Section.

The author is indebted to a number of people in the University of Michigan and at RCA for encouragement and helpful cooperation throughout the period of work on this subject. Special appreciation is due the management of the Radar Section of RCA for suggesting, guiding, and maintaining this project through to the results and conclusions which are described here. Mr. N. I. Korman

has contributed to the approach and the methods which have been used. The help of Mr. L. E. Matson is also appreciated.

My Committee at Michigan has patiently guided and encouraged my thesis work through many stages. Their meetings in New York and at Michigan in order to follow and appraise my work have maintained substantial contact during its progress, even though the dissertation has been prepared "in industry."

It is expected and hoped that the author will have opportunities in the future to extend the results found here as newer circuit components become available.

November 5, 1954

TABLE OF CONTENTS

Page

LIST OF ILLUSTRATIONS vii

INTRODUCTION 1

CHAPTER ONE

Current-Computing Fundamentals 8

CHAPTER TWO

Summary of Current-Computing Demonstration Results 22

Circuit Models 22

Specifying Accuracy 35

Assuring Stability 38

Using Four-Terminal Network Methods . . . 38

AC Computing Amplifier 39

Chopper Stabilizing 40

For the Future 41

CHAPTER THREE

Operational Amplifier Design 42

Basic Considerations 42

DC Transistor Amplifier..... 44

Current-Computing Network Relations.... 51

Typical Values of Network Parameters... 57

Stability..... 58

Phase and Gain Control..... 65

Recommendations for Transistor Computing-Amplifier Designs..... 71

CHAPTER FOUR

System Error Analysis..... 81

CHAPTER FIVE

Conclusions..... 94

Specific Results..... 94

Discussion..... 96

APPENDIX I - List of Symbols..... 102

Major Quantities..... 102

Subscripts..... 104

Transistor Diagrams..... 105

APPENDIX II - Early Transistor Tests..... 106

Point-contact Transistors as Linear Amplifiers..... 107

Some Possible Methods of Using Transistors in Voltage-Analogue Computing..... 114

Early Current-Computing Circuit Tests.. 118

APPENDIX III - Pertinent Four-Terminal Network Relations..... 122

APPENDIX IV - Error Derivations..... 128

General Definitions..... 128

Operation of Isolation..... 132

Operation of Integration..... 135

Operation of Differentiation..... 139

BIBLIOGRAPHY..... 144

LIST OF ILLUSTRATIONS

Figure No.	Title	Page No.
1-1	Isolation and Multiplication by a Constant	9
1-2	Operation of Summation	10
1-3	Methods of Performing Integration	11
1-4	Methods of Performing Differentiation	12
2-1	Transistor Current Amplifier, Front	23
2-2	Transistor Current Amplifier, Rear	24
2-3	Transistor Current Amplifier, Encased	25
2-4	Example of Summing and Scale Change	29
2-5	Example of R and C Integration	30
2-6	Example of R and L Integration	31
2-7	Example of R and L Differentiation	32
2-8	Example of R and C Differentiation	33
3-1	Transistor Current Amplifier Tested	45
3-2	Measured Responses of Current Amplifier	46
3-3	Table of Technical Specifications	47
3-4	Current-Computing Operational Network	53
3-5	Nyquist Stability Criterion	62
3-6	Chopper DC Transistor Amplifier	76
3-7	Application of Chopper DC Amplifier	77

Figure No.	Title	Page No.
4-1	Waveforms Considered in Error Analysis	83
4-2	Calculated Error for Each Operation	86
II-1	Transistor-Vacuum Tube DC Amplifier	112
II-2	AC Transistor Computing Amplifier	121
III-1	Modified Four-Terminal Network	123
IV-1	Instantaneous Fractional Errors	134

INTRODUCTION

"Current Computing" is an abbreviated name for one system of electronic analogue computation which makes use of current as the analogue variable. By means of current computing, it is expected that new techniques, and especially the use of transistor amplifiers, may be applied to extend the usefulness of analogue computing units.

Potentialities for increased use of analogue computers are largely due to the recent advances in so-called subminiature and low-power components, which permit relatively complex electronic equipment to be compacted into small space and to have reasonable power consumption. An outstanding example of these advances is the transistor, whose low dissipation and physical advantages have made possible more elaborate equipments with savings over vacuum tubes in power, size, etc., as widely reported in recent literature[1].

(1) Superscript numbers refer to references listed in the Bibliography.

The method described here attempts to use transistors to their full advantage in the growing application of electronic analogue computers in scientific, military, and commercial fields. Present analogue computers find widespread use in scientific studies of differentially related variables, such as in aircraft design[2] [3].

Recently developed analogue techniques such as the use of a chopper amplifier for drift stabilization[4] have assured an effective and economical place for the analogue computer even side-by-side with the expanding use of digital machines. There are problems which can be more efficiently solved by the analogue computer than by digital methods, and each of these techniques has its own favored domain of usefulness[5, P. 2] [6, P. 3].

A vast amount of thought and technical work has gone into the development of modern electronic analogue methods. Bibliographies of pertinent literature are available[5, P. 369]. It is on the basis of this accumulated art that current computing begins. It is developed along a logical pattern to find analogue methods which are b e s t suited specifically to the use of transistors as

---

(2) (3). . . . Superscript numbers refer to references listed in the Bibliography.

active circuit elements in the computing system.

A concise and clear picture of the principles on which current computing operates is obtained by a direct comparion between this technique and the existing methods of voltage analogue computing. For this reason the dissertation opens with a side-by-side presentation of current computing in terms of the well-developed voltage-computing practices. It is well for the reader already to have a general knowledge of electronic analogue computing techniques, as the basic principles are not reviewed here, but further reference is made to prominent texts in the field.

When the similarities between voltage and current computing systems have been illustrated in each of the basic mathematical operations which these computers perform, the current-computing system is considered by itself. Certain properties of the system, such as the need for precision passive elements, the need for high amplifier gain, and the importance of frequency response are outlined as they bear upon current computing.

Since the date at which this investigation of current computing was begun, there have appeared several brief descriptions

of similar methods of using the current analogue. Two references in particular have considered this arrangement of circuit elements in a parallel vein (7, P. 419) (8).

In order to prove the main thesis, that transistors can indeed be used for analogue computing, the specific circuits which have been developed, and the test results of their use, are presented in summary form in a chapter entitled "Summary of Current-Computing Demonstration Results". From these concrete examples an appreciation is gained of the relative magnitudes of all system quantities, so that the analytic study which follows later has a typical numerical basis from which to resolve the capabilities of this system.

Since many of the system parameters, such as overall unit transfer function, depend on the active element used, that is, here, the operational amplifier, this unit is studied in detail. Two important results of the study have been: the evaluation of important properties which the transistor operational amplifier must have, and the determination of suitable means of achieving them. A chapter entitled "Operational Amplifier Design" describes the procedures and criteria which are used to obtain optimum effectiveness from available transistors.

Once an operational amplifier has been built which is as nearly ideal as possible, based on the properties just mentioned, its use in the computing system can be analyzed in detail. Each important parameter of the amplifier, such as current gain or bandwidth, will then have been measured and will be known in mathematical terms. By means of system relationships, the effects of each parameter on the accuracy of a computing unit, such as an adder, are predictable. The analytic relationships which express overall accuracy as functions of the parameters are discussed and developed in the "System Error Analysis" chapter and in Appendix IV. Accuracy is expressed in terms of the faithfulness with which the operational unit delivers a step-function signal at its output terminals. Practical values are cited for the transistor amplifiers whose properties have been measured in this study.

Typical decisions which a design engineer must make in the construction of useful hardware are described in the chapter of "Conclusions". Suggestions are made in general terms on how to obtain the best engineered equipment for practical applications having certain known or predictable characteristics.

System error analysis defines how transistor amplifiers must be built in order to operate satisfactorily and allow suitable accuracy in the current-computing arrangement proposed here. For an amplifier meeting these requirements, a workable system is described in detail, and the use of this system is shown to be potentially practical and effective.

In order that a complete picture be presented of the lines of attack and intermediate phases of this investigation, certain other topics have been added as Appendices to the main body of the report. These additional topics provide continuity to the study and they illustrate why major choices and decisions were made as to the direction the attack would assume. One major decision, of course, was that the transistors themselves have definite limitations for voltage analogue computing, and the reasons are discussed in Appendix II. It was also felt that some indication of the chronological order in which these study phases occurred would be illuminating and of historical interest.

The probability of greatly improved junction transistors soon being developed means that potential improvements and wide usefulness should be ahead for current-computing systems. As transistor frequency response is extended, for example, an

amplifier may be built having the same or greater bandwidth and more degenerative feedback. Such an amplifier will pass the analogue variable with improved faithfulness over present transistor amplifiers. Maximum signal excursions are also limited by present transistors. As units having higher allowable dissipations are developed, they may be applied to increasing signal power delivered to load or to the next computing operation or to a transducer, as the case may be. In summary, the methods of current computing seem to fit and utilize effectively the unique circuit properties of transistors.

CHAPTER ONE

Current-Computing Fundamentals

The basic building blocks of analogue computers are units which perform specific mathematical operations upon the variables. Typical examples of the most basic operations needed to fill a wide variety of applications are:

(1) Isolation (to prevent loading one computing circuit by another)

(2) Multiplication by a Constant (including change of sign)

(3) Summation (including subtraction)

(4) Integration with respect to time

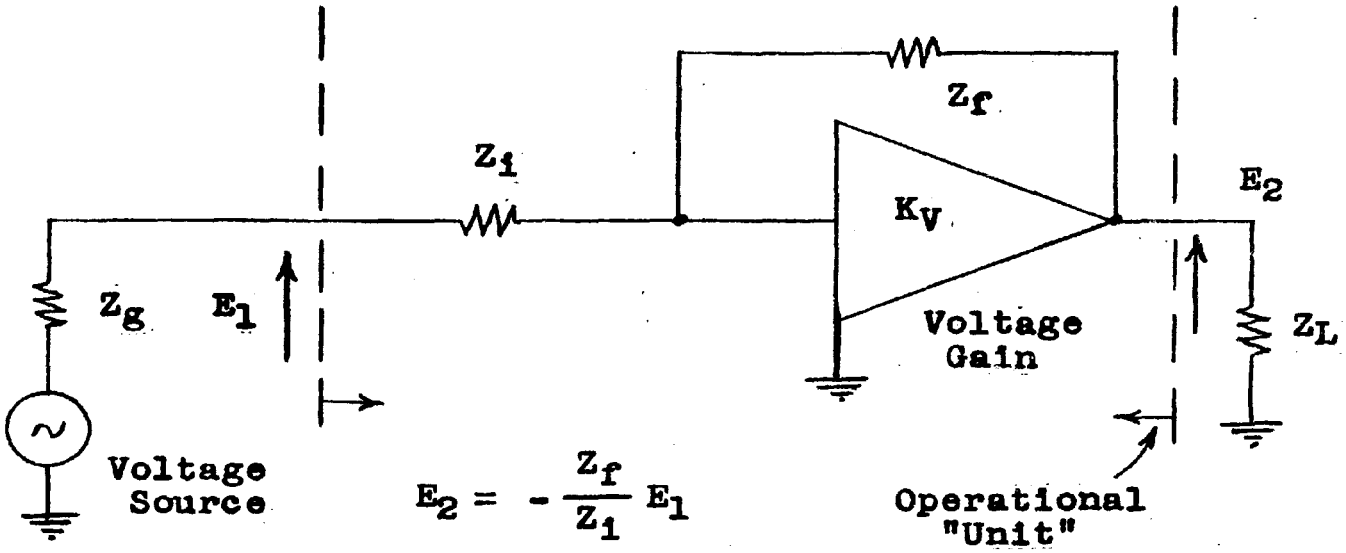
(5) Differentiation.

Figures 1-1 through 1-4, on the following pages, illustrate the circuit arrangements as they are commonly used for voltage analogue computing, along with the corresponding arrangement to perform the same operation when current is the variable.

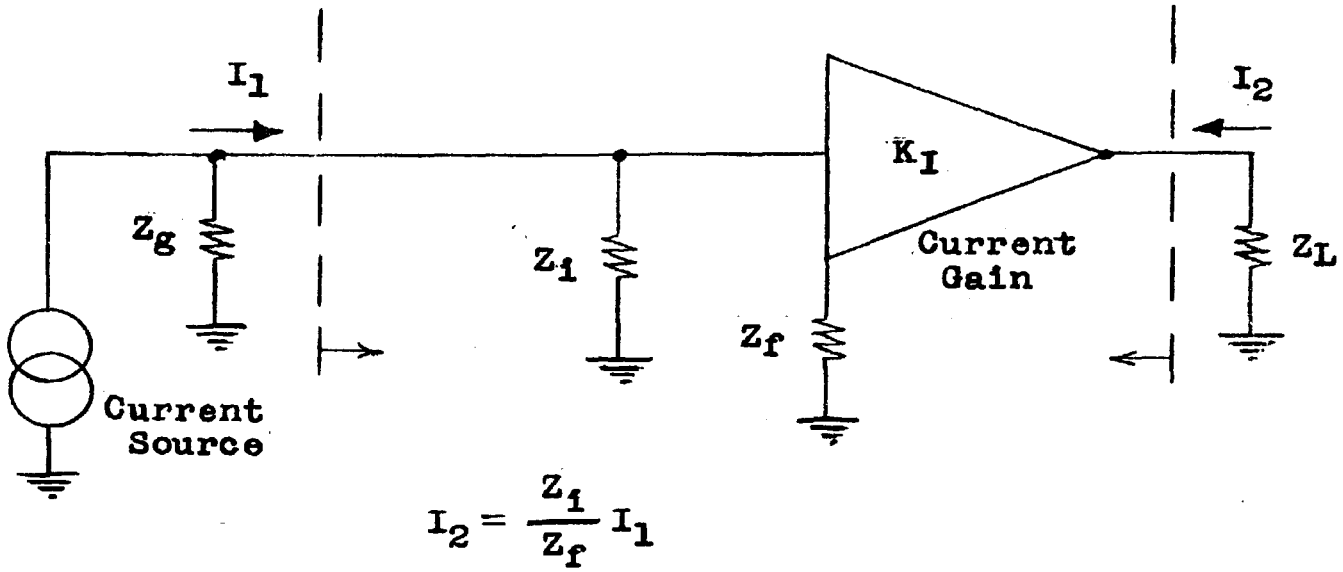
These four figures provide a broad descriptive picture of how the current-computing system functions. The operation is idealized here in simplest terms in order to show the principles.

ISOLATION AND MULTIPLICATION BY A CONSTANT

Arrangements of Amplifiers and Components



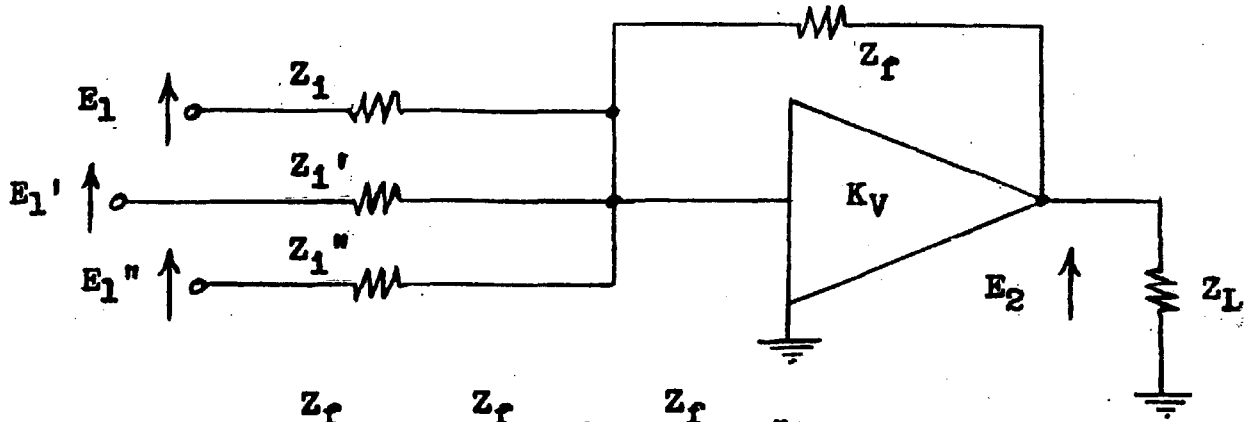
a) Voltage Analogue Computing



b) Current Analogue Computing

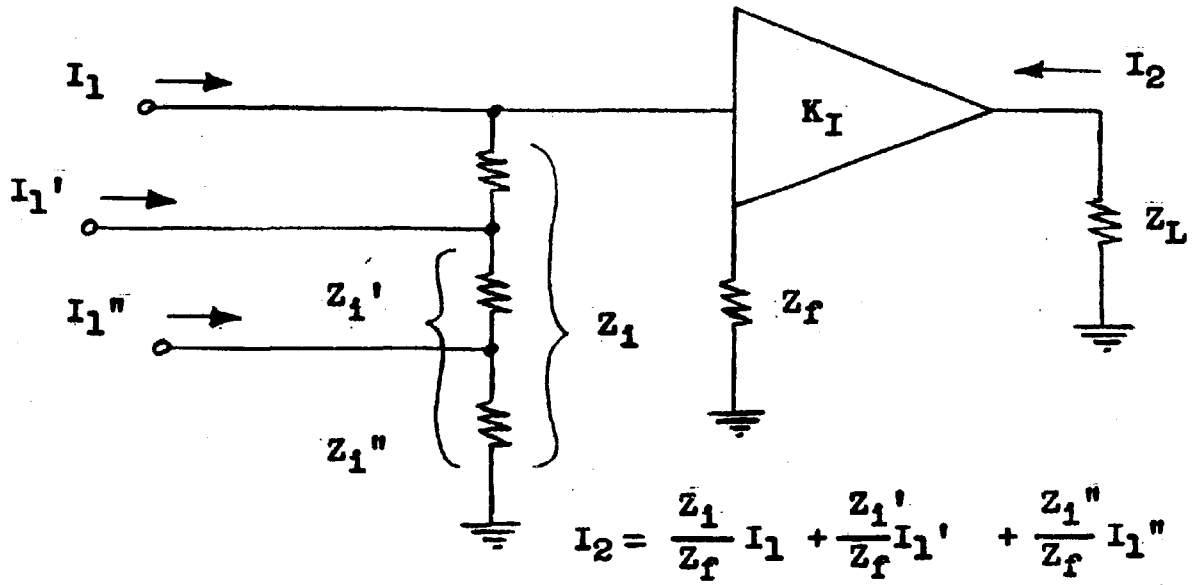
Figure 1-1

OPERATION OF SUMMATION



$$E_2 = -\frac{Z_f}{Z_i} E_1 - \frac{Z_f}{Z_i'} E_1' - \frac{Z_f}{Z_i''} E_1''$$

a) Voltage Computing



$$I_2 = \frac{Z_i}{Z_f} I_1 + \frac{Z_i'}{Z_f} I_1' + \frac{Z_i''}{Z_f} I_1''$$

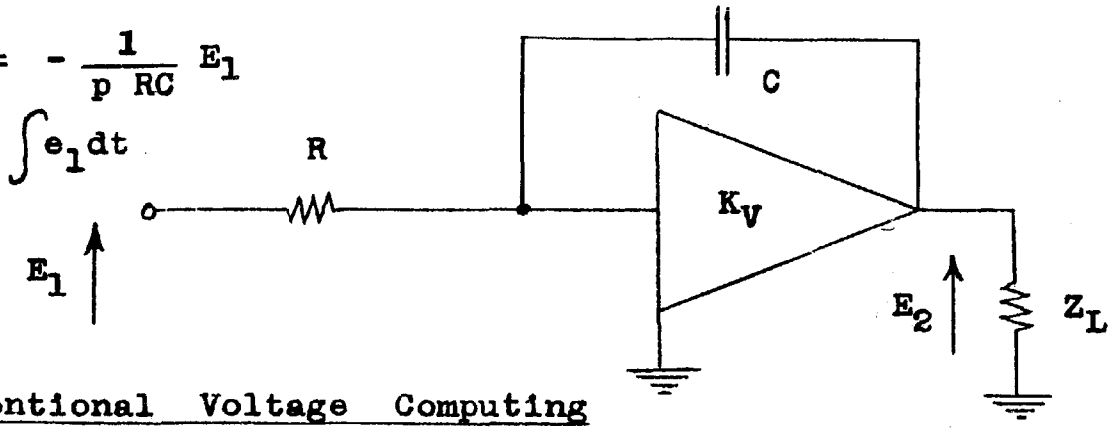
b) Current Computing

Figure 1-2

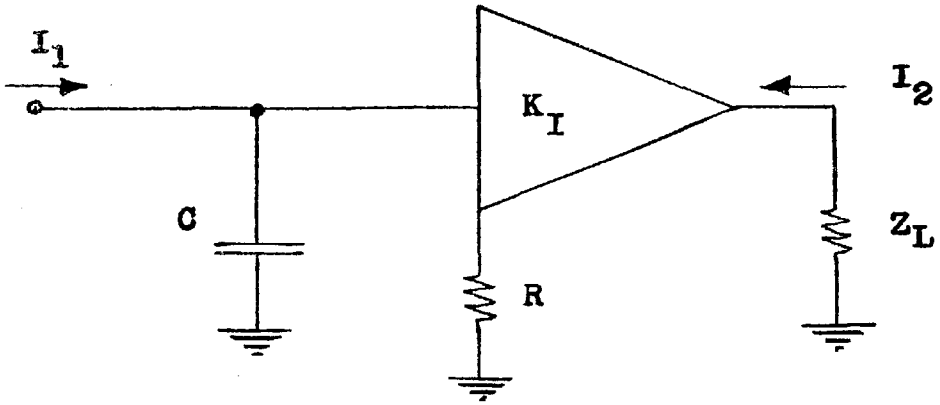
METHODS OF PERFORMING INTEGRATION

$$E_2 = -\frac{1}{p\,RC} E_1$$

$$e_2 = -\frac{1}{RC}\int e_1 dt$$



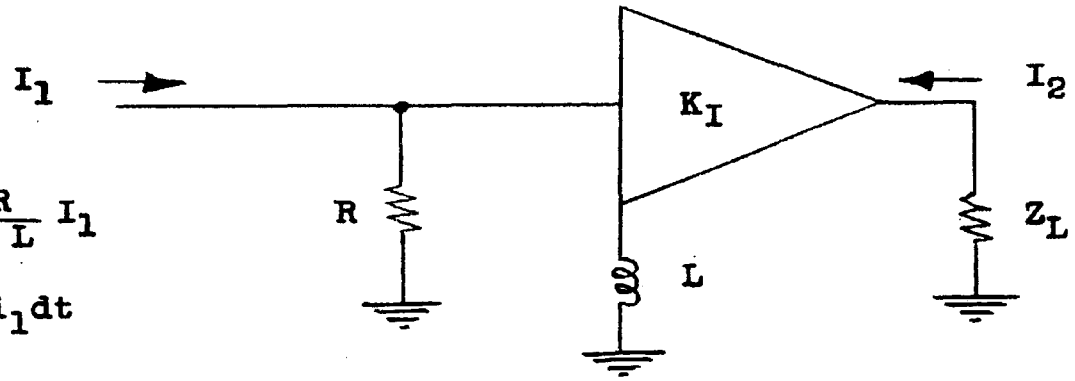
a) Conventional Voltage Computing



$$I_2 = \frac{1}{p\,RC} I_1$$

$$i_2 = \frac{1}{RC}\int i_1 dt$$

b) Current Computing with C and R



$$I_2 = \frac{R}{p\,L} I_1$$

$$i_2 = \frac{R}{L}\int i_1 dt$$

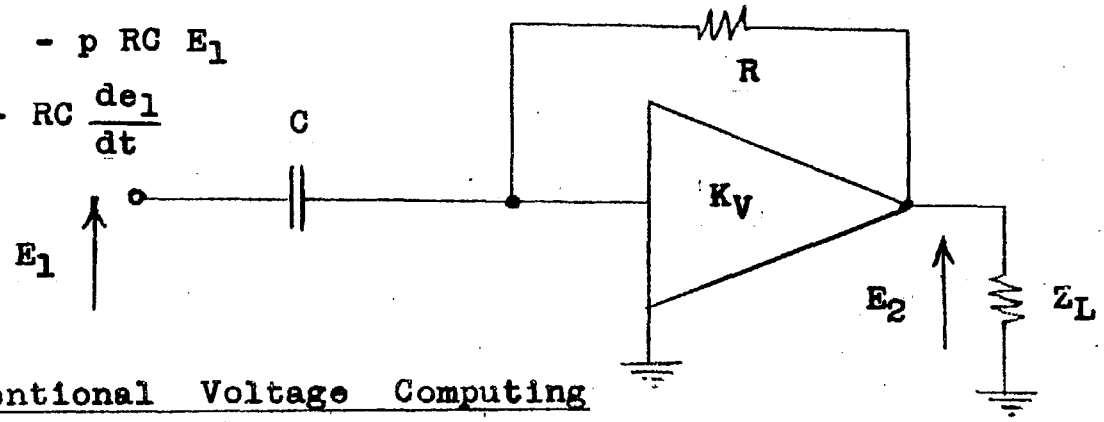
c) Current Computing with R and L

Figure 1-3

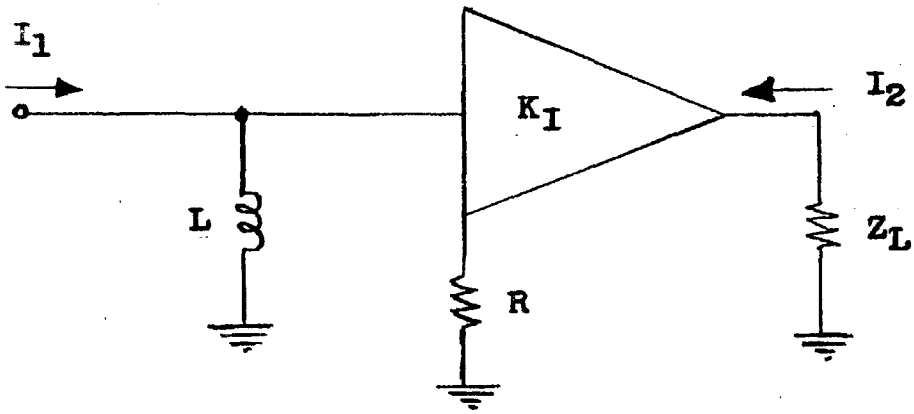
METHODS OF PERFORMING DIFFERENTIATION

$E_2 = - p\,RC\,E_1$

$e_2 = - RC \frac{de_1}{dt}$



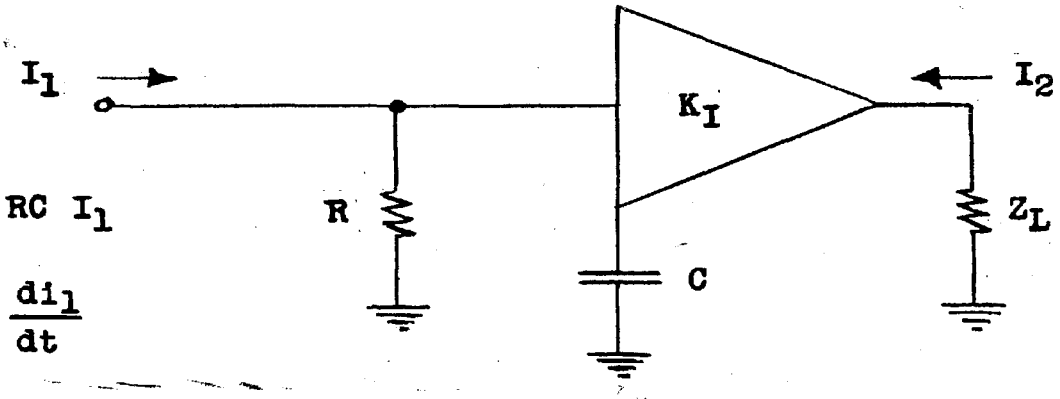
a) Conventional Voltage Computing



$I_2 = p \frac{L}{R} I_1$

$i_2 = \frac{L}{R} \frac{di_1}{dt}$

b) Current Computing with L and R



$I_2 = p\,RC\,I_1$

$i_2 = RC \frac{di_1}{dt}$

c) Current Computing with R and C

Figure 1-4

The relationships between the input and output voltages and currents, which are shown, represent the desired situations. These relationships are approximately brought about in actual equipment by the following design objectives.

Ideally the gains, K_V, and K_I, of the amplifiers are infinite in magnitude. The amplifiers' own input impedances should be: (1) infinite for voltage computing, and (2) zero for current computing. The equivalent internal impedances of the signal generators, Z_g, or of the preceding stages from which the operational units receive their inputs are: (1) for voltage computing, relatively much lower than the input impedance of the operational unit, and (2) for current computing, relatively much higher than this input impedance. The output impedances of the operational units are (1) much lower than the equivalent loading impedance for voltage computing, and (2) much higher than the load for current computing.

In Figures 1-3 and 1-4 the transform relationships between output and input variables are shown by capital letters, where "p" represents the differential operator. The lower-case variables show the instantaneous quantities in the time domain where initial conditions have been neglected.

The exact requirements of the so-called operational amplifier, which is represented in these figures for each system by the triangular block, will be discussed for current computing in more detail later. It will be observed now, however, that in all uses shown it is a three-terminal device, and it is the only active element within these elementary operational units of any large analogue computer.

It is important to note, also, the requirements that all passive circuit elements shown in these figures be of precisely known electrical properties. They are precision components, of known and stable electrical values, and they determine which operation each unit performs upon the variable. These passive elements often also largely determine the accuracy with which the operation takes place, that is, as long as the amplifier is suitably designed so as to introduce relatively little degradation in its role of active element.

It may be shown that the precision passive elements are capable by themselves of performing mathematical operations upon the analogue variable.[5, p. 11]. In general, however, unacceptable attenuation is suffered by the variable when passive elements alone are used. Some means of retaining input and

output signal levels of comparable magnitude, as well as simultaneously performing the desired computing operation, is necessary. It is often desirable to increase the output signal above the level of the input, so as to provide positive gain and to overcome circuit losses elsewhere in the system. An operational amplifier, such as is shown in Figure 1-1, will perform the desired and necessary function of maintaining or increasing the signal level. By proper design the amplifier will not contribute significant loss of accuracy.

The amount of overall gain needed from input terminals to output is determined by the scale factors of the variables, that is how signal amplitude is related to the magnitude of the equation variable which it represents. Naturally, the gain and scale factors of the system must be precisely known, as the amplitude of the signal contains the information which is operated upon; it is the basic system variable, whose value will later be carefully measured or used as one of the results desired from the whole computation process.

Figures 1-1 through 1-4 show side-by-side comparisons between the conventional voltage-analogue computing system and the current-computing method of performing similar operations.

These comparisons are important in that current computing owes most of its lore and its method of approach to the voltage-computing forerunner. The reason that current computing may start out with a reasonably workable system and avoid arduous searching and study in a given problem for optimum parameters, such as the impedance values and scale factors to be used, is that voltage computing has developed techniques of selecting these parameters for the problem.

It is an interesting and illuminating exercise, which will not be pursued here, to express the transfer equations of voltage computing in terms of admittances, and to note the close correspondence with the transfer forms of current computing as obtained, for example, in Figure 1-2.

One of the parents of voltage-analogue computing and, therefore an ancestor of current computing, is the theory of feedback systems and feedback amplifier design. The higher the gain of the amplifier in each analogue computing system, the more independent the mathematical operation may be made of some circuit imperfections. This subject is discussed in detail in the "System Error Analysis" chapter of this paper. For the present, however, it will be mentioned that often the precision passive

circuit components may be selected or adjusted to degrees of precision which make them relatively unimportant in determining the accuracy of the computing operation. For example, for laboratory use, temperature ovens are commonly used to help hold precision computing components, such as capacitors, at known constant values.

Amplifier gain is thus made very large in design, so that by means of large amounts of degenerative feedback any degrading effects of the necessary gainful elements can be minimized. A voltage-computing amplifier developed by E. A. Goldberg has a DC gain exceeding 150 million[4]. When the entire amount of this gain is used for subduing amplifier effects, the resultant gain of the computing operation will be of the order of unity. One benefit of such degeneration is the excellent isolation between operations which is afforded by virtue of the low output impedance which this parallel or voltage feedback causes. Output impedances of .02 ohms with this equipment are normal.

In order to achieve with satisfactory stability such very large feedback, Bode has shown that some inherent requirements of circuit amplitude and phase control must be met [9]. The term "overall stability" will be restricted for this report to the behavior

of one operational unit, that is, one computing amplifier with the associated passive components and load. Certain problems of stability in large-scale analogue computers involve large loops formed by many interconnected operational units. For these larger systems, which could be specified only for the particular problem being solved, it is important that remote and so-called "hidden" loops be considered to prevent regeneration and instability [10]. It will not be the purpose of this dissertation to analyze these individual overall systems; again the safety measures for current-analogue computing are similar in the broad sense to the precautions which are well established and used in voltage systems[2].

For current computing, no amplifiers have yet been built which have the tremendous gains, such as the voltage gain of 10^8, as are presently used in voltage computing. It will be advantageous to advance the current-computing gains to large values as soon as the state of the art permits.

In the meanwhile, the frequency response of the individual transistor has limited the maximum forward gain for stable operation which could be obtained in the amplifiers here. In general, each transistor has been assumed to a first approximation to act like a minimum-phase network whose upper frequency

response, as measured by current gain, drops asymptotically at six decibels per octave from the cut-off or "break" frequency. Although junction transistors have been measured to have greater than 90 degrees of phase shift at very high frequencies[7, p. 348], this effect usually occurs beyond the frequency at which gain is below unity, so that, for our purposes, the divergence of a single stage from similarity to the asymptote of a minimum-phase network causes no additonal restrictions.

An overall amplifier for many computing and resistive feedback applications may be designed for a net phase lag of 150° or less occurring within the band of frequencies where overall gain exceeds unity. This 30° "phase margin", from the condition of 180° phase shift where regeneration begins, is deemed good and necessary engineering practice to insure stability[9]. Similarly, since, for a multistage amplifier, the phase response exceeds 180° somewhere beyond the frequencies where gain has gone down to unity, it is good practice to make sure that gain is at least ten decibels below unity gain (i.e. 10 db below 0 db) where the 180° point is reached. The -10 db of gain here forms a "gain margin" at the phase reversal frequency. All amplifiers for analogue computing applications are designed for

adequate margins of phase and gain to insure stability under all conditions of feedback.

The "break" frequency, defined as the frequency at which the gain is three decibels below low-frequency gain, for single junction transistors depends on the method of manufacture and on physical properties which are only to a slight extend under the circuit designer's control. One exception to this rule exists in the junction tetrode described by the Bell Telephone Laboratories [11], but of which no samples have been obtainable. Available transistors have upper break frequencies of the common-emitter current-gain properties which are variously reported as being anywhere from 10 kc to approximately 60 mc, the latter being for Philco's surface-barrier transistors [12].

Measurements made of typical break frequencies for the current gain (α_{cb}) of RCA's type 2N34 PNP transistors yielded an average of 16.6 kc for twelve samples. This type of junction transistor has been used exclusively in all the experimental work on current computing which is reported here.

The steps which were taken to control current-gain and phase behavior, and to provide the necessary stability margins

in the transistor amplifier circuits which have been built, are discussed in a later section along with the design of the amplifier itself.

There are a number of other considerations which bear upon the basic system proposed here for current computing. Most of these are considered in greater detail with the two broad topics of Amplifier Design in Chapter Three and of Error Analysis in Chapter Four. The effect of the quality of the passive precision elements used is not, at the present time, a limiting factor in system accuracy. These topics just listed cover virtually the whole current-computing system with the exception of the arrangements themselves of active and passive elements to perform specific operations, which have been described here in this chapter.

CHAPTER TWO

Summary of Current-Computing Demonstration Results

The purpose of this chapter is to present in brief, summary form an overall picture of the results which were found by circuit tests and by systems analysis.

I. Circuit Models

The specific hardware produced in the course of this study is shown in the photographs of Figures 2-1, 2-2, and 2-3 on the following pages. These pictures show two models of the three-stage direct-coupled transistor circuit which was used as the operational amplifier for the qualitative test results which are shown in this chapter. The amplifier has been stabilized by phase-control networks for the application of approximately 60 decibels of feedback. This amount of feedback is sufficient to reduce the effects of the amplifier itself to a degree which allows computing with an accuracy suitable for many practical applications. As an illustration, when it is used with signals which have sinusoidal component frequencies of 100 cps. and less, the amplifier itself will introduce a peak instantaneous error into the

TRANSISTOR CURRENT AMPLIFIER

CARD MODEL

Front View

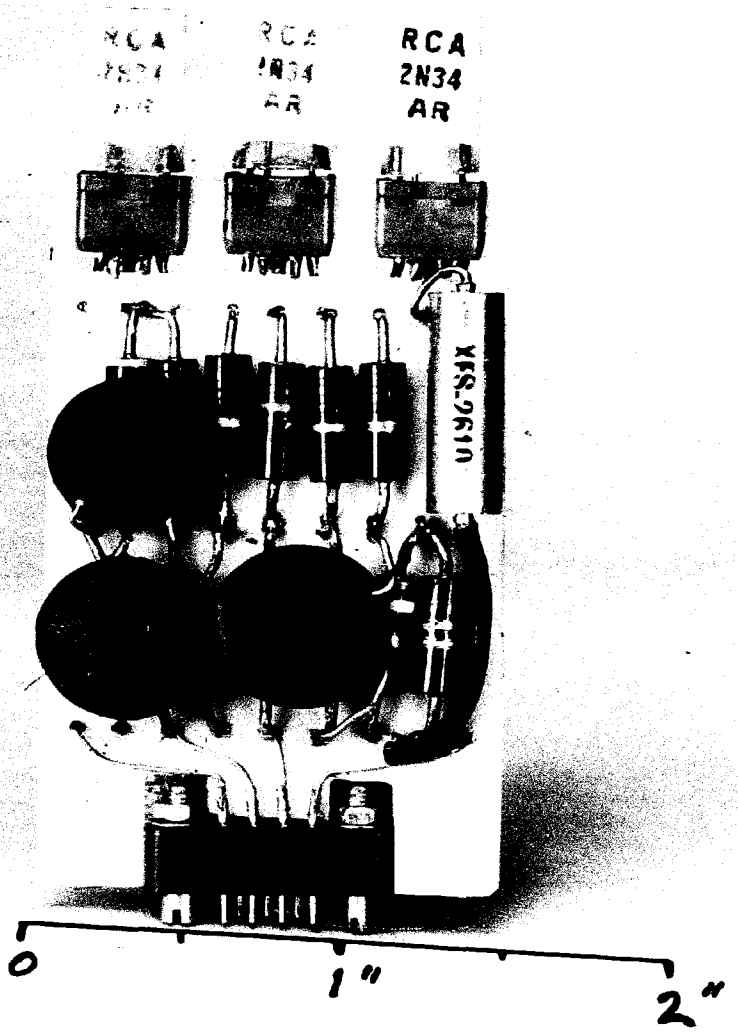


Figure 2-1

TRANSISTOR CURRENT AMPLIFIER

CARD MODEL

For Printed Circuits and Dip Soldering

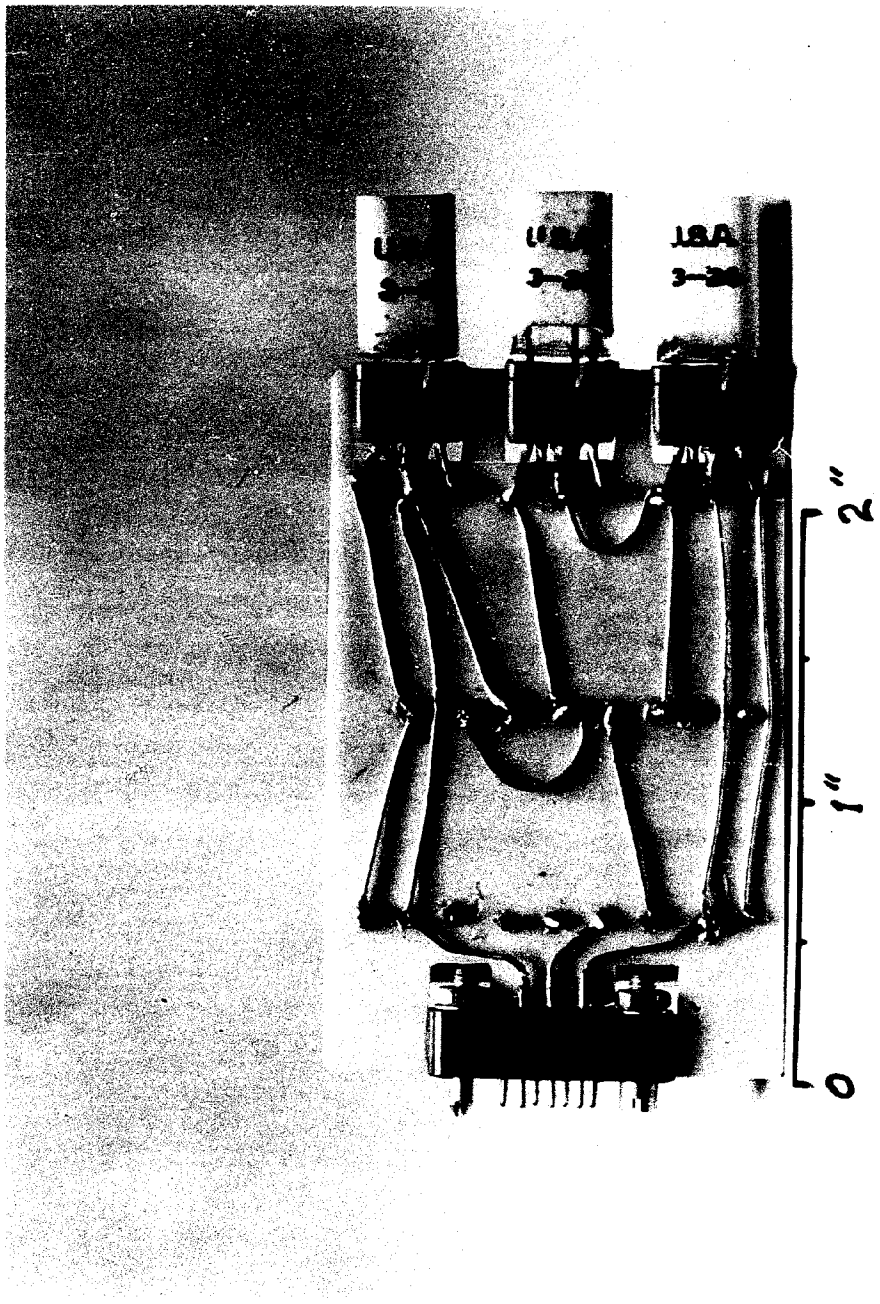


Figure 2-2

TRANSISTOR CURRENT AMPLIFIER

ENCAPSULATED MODEL

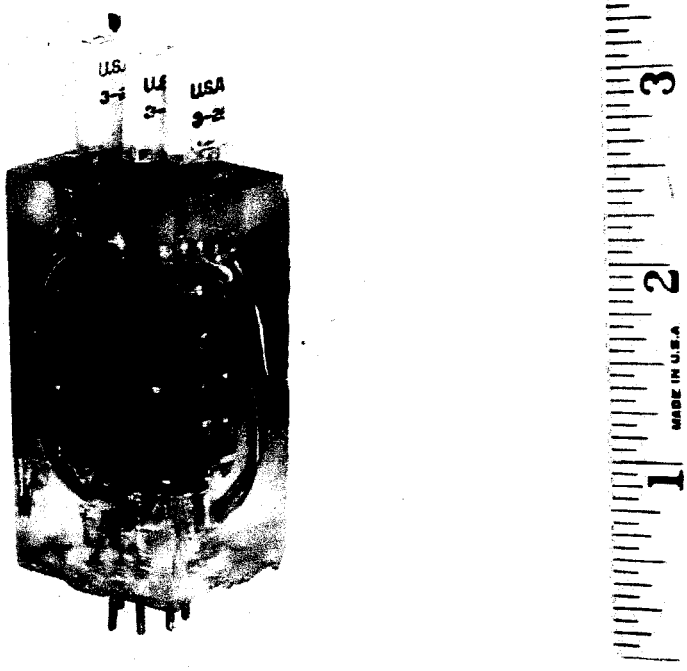


Figure 2-3

operation of summation, for example, of less than a quarter of one percent.

The schematic diagram of this amplifier is the same, except for stabilizing network values, as that shown in Figure 3-1.

Figure 2-2 shows that the layout may easily be adapted for printed circuit and dip-soldering techniques of manufacture. Figure 2-3 shows another model of the same circuit, which has been potted in clear resin for protection of the circuit elements from moisture and shock.

In any final application, a large number of identical amplifiers will probably be required. These two models utilize space and power efficiently, so that many amplifiers can be mounted side by side, . In such an arrangement the amplifiers can be individually withdrawn for test, each as a unit with its own transistors. A simple test jig can be provided to measure the performance of one amplifier at a time.

The amplifiers in Figures 2-1, 2-2, and 2-3 have power gains of greater than 60 decibels. This magnitude does not represent the utmost capabilities of the transistors, since some

gain has been used degeneratively within the amplifier to accommodate transistors of widely divergent characteristics. The transistors and the components within each amplifier unit dissipate a total of 46 milliwatts.

The amplifiers have been designed primarily to provide a large value power gain, and secondarily to have the other desirable characteristics which are described in the chapter on "Operational Amplifier Design". One peculiar and important feature is the design for an intentionally low input resistance, nominally 1000 ohms, in this particular circuit.

These operational amplifiers were designed for use in a whole system having a nominal impedance level of 1000 ohms. That is, the load and summing resistances should be of approximately this value for such operations as scale-factor change, isolation, and summing. Impedances used in the other operations of integration and differentiation will also usually be of this order of magnitude in the principal frequency range of interest. The reason for this choice of impedance level is outlined in the chapter on amplifier design.

The amplifier shown in Figure 2-1 has been demonstrated and widely tested in current computing. Although a number of specific criticisms can be made, this unit demonstrates qualitatively, and to a degree quantitatively, that current computing is a useful and a powerful method.

Figures 2-4 through 2-8 show the qualitative results. In each figure four waveforms are shown which occur at four important points in that operation. These voltage waveforms were photographed directly form an oscilloscope located at the points shown, and from these voltages the currents which flow in the various leads may be inferred. From a calibration of the oscilloscope's vertical sensitivity and from measurements on these photographs the currents can be estimated to an accuracy of five to ten percent.

The operation of integration may be performed either as shown in Figure 2-5 or as in Figure 2-6. For the particular time scales and components illustrated here it is observed that resistance-capacitance integration provides the expected output shapes more closely than does the resistance-inductance arrangement. In the latter a noticeable curvature occurs in the output

Example of Summing and Scale Change

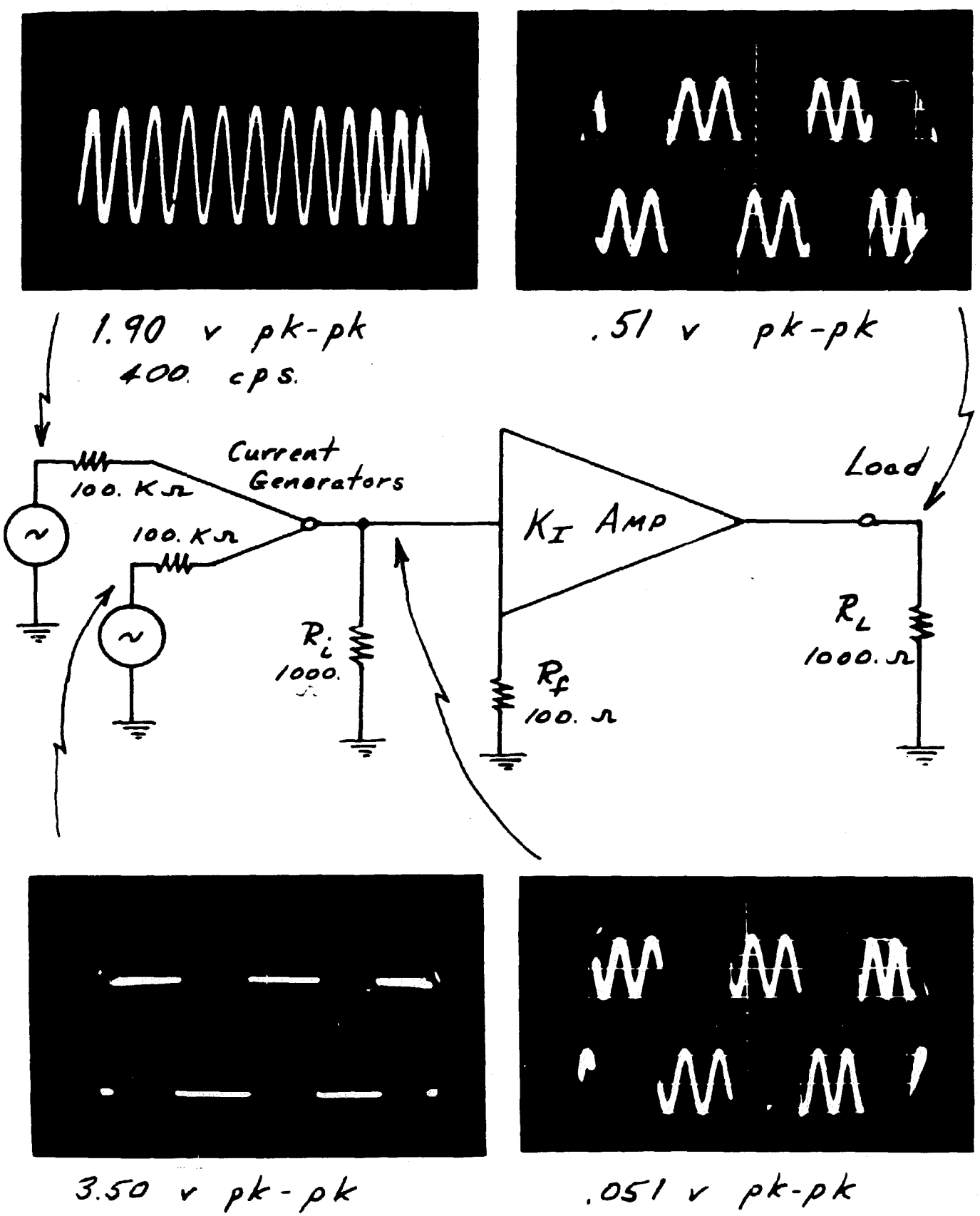


Figure 2-4

Example of R and C Integration

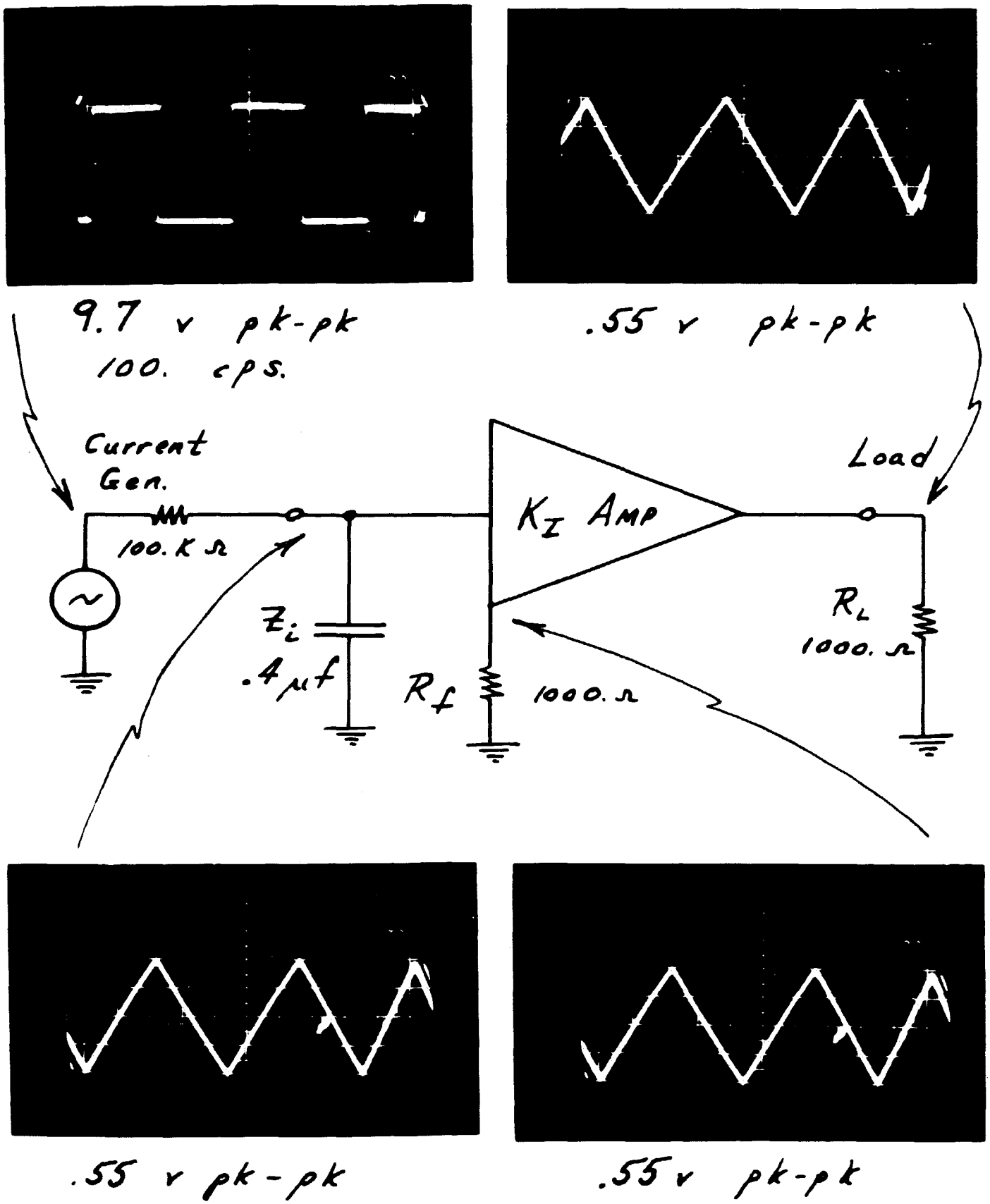


Figure 2-5

Example of R and L Integration

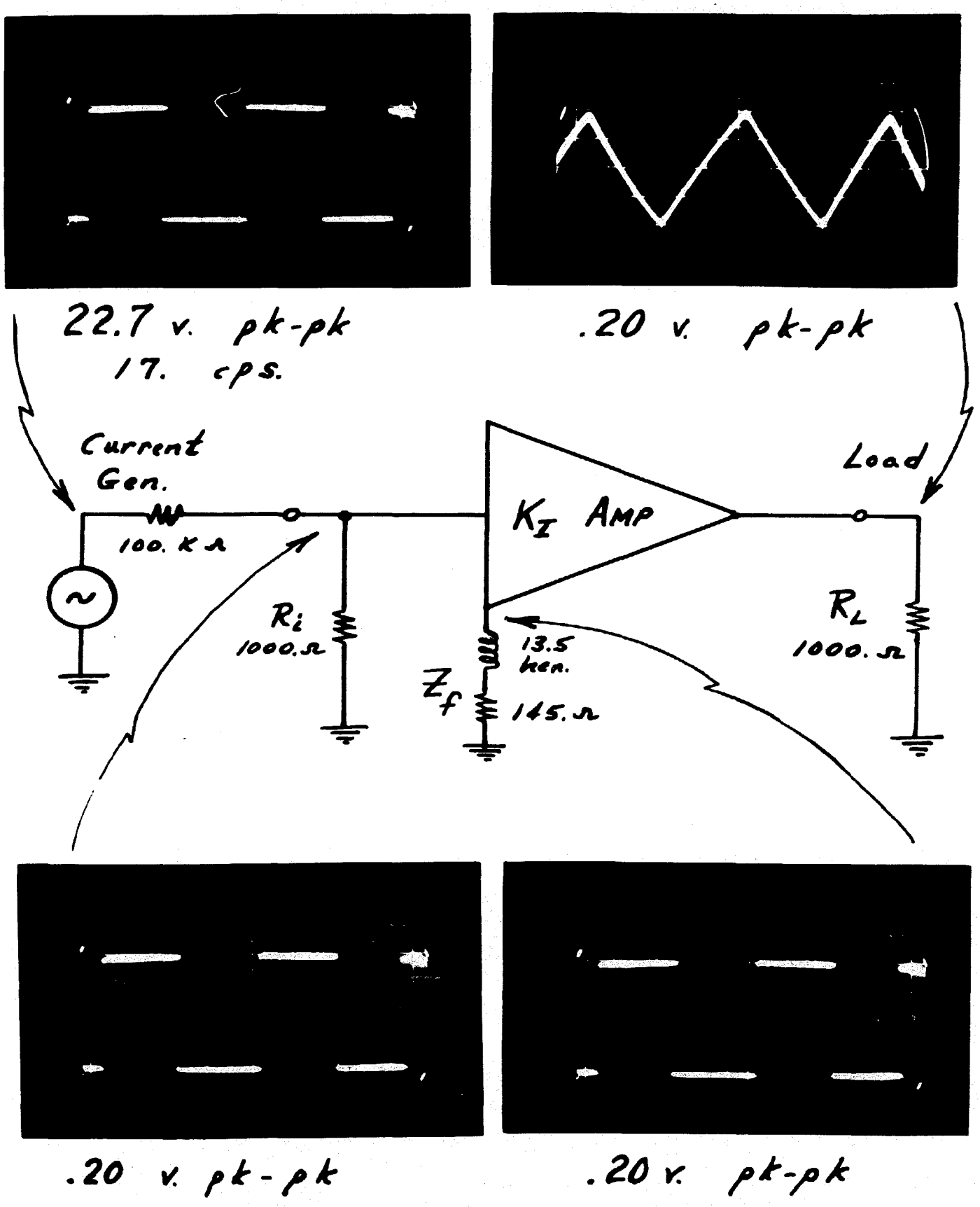
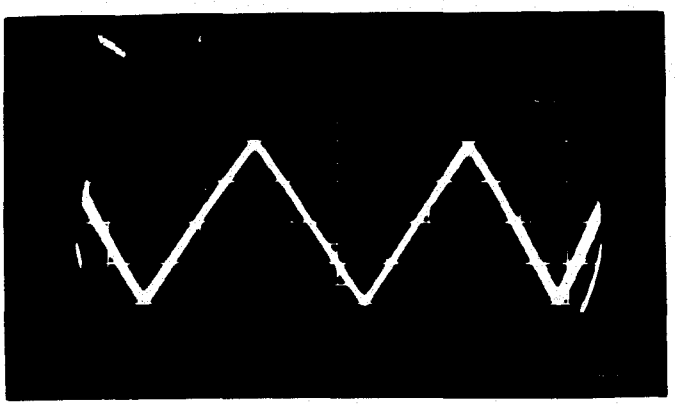
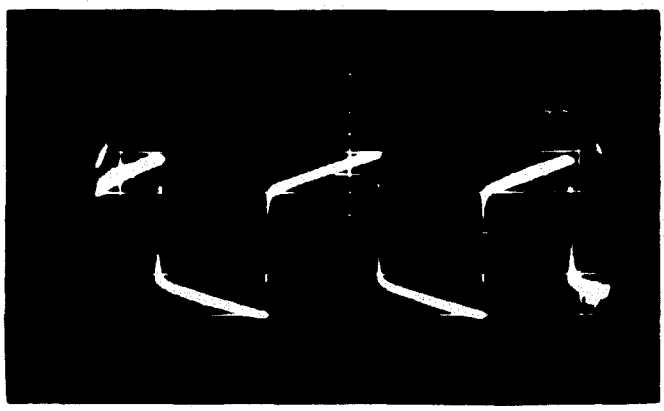


Figure 2-6

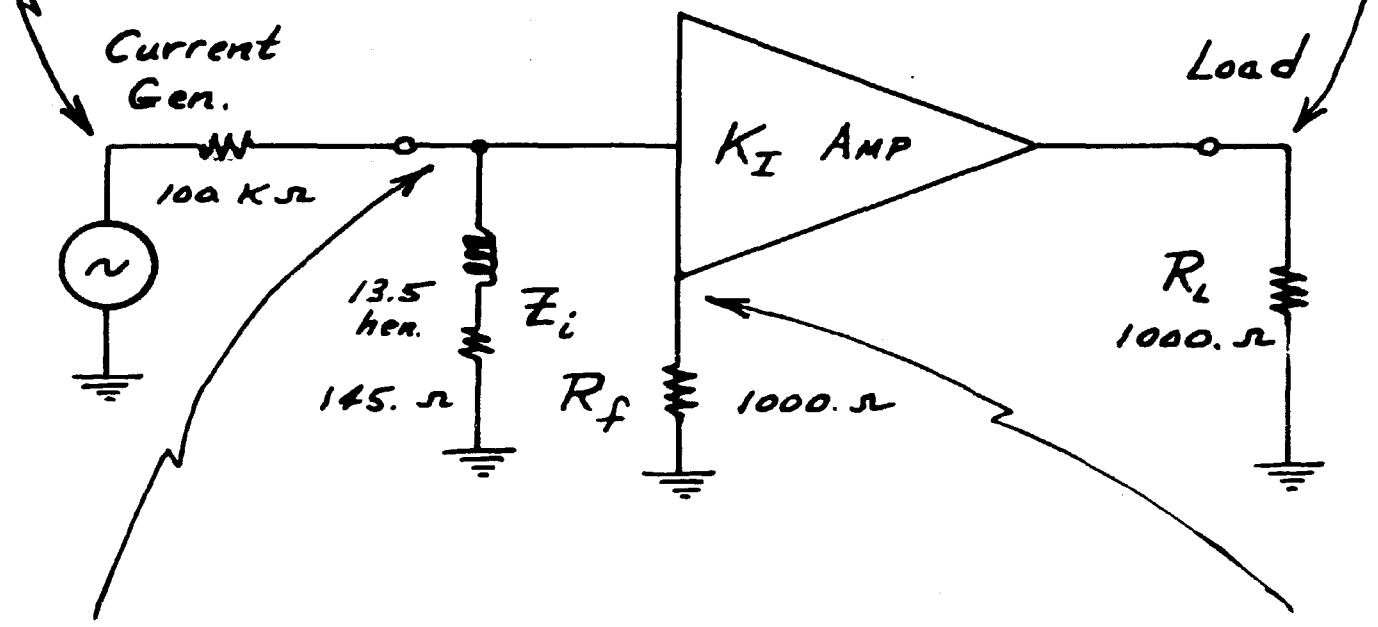
Example of R and L Differentiation

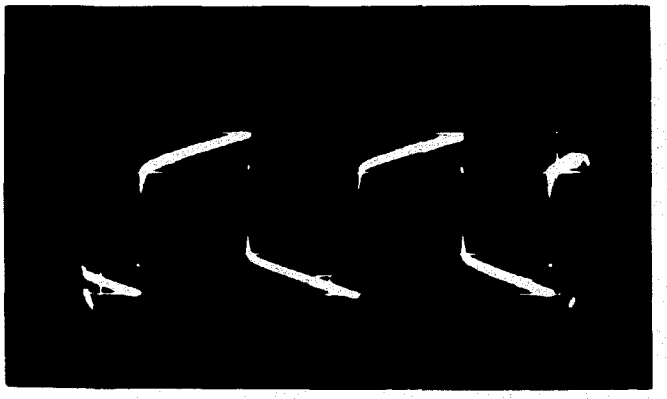


45. v. pk-pk
10. cps.

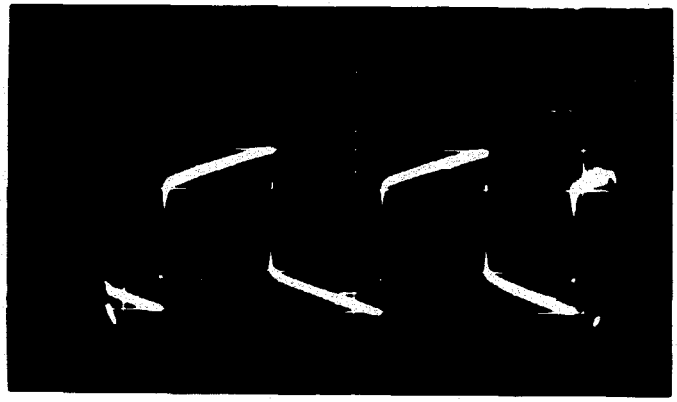


.31 v pk-pk





.31 v pk-pk



.31 v pk-pk

Figure 2-7

Example of R and C Differentiation

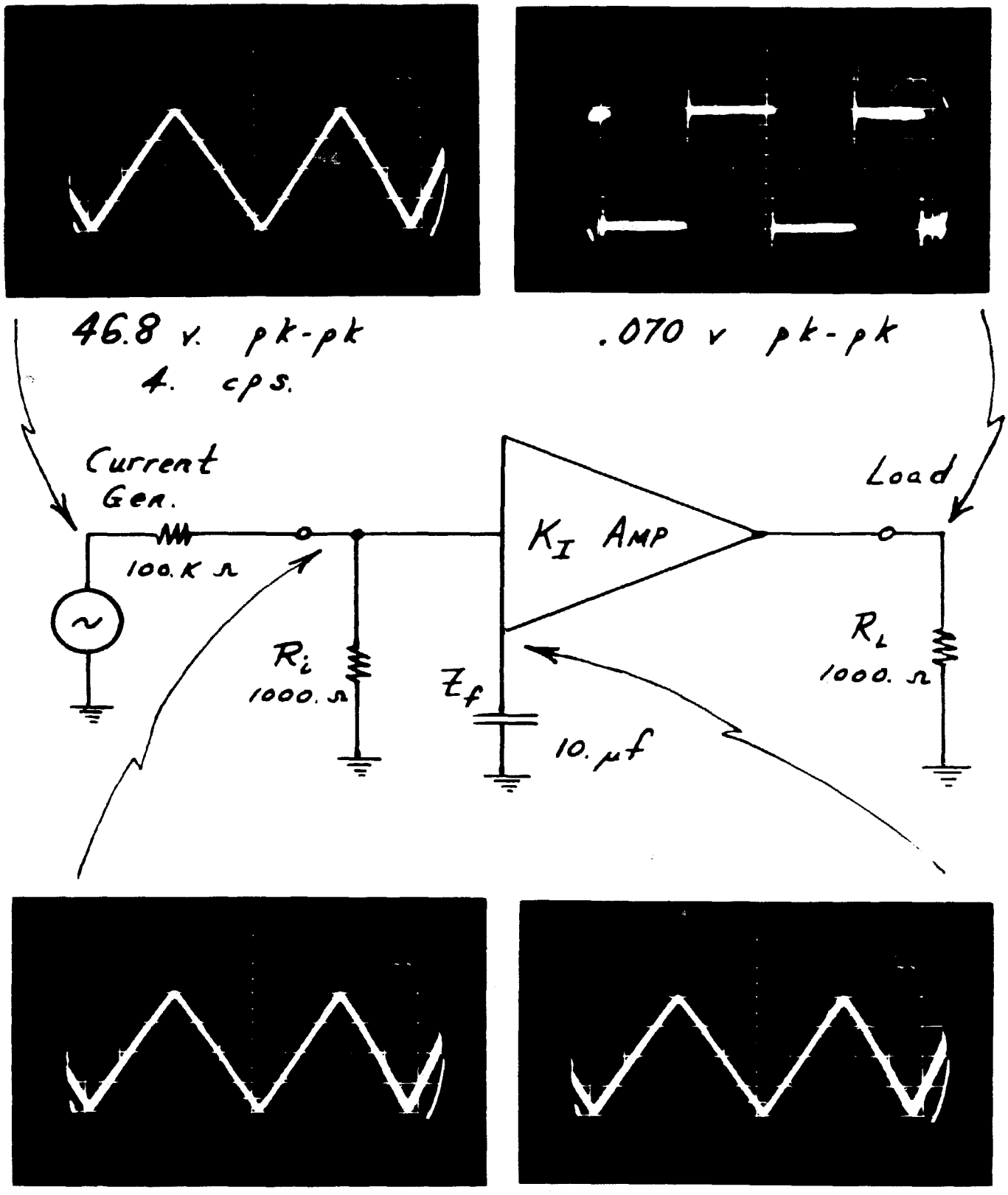


Figure 2-8

signal's rise and fall. In each of these figures the time scales and components have been chosen to provide a peak-to-peak output of the same order as the input signal size.

Differentiation similarly permits a choice of methods which are shown in Figures 2-7 and 2-8. This operation might typically be used in radar applications for calculating the rate of change of coordinate variables. An interesting feature shown qualitatively by Figure 2-8 is the oscillatory ringing which occurs at the output's rising and falling edges. The criteria for system stability are discussed later, and the conditions are defined where computing impedances and amplifier response can interact to yield instability. The rate of decay of the ringing transient is a measure of the system stability in this particular connection.

Figure 2-7 shows that considerable imperfection in the differentiation process occurs as a result of resistance within the reactive element. The voltage waveforms at the amplifier terminals should all be flat-topped, square waves for true differentiation of the input triangular waveform. A measure of quality for the reactive element used in all these operations is the concept of "Q" or, inversely, the power factor of the single component. The fact that it is much easier to obtain a low power

factor in capacitors than in inductors means that performing these operations by means of capacitive reactances is as a rule preferable if physical sizes and stability remain reasonable.

The photographs and measurements of Figures 2-4 through 2-8 show some of the necessary considerations, such as the importance of stability and power factor, which will be brought out in more detail in the following chapter.

II. Specifying Accuracy

The second major result of the thesis work has been the establishment of a useful method of measuring and specifying the computing accuracy of a single operational unit. For this method the system's relationships are expressed analytically, and known, measured parameters are inserted. From such a procedure the projected accuracy of this computing system may be determined in each of the likely applications. An important effort has been directed toward finding an adequate definition of computing accuracy and a general presentation of it. The method of error analysis which seems best for use here and which is convenient for many practical uses is discussed in detail in the chapter on "System Error Analysis".

The expression of system error in terms of the root-mean-square value of error taken over a whole interval in which the computer solution is observed seems to serve these needs. A familiar wave for analytical purposes is chosen. The system input is made a mathematical function chosen to deliver ideally a step output of current. The generator is assumed to have an infinite bandwidth. The difference between the ideal and the actual outputs is determined for each operation as a function of equipment and waveform variables, and a fractional error is found. The derivations are carried out in Appendix IV. Typical curves of this RMS error are shown in Chapter Four for the parameters of the circuits tested to date. The most important of the recognized sources of error are included in the analytic system relations which operate upon the input signal. The behavior of the system in producing nearly a step output waveform seems to show very well the individual effects of the various important error sources.

The numerical results of error analysis shown in Chapter Four can be improved in the design of future equipment, partly because the calculations which went into these curves serve to point out the goals that must be sought in designing each component

of the computing system for improved accuracy. A prime example is that of amplifier input loop resistance, R_{11}, which must be made as small as possible for optimum accuracy. Although this fact had been intuitively appreciated up to this point, now the exact effect of R_{11} on system errors can be established. The need for low input resistance is easily met by transistors, and their intrinsically low value may be accentuated by such devices as sub-loop feedback.

It should be noted that the approach to error analysis used here for current computing is applicable to other analogue computing systems. An RMS criterion of computing error averaged over the interval of computation is useful generally in problems of complex waveshapes. The data presented in Chapter Four form a definite part of the results of this investigation, somewhat less for the numerical values than for the method which they summarize. From curves such as those given there it is easy to select some of the parameters which ought to be optimized in a specific application. For example, if short pulses must be faithfully manipulated, some improvement in the bandwidth must be obtained, possibly at the expense of permissible feedback magnitude. Time scales for optimum utilization of the computing components may be interpreted from

a plot such as is presented and discussed in Chapter Four.

III. Assuring Stability

Another important aspect of current computing has been investigated, namely the determination of the stability criteria for single operational units when they are used with any of the possible impedance combinations. This study is especially important for amplifiers using transistors because of the restrictive upper-frequency limit and phase shift of present samples. The Nyquist criteria have been applied to finding just what impedance values are permissable in conjunction with the amplifier frequency and phase responses. An analytical method, which is based on assuming a continuous function for amplifier response, and a graphical point-by-point method of applying these criteria are suggested. These methods are described in Chapter Three.

IV. Using 4-Terminal Network Methods

A device or technique which has aided greatly in defining the design objectives of operational amplifiers for the current-computing system has been the use of an equivalent 4-terminal

network. The amplifier itself is assumed linear and it is conveniently represented for small signals by this combination of lumped, active and passive impedances. A natural extension, from use with just the amplifier, is to show how the whole operational unit, including precision elements, may also be considerably simplified into an equivalent 4-terminal network. The methods developed, along with useful formulae and typical values, are given in Sections III and IV of Chapter Three.

V. AC Computing Amplifier

As a prologue to the design of direct-coupled operational amplifiers, some AC-coupled transistor amplifiers were developed and tested for current computing. The effect of the minimum useful low-frequency response inherent in AC amplifiers is to restrict the range of time scales which may be used in analogue computing. Such amplifiers are far easier to build with transistors because of the isolation between bias and signal circuits, and they are recommended wherever the computing time scale permits.

One of these AC amplifiers is described in Section III of Appendix II.

VI. Chopper Stabilizing

Drift has been measured as being of secondary importance in the DC transistor amplifiers built here. These tests have, however, been at room temperatures only. The effects of temperature upon the leakage currents of germanium junction transistors are significant[7. p. 169].

It is felt that adequate operation at elevated temperatures can be obtained by employing the chopper-stabilizer principal of Goldberg[4]. The 400 cps. chopper and AC amplifier combination which is discussed in Chapter Three has maintained, within three decibels, its room temperature DC gain when elevated to 85° C. This supplementary amplifier will be highly effective in minimizing the effects of temperature when used in conjunction with a direct-coupled basic amplifier such as was used for the current-computing tests. Such a chopper-stabilized composite unit has been tested in principle, but it has not been exhaustively investigated for temperature behavior. This technique seems promising for critical applications.

VII. For the Future

The brief chapter which appears later, entitled "Conclusions", forms an important part of the results of this study. It is largely on the points listed there that further work on current-computing will be based.

CHAPTER THREE

Operational Amplifier Design

The discussion so far has been general in nature, and it has shown how the various elements of a current-computing system can be fitted together to perform a specified operation, such as summation, integration, etc. Some of the general requirements imposed upon the precision passive circuit elements have been listed. The next step will be to investigate the properties of the active circuit elements in detail, in order first to note just what properties are important to effective analogue computation with current as variable, and second to show how these are achieved in transistor circuit design and in reduction to practice.

I. Basic Considerations

Many of the properties of the computing amplifier which have been found important in voltage-analogue computing will be transferred directly to the current-analogue counterpart. Examples of the desirable properties which are common to both systems' computing amplifiers are:

(1) Stability of Gain, (namely Power Gain in both systems) as a function of time, of ambient temperature, of power supply variations, of vibration or acceleration, of humidity, and of other physical factors.

(2) Freedom from systematic circuit noise, in that the amplifier must not contribute unwanted signal, such as hum or transients, to the desired signal in significant amount.

(3) Maximum open-loop bandwidth of frequency response, which is consistent with unconditional circuit stability when the feedback loop is closed, as prescribed by the specific operation being performed.

(4) Maximum range of signal excursion at the output of the operational amplifier. For DC operation this range is usually symmetrical about zero output voltage and current. A range of load resistances which the amplifier may drive is always specified.

Other circuit properties which are required by the choice of current as analogue variable are:

(1) Low amplifier input impedance;

(2) High amplifier output impedance;

(3) Isolation of the amplifier and its power supplies from the computing system ground terminal,

II. DC Transistor Current Amplifier

The schematic diagram shown in Figure 3-1 describes the most successful attempt to date to achieve all these objectives. It has been built and tested in the laboratory. The measured frequency responses of the current-gain magnitude and phase are presented in Figure 3-2. These curves are used and discussed in the Stability section of this chapter and in the Error Analysis chapter. In Figure 3-3 on a following page are tabulated the important electrical properties of this particular current amplifier design. The circuit developed here does not represent the ultimate capabilities of transistors, as a number of practical compromises have been necessary.

It will be noted that considerable degenerative feedback is used around each of the three common-emitter stages in the form of low-valued resistors shunting between collector (output) and base (input) of each stage. Because of each stage's phase reversal, each shunt forms a parallel or voltage feedback path. This type of feedback lowers the stage power gain and lowers

TRANSISTOR CURRENT AMPLIFIER TESTED

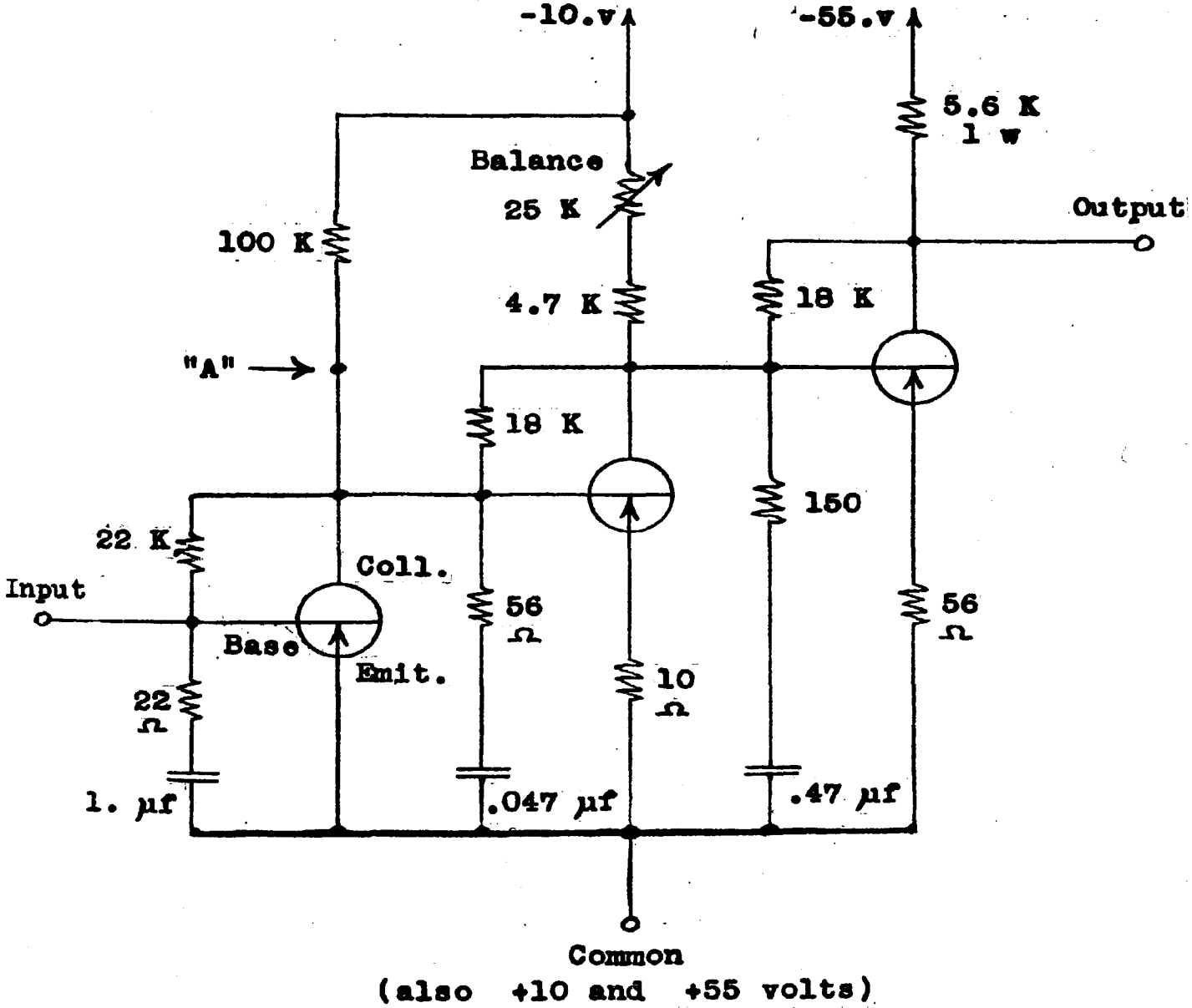


Figure 3-1

MEASURED OPEN LOOP RESPONSES OF CURRENT AMPLIFIER

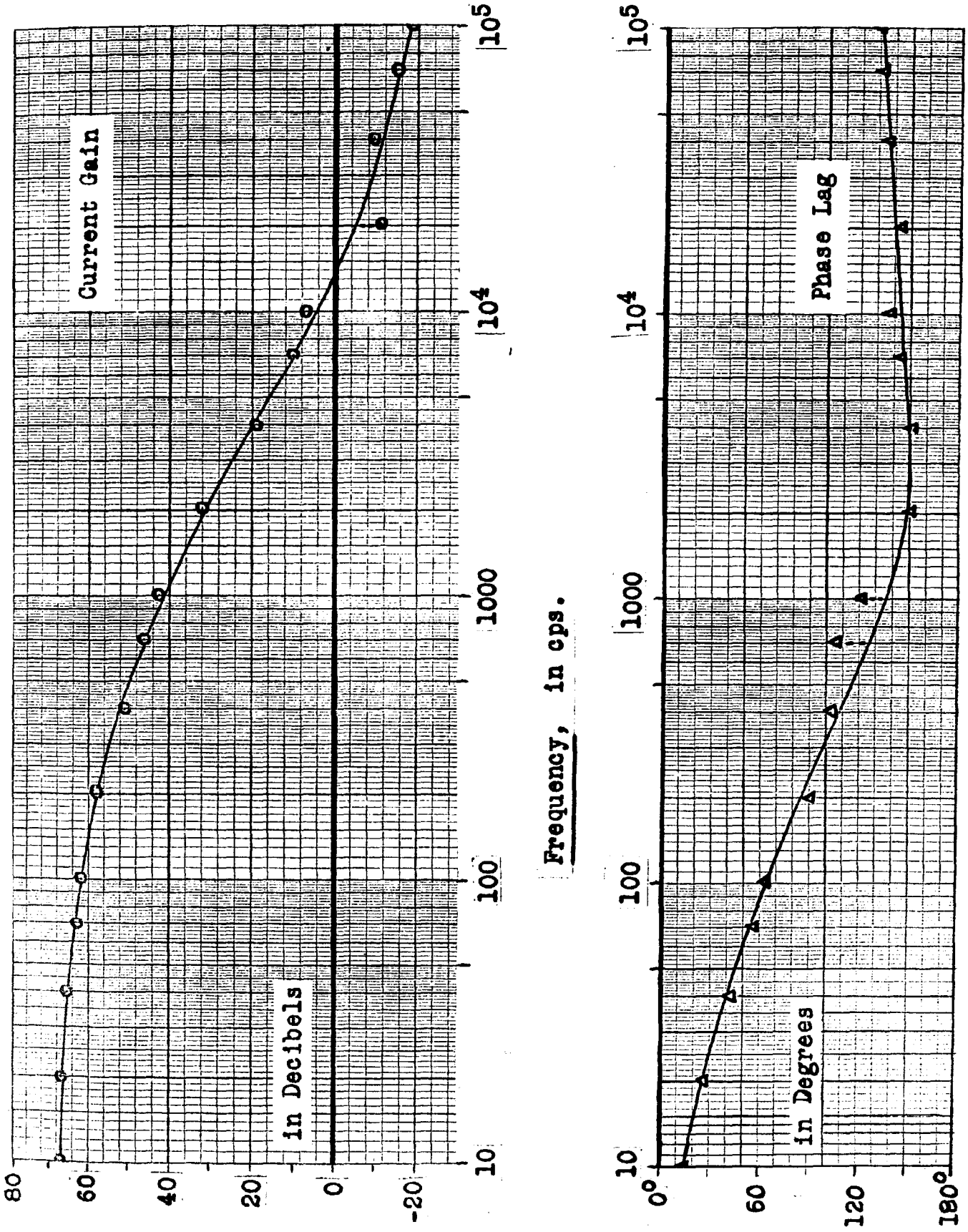


Figure 3-2

Table of Technical Specifications for Transistor DC Amplifier

Schematic diagram in Figure 3-1

Gain and Phase responses in Figure 3-2

Number of transistors	3
Type transistor	RCA 2N34 *
DC current-gain, K_{I_o}	- 2360.
Gain down 3 decibels	65. cps.
Supply power input	460 milliwatts
Maximum current output	$\pm$ 7.5 milliamps
Nominal loading resistance	0 to 2000 ohms
Phase angle at unity gain	142°
Frequency of phase reversal	> 100. kc
Input resistance	3200 ohms

This is the best transistor DC amplifier which has been built for use with, and tested in, the current-computing units to date.

---

* The RCA type 2N34 transistor is a low-power, low-frequency, diffused-junction, PNP transistor. These circuits may be adapted with slight changes for similar types and for later versions of this type transistor.

Figure 3-3

its input and output resistances. The principal advantage of the feedback is great reduction of the dependence of performance upon the individual transistor's properties. At the present state of the transistor art, it was felt that individual-stage DC feedback is necessary so that each transistor will automatically assume an operating point in a linear region of its characteristics. This feedback applies as well to all signals, and so it assures stable stage-gains. Open-loop frequency response is also appreciably improved by the feedback, although overall degenerative feedback would be equally effective in this regard.

The schematic diagram of Figure 3-1 is shown for battery-supply operation. By means of some revisions this circuit may be operated from a single power supply of -100 volts. Circuits have since been designed to operate this same amplifier from a single and considerably lower voltage supply by means of transistor current and voltage regulators.

The forms in which a similar amplifier circuit has been constructed are shown in Figures 2-1, 2-2, and 2-3. The waveforms of Figures 2-4 through 2-8 were obtained from the amplifier of Figure 2-1 when battery operated. Several direct-coupled transistor amplifiers were built, based on the results of work on the

AC amplifier which is discussed in Appendix II.

The common-emitter transistor connection has been chosen for all stages of the amplifiers for current computing, because it affords the greatest power gain per stage of the various possible connections. For the transistor type used here, and in the particular circuit used, this connection provides a stage having approximately 1000 ohms input impedance and 10,000 ohms output impedance. Individual stage feedback somewhat modifies these values. The fact that several (here three) such stages are essentially iteratively cascaded means that the output impedance of one stage and the input impedance of the next are not matched, and some signal attenuation necessarily occurs.

The impedance level at the amplifier input and between stages is thus of the order of 1000 ohms for low-frequencies. This amplifier operates satisfactorily for current computing when the summing and feedback impedances, Z_i and Z_f, are of this order. Appendix IV shows the effects of impedance magnitudes upon accuracy. It is on the basis of these effects that the choice of all unit impedances is made to compare with the magnitude of the input loop resistance, R_{11}. They are made roughly one to several thousand ohms in this case.



It is to be noted that it is not this low impedance, R_{11}, which loads the voltage signal appearing across the summing impedance, Z_i, as, for example, in Figure 2-5. Z_i, here a capacitor, is loaded by an effective impedance of the current amplifier with series degenerative feedback. Such feedback greatly magnifies the impedance which appears between the input terminal and ground. This effect of the amplifier in multiplying its input impedance is described quantitatively in Section III by Equation (3-9b).

Great care has been exercised in gain and phase control for this circuit to provide sufficient high-frequency stability margins with feedback. The shunting type of RC control networks is used. The effects of the networks are included in the plot of the frequency responses which are shown in Figure 3-2 for the DC amplifier tested here.

The method of selecting these networks is described in Section VI of this chapter. The design is based on measured analytic properties of this particular amplifier circuit. It represents a reasonable approach to the optimum network design, where as little as possible gain and bandwidth are sacrificed for assured stability (9).

No visible noise has been found by oscilloscope measurement on the amplifier's output signal for the condition of essentially an open circuit input (which will be the condition approached in practical current-computing operation). At somewhat higher current gains, namely, above 80 decibels, random noise has been observed. Wider bandwidths would increase the noise problem for these present transistors, but is expected that improvements in transistors themselves will keep the noise problem in the background for this application.

III. Current-Computing Network Relations

The behavior of various parts of a current-computing system is conveniently expressed in terms of 4-terminal network relationships. Once the basic operational amplifier has been designed and built, it becomes effectively a 4-terminal device (with a common through terminal) which is then placed in a network of passive computing components to perform a specific mathematical operation. The properties of the amplifier itself as a 4-terminal network are discussed in Appendix III. Basic network equations relating currents and voltages are given there. Since the form of the network in which the amplifier is placed is invariant, certain general relationships may be developed to predict unit behavior.

Figure 3-4(a) shows the current-computing operational unit, including precision passive elements and the basic computing amplifier. These elements may all be taken together, as shown in the larger dotted square, to form a consolidated idealized 4-terminal network which operates upon the circuit variables from the equivalent generator and delivers them to the equivalent load. The operations which this whole network performs, then, for linear operating regions of the amplifier, may be expressed in terms of the four new equivalent network parameters. The new network is shown in Figure 3-4 (b). The new parameters are designated by primed terms, and they are expressed in terms of the basic equivalent circuit parameters of Appendix III and of the two precision elements by means of new loop equations.

$$E_{1g} = I_1' Z_{11}' + I_2' Z_{12}' \quad * \qquad (3\text{-}1)$$

$$E_{2g} = I_1' Z_{21}' + I_2' Z_{22}' \qquad (3\text{-}2)$$

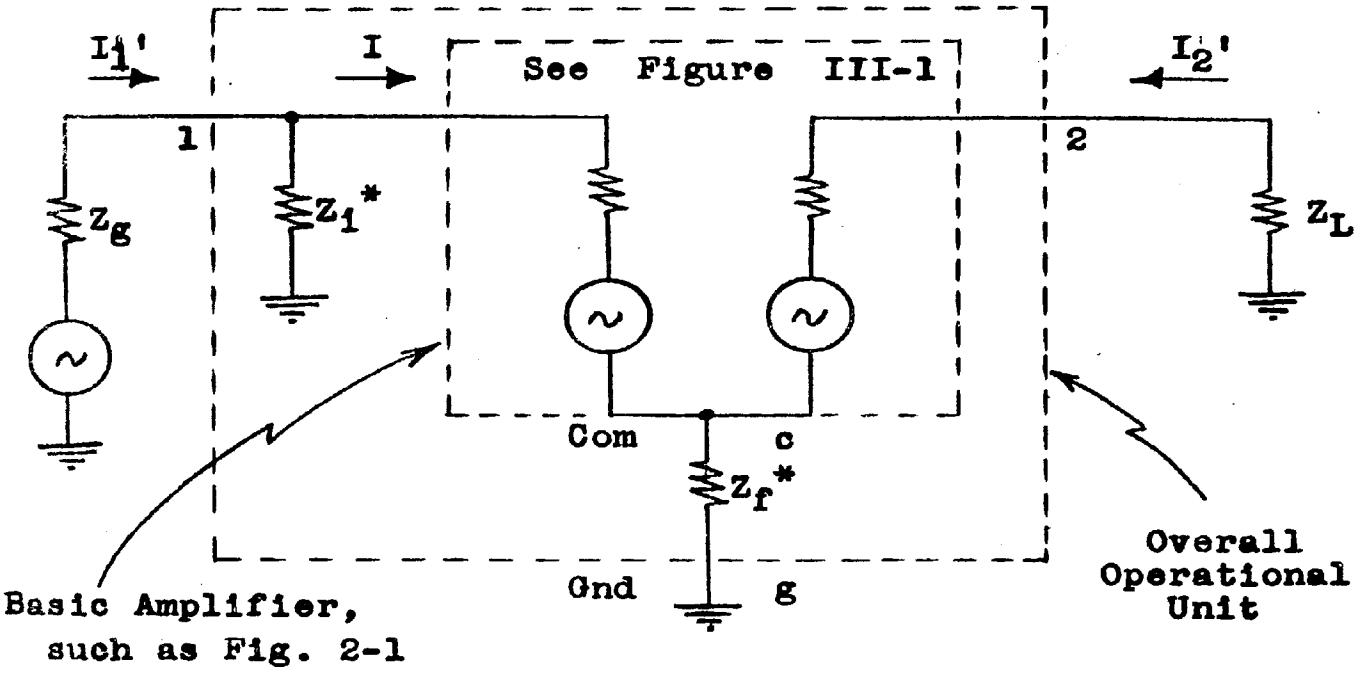
where:

$$Z_{11}' = \frac{Z_i (Z_f + Z_{11})}{Z_i + Z_f + Z_{11}} \qquad (3\text{-}3)$$

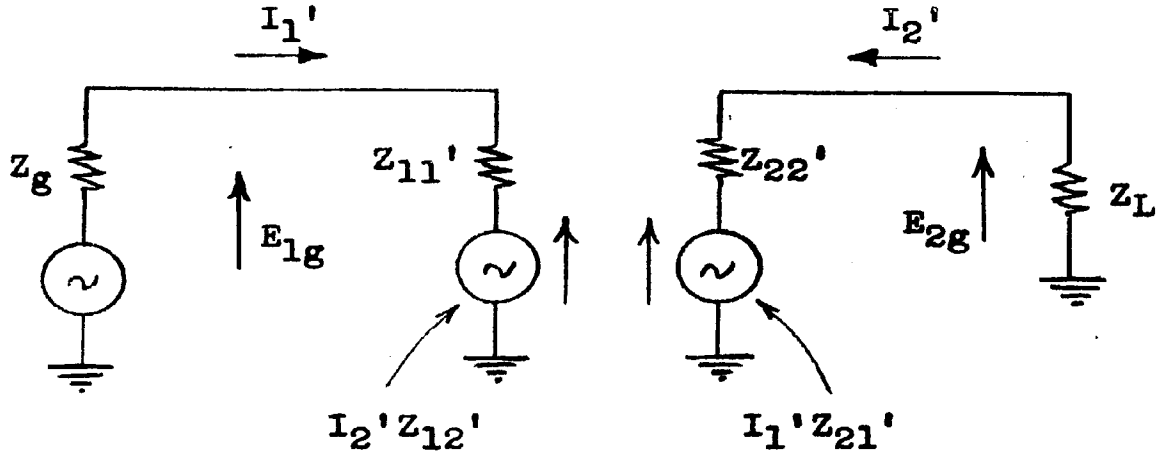
$$Z_{12}' = \frac{Z_i (Z_f + Z_{12})}{Z_i + Z_f + Z_{11}} \qquad (3\text{-}4)$$

* See Appendix I for list of symbols used.

CURRENT - COMPUTING OPERATIONAL NETWORK



a) Elements in the Computing Network



b) Simplified Equivalent Circuit

Figure 3-4

$$Z'_{21} = \frac{Z_i (Z_f + Z_{21})}{Z_i + Z_f + Z_{11}} \qquad (3-5)$$

$$Z'_{22} = Z_{22} + Z_f - \frac{(Z_f + Z_{12})(Z_f + Z_{21})}{Z_i + Z_f + Z_{11}} \qquad (3-6)$$

From these new 4-terminal network parameters may be calculated such overall properties of the system as:

(1) Forward gain or transfer, and hence the accuracy of analogue computing;

(2) Input and Output impedances, to determine loading upon the source and attenuation in driving a prescribed load;

(3) Stability of operation, from Equation (12) of Appendix III.

Computer terminology often refers to the small residual signal at the computing amplifier's input as the "error" signal. Thus in Figure 3-4(a) the error current is represented by plain I, which is used here as capital iota. The instantaneous current at this point, in the time domain, is given by lower case iota. The choice of this symbol for error current seems appropriate, because it is always a very small quantity.

Utilizing the formulae of Appendix III and based upon the one assumption that

$$Z_{12} \ll Z_f \ll Z_{21} \quad , \tag{3-7}$$

which is entirely justified for the circuits tested, (see Section IV of this chapter),

$$K_I' \simeq \frac{Z_i K_I}{Z_i + Z_{11} + Z_f (1 - K_I)} \simeq - \frac{I_2'}{I_1'} \tag{3-8}$$

This operation unit transfer function is used extensively in the Error Analysis and Stability portions of the dissertation.

It may also be shown that the new effective input impedance to the operational unit, at point "1" of Figure 3-4(a), is composed of the parallel combination of Z_i and

$$Z_{11} + Z_f - \frac{(Z_f + Z_{12})(Z_f + Z_{21})}{Z_f + Z_{22} + Z_L} \tag{3-9a}$$

without any assumptions. This shunting term, given by (3-9a) may be justly approximated by

$$Z_{11} + Z_f (1 - K_I) \tag{3-9b}$$

within the previous assumption of (3-7). Thus the current gain acts in an important way to raise the impedance which shunts Z_i.

The net effective input impedance, Z'_{in}, is closely given by

$$Z'_{in} \cong Z_i \quad . \tag{3-10}$$

The exact expression for output impedance of the operational unit depends upon Z_g, and it may be found from these formulae. By design, however, Z_g will be so much larger than Z_i that the generator may be considered to be an ideal current source. Then

$$Z'_{out} = Z_{22} + Z_f - \frac{(Z_f + Z_{12})(Z_f + Z_{21})}{Z_i + Z_f + Z_{11}}$$

$$= Z'_{22} \tag{3-11a}$$

For Z_i, Z_f, and Z_{11} of the same order,

and $Z_{12} \ll Z_f \ll Z_{21}$,

and $-K_I \gg 1$:

$$Z'_{out} \cong -\frac{K_I}{3}(Z_{22} + Z_f + Z_L), \tag{3-11b}$$

which is many times larger than the output impedance of the basic amplifier.

IV. Typical Values of Network Parameters

For the transistor amplifier of Figure 2-1 the following values were found for the parameters of the basic equivalent network, that is, for the amplifier alone without precision passive elements.

Fifteen type 2N34 transistor samples were used in the tests, in 7 combinations of 3, so that none was used in the same position in the amplifier twice. The averaged parameter values are given. They are measured for low frequencies only.

$R_{11} = 1870.\ \Omega \qquad R_{12} = -.337\ \Omega$

$R_{21} = -2.29\ M\Omega \qquad R_{22} = 1184.\ \Omega$

From these may be calculated

$$\alpha = -1920 \quad \text{and} \quad K_I = \frac{-2,290,000.}{1184 + R_L + R_f} .$$

This amplifier was used in the tests of current computing which produced the waveforms of Figures 2-4 through 2-7. Some circuit modifications of the phase control networks were made after these tests, and the resulting test circuit is shown in Figure 3-1. The DC equivalent-network properties, as expressed by the four impedance (resistance) parameters just given are

similar before and after the changes. These values are presented as typical of the orders of magnitude which have been found useful in design.

V. Stability

All circuit configurations which are used for accurate analogue computation and which involve active elements rely heavily upon degenerative feedback to produce mathematical operations which are sufficiently independent of amplifier imperfections. The higher the internal gain within the computing unit and, consequently, the more degeneration used, the greater this independence can be made (13, p. 527).

Large values of degenerative feedback, such as 60 decibels used here, mean that careful attention must be paid to the circuit control of amplifier gain and phase responses over the useful frequency spectrum and beyond (14). Transistors, with their present relatively narrow frequency range, require consideration of phase and gain response control at much lower frequencies than vacuum tubes. When higher-frequency transistors become available the effects will still be present but will be less important for a given analogue problem and timescale.

In order to use the maximum bandwidth available in whatever type amplifier is employed, the criteria of stable circuit operation must be determined. For example, the effects of stray reactances at the edge of the useful passband or beyond may cause regeneration and instability.

The transfer function of the computing unit is examined in terms of the Nyquist criteria to determine unit stability. The stability study presented here shows, in effect, methds of applying these criteria when we have certain specific pieces of known information.

The case of so-called conditional stability is to be avoided in good engineering design of computing units because such operation does not permit the safety margins which are required to assure absolute stability in all operating circuits. For this reason conditional stability will be avoided in practice and in analysis. Further, only the stability of single operational units is determined in this dissertation, although the method is of course applicable to several or many interconnected units.

The current computing unit transfer function is defined in Section III by Equation (3-8) and is:

$$K_I' \cong \frac{K_I}{1 + \frac{Z_{11}}{Z_i} + \frac{Z_f}{Z_i}(1 - K_I)} \qquad (3\text{-}12)$$

where

K_I' is the overall unit current gain,

K_I is the amplifier current gain,

Z_i is the summing element impedance,

Z_{11} is the input loop impedance of the amplifier,

Z_f is the feedback element impedance,

and all of these may be functions of the complex frequency variable "p". A direct parallel exists between this expression and a steady-state overall gain which may be expressed in terms of a loop gain. We shall identify the loop gain by the symbol $\underline{\Phi}(p)$, which Nyquist calls "AJ". For the computing amplifier with feedback, the net gain is given by:

$$K_I' \cong \frac{K_I(p)}{1 + \underline{\Phi}(p)} \qquad (3\text{-}13)$$

where

$$\underline{\Phi}(p) = \frac{Z_{11}}{Z_i} + \frac{Z_f}{Z_i}(1 - K_I) \qquad (3\text{-}14)$$

It is a simple matter to follow through Nyquist's method upon $\underline{\Phi}(p)$ to establish the relationships which are necessary

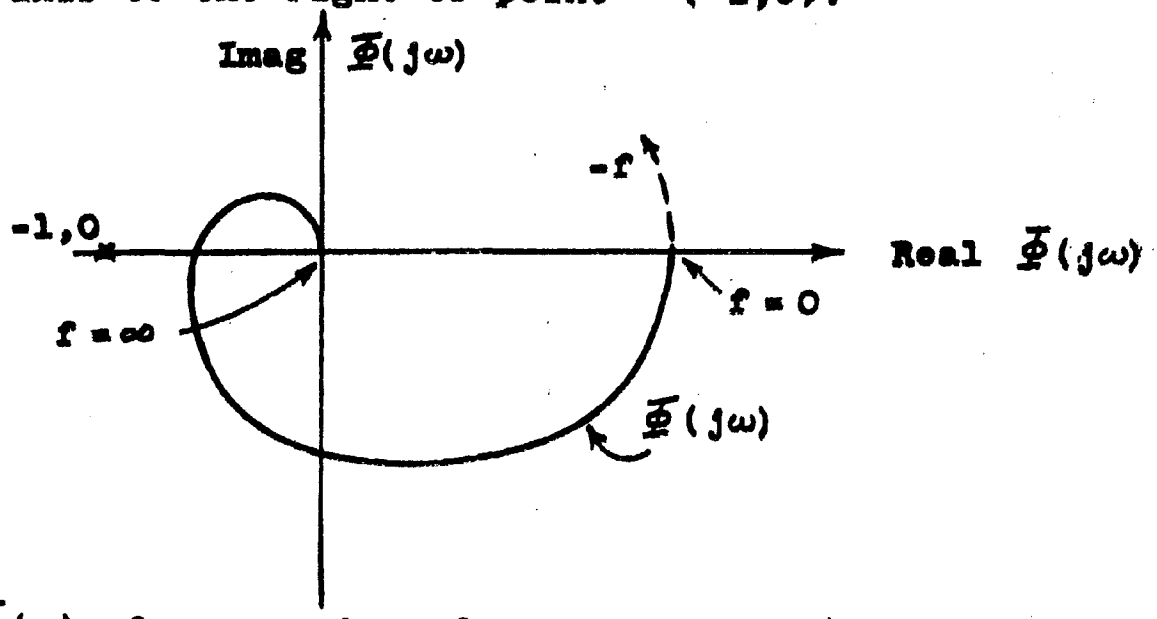
between Z_{11}, Z_i, Z_f, and K_I in order to assure stability.

The familiar Nyquist diagram is plotted in a complex plane, such as in Figure 3-5(a), for known values of these four parameters for real frequencies, here as $\bar{\Phi}(j\omega)$. If the point -1 + jO lies outside the (closed) plot for all frequencies, the computing unit is stable. Figure 3-5(b) shows typical plots expected for the unit operations of Isolation, Integration, and Differentiation.

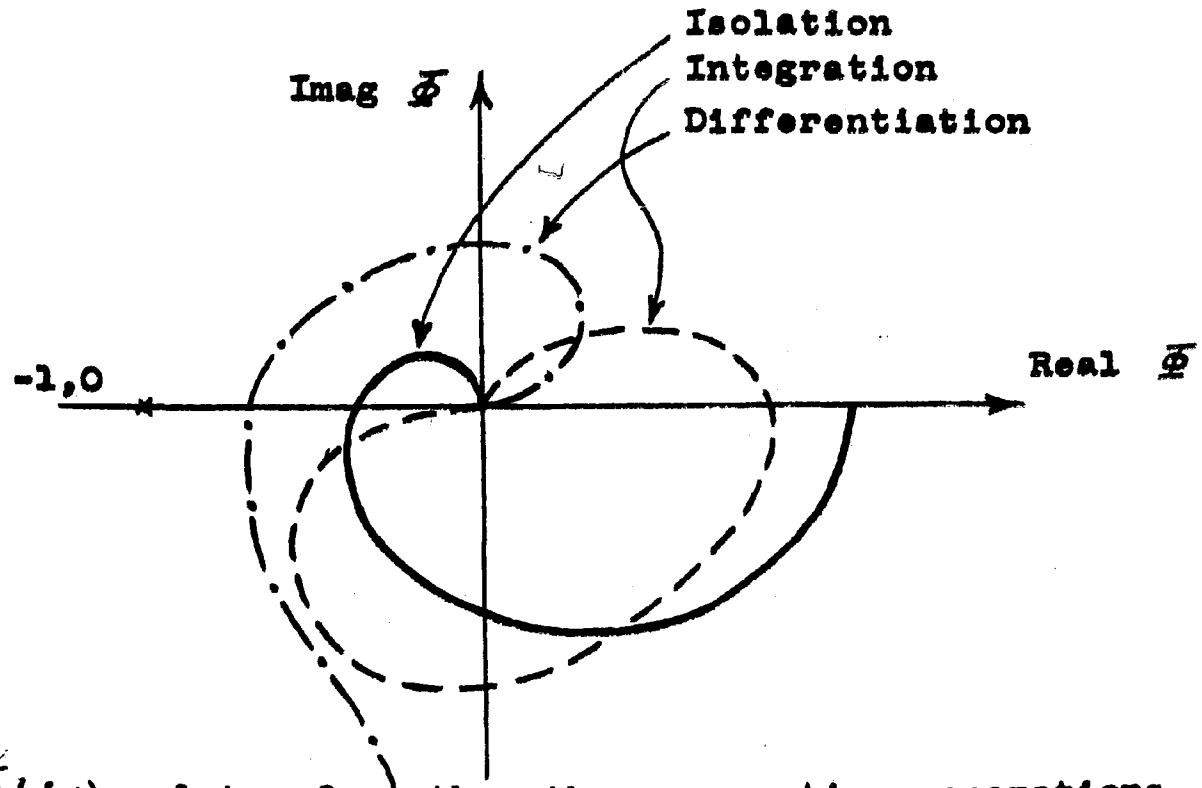
Each operation deserves a separate study to define the impedances and amplifier response necessary for stable operation. The Isolation operation, for example, usually uses resistive summing and feedback elements such as in Figure 2-4. If Z_{11} is considered also resistive, then the frequency dependence of $\bar{\Phi}(j\omega)$ is entirely due to that of $K_I(j\omega)$. When an analytic expression for $K_I(j\omega)$ can be found, possibly by curve-matching the measured amplifier response, as in Appendix IV, it may be substituted into $\bar{\Phi}(j\omega)$. The frequency at which $\bar{\Phi}(j\omega)$ is real and negative is found. There will be only one such positive frequency unless the amplifier contains more than six stages of the normal minimum-phase type, which is not likely. The test of whether $\bar{\Phi}(j\omega)$ at this frequency has a larger magnitude than unity tells

NYQUIST STABILITY CRITERION

These circuits are stable when $\bar{\Phi}(j\omega)$ crosses the real axis to the right of point (-1,0).



a) $\bar{\Phi}(p)$ for $p = j\omega$ forms the Nyquist plot



b) $\bar{\Phi}(j\omega)$ plots for the three computing operations

Figure 3-5

stability, where the unit is unstable if $\bar{\Phi}(j\omega)$ exceeds unity.

Similar tests are valuable for the other unit operations, where Z_i and/or Z_f are reactive, such as in Integration and Differentiation. Since $\bar{\Phi}$ for these operations depends on more than one frequency-dependent term, its plot on the complex plane will have one of the other forms shown in Figure 3-5(b). The frequency at which $\bar{\Phi}(j\omega)$ is real and negative, and the magnitude of $\bar{\Phi}$ at this frequency, again defines stability as for the case of Isolation.

If an analytic expression for $K_I(j\omega)$ is not readily available, the same results may be obtained graphically. The stability of the computing unit is tested point by point, where specific values of gain $K_I(j\omega)$ and phase are known. At each such frequency the values of all circuit impedances Z_i, Z_{11}, and Z_f, are calculated for the steady-state condition. All these values with their real and imaginary parts are substituted into Equation (3-14), and $\bar{\Phi}$ is found. A few points of the plot, such as Figure 3-5(a), are usually sufficient to sketch in the whole frequency contour. Stability is obtained when all real values of $\bar{\Phi}(j\omega)$ lie to the right of $(-1, 0)$, as before.

Either of the following reasons for applying the criteria may be involved:

(1) To choose Z_i and /or Z_f for a given amplifier's $K_I(j\omega)$ and its Z_{11}, or

(2) to determine the design criteria for $K_I(j\omega)$ of the current-computing amplifier in order to meet certain general conditions of anticipated use with a wide range of Z_i's and Z_f's.

The latter purpose was basic to the design work described in the dissertation. For example, it may be shown from Equation (3-14) that for each operation, when simple impedances are considered, there is a maximum phase shift which the computing amplifier can have and be sure to remain stable, for any frequency below that at which its gain has dropped to approximately unity. The following are the maximum safe amplifier phase shifts for stability which each operation allows:

(1) For Isolation, 180 degrees

(2) For Integration, 270 degrees

(3) For Differentiation, 90 degrees.

Stability is assured by the above limits but, conversely, instability is not assured by exceeding them. There are

impedance values which permit stable differentiation, for instance, with the amplifier of Figure 3-1, which has up to 150 degrees of phase shift before dropping below unity gain.

The amplifiers here were designed for the Isolation operation, as a demonstration of current computing, so that 180 degrees was their design limit of phase shift. The steps taken to control this shift are outlined in the following section of this chapter.

VI. Phase and Gain Control in the Computing Amplifier

With the stability criteria of Nyquist and Bode interpreted as in Section III, the design of amplifier frequency responses for current computing is specified. The amplitude and the phase responses versus frequency for the amplifier must be controlled so that the criteria are at least met within all anticipated operating conditions. Above this minimum design specification, however, suitable safety margins will be allowed as good engineering practice to take into account possible shifts and variations which cannot be included in the analytic design.

It has been determined that for stability in these demonstration circuits the amplifier phase shift (lag) shall not reach 180° as long as gain is greater than zero decibels. For safety, it will be further specified that phase angle shall not exceed even 150° (30° phase margin) in this frequency interval. Also for safety, the phase shift shall not reach 180° until gain has dropped to at least ten decibels below zero, thus providing a ten decibel gain margin. The degree to which these conditions have been met is shown in Figure 3-2.

Phase control for the DC amplifier is, of course, only necessary at higher frequencies where the transistor's low-frequency properties degenerate. Increasing frequency acts to reduce gain and introduce phase lag from the input to the output of each stage. The frequency behavior of individual common-emitter transistor stages is ably discussed in the literature(7. p. 194)(15).

By means of simple, shunting RC combinations additional frequency-dependent attenuation and phase lag are added to the basic response of the amplifier. It will be assumed that sufficient isolation is afforded by each transistor stage to

make the action of each control network independent of the other networks and of the basic amplifier response. This assumption, which is valid only to a first approximation, permits simply adding graphically the response curves of the inserted networks, and those of the amplifier, to obtain curves versus frequency of the net gain and phase responses.

Starting with the basic amplifier, without any control circuits present, its gain and phase characteristics were measured. The three-decibel break frequency for the circuit of Figure 3-1, without the stabilizing (reactive) networks, occurred at just 20 kilocycles. The low-frequency forward gain of 68 decibels (plus another ten decibels for gain margin) had to be killed below the frequency at which the net phase shift equals 180°. Care was exercised to insure that the added phase lag caused by the control networks never brought net overall phase shift to more than 150° at any frequency below that at which the forward gain has dropped from 68 to zero decibels.

From the amplifier schematic, such as Figure 3-1, it is noted that there are only three relatively isolated points

available at which networks may be added. These are:

(1) across the input to the first transistor

(2) between the first and second transistors

(3) between the second and third transistors.

Therefore, three control networks were to be selected which would provide the necessary gain and phase control, but which consume the minimum necessary amount of precious bandwidth.

Each control network consists of a resistor and capacitor in series. Each is shunted between the chosen point (or node) in the amplifier circuit and the common through-terminal. The behavior of each control network is briefly as follows.

At very low frequencies the capacitive reactance is very high and no shunting effect occurs. At frequencies at which phase control is desired the capacitive reactance is comparable in magnitude to the series resistance and/or the equivalent generator resistance of all the rest of the circuit. The current which is shunted to the common terminal (that is, to the amplifier ground) has a phase lead, compared to the voltage signal appearing across the network, of an amount depending upon resistance and reactance

magnitudes. The remaining current, which carries the signal on to the rest of the amplifier, lags the voltage at this point, and so the apparent phase shift (lag) of the whole amplifier has been increased at this frequency. At much higher frequencies the reactance of the shunting capacitor is so small in comparison to circuit resistances that it causes no appreciable phase shift in the overall amplifier. In summary, then, the network has caused a maximum phase shift at a particular frequency without changing phase shift at very low or very high frequencies. It has caused signal attenuation at high frequencies only.

In order to modify the basic responses of the amplifier, the effects of such RC networks were added one by one graphically to the basic amplifier curves. Test results of the overall properties of the stabilized computing amplifier are given in Figure 3-2.

The RC phase control network at the amplifier input terminal, shown in Figure 3-1, has a pronounced effect upon amplifier input loop impedance, Z_{11}, at the upper frequencies of the amplifier pass band. This input impedance drops at approximately six decibels per octave. For the calculations of

Appendix IV, Z_{11} has been assumed constant over the useful frequency range. Such an assumption should be carefully evaluated along with the frequency dependence of K_I in an appraisal of computing capabilities. A more thorough analysis might consider Z_{11} of the amplifier to be a compound network composed of the DC input resistance value shunted by the actual stabilizing network.

The transistor itself has been described as having such a compound intrinsic network at its input at very high frequencies[15]. The net higher-frequency effects, of which the changing transistor input impedance is a part, are responsible for the amplifier's phase shift and so for any ultimate circuit instability due to regeneration. This transistor impedance-change effect is far removed from the frequencies at which the control networks inserted here are made effective.

The value of careful design of the stabilizing networks shows up in preserving as much useful bandwidth as is possible, yet establishing this assurance of stability when feedback is applied. The conservation of bandwidth is especially important with present transistors, which have little enough bandwidth even

before stabilizing. This situation contrasts sharply with vacuum tubes which might provide an amplifier stabilized for this amount of feedback with still several more decades of upper-frequency usefulness remaining. The final bandwidth of the stabilized transistor amplifier shown in Figure 3-2 is adequate for many DC computing applications.

VII. Recommendations for Transistor Computing Amplifier Designs

Based upon the design experience to date, there are a number of pertinent recommendations which are appropriate for consideration in the future design of current-computing transistor amplifiers:

(1) The maximum output signal excursion of an amplifier is a function of the allowable dissipation in the output transistor stage. Until single transistors are available with sufficiently increased ratings, various combination stages can be used for higher outputs or for efficiency. Complimentary symmetry in the operation of cascaded and push-pull DC coupled stages offers great advantages[16]. This operation requires

PNP and NPN transistors of quite similar characteristics. If these latter are not available, other push-pull and/or parallel arrangements can utilize power transistors in class A or class B amplifier output stages[17].

(2) Transistor upper frequency limitations, notably of α_{cb}, restrict the available computer bandwidth to a serious degree. As higher current gain is required for greater system accuracy, Bode has shown that the stabilization of the amplifier for feedback will consume more bandwidth. If the same type transistor is used in a higher gain application the bandwidth left for manipulation of the computing variables would be much smaller than obtained in the work described here.

Higher-frequency transistors are to be desired and used wherever possible. In lieu of higher-frequency response, or for use in conjunction with it for maximum utilization of bandwidth, at least one other technique is available. Cohen, of the RCA Tube Department, has suggested that common-emitter stages with added emitter resistance yield disproportionately higher α_{cb} cutoff frequencies.

In spite of loss due to degeneration through this resistance, a net increase of bandwidth seems possible. This technique should be evaluated in new designs.

(3) The choice of amplifier loading impedance has here been predicated upon maximum signal and on the amplifier output impedance. Often loading impedance will be set by some transducer which must be actuated or driven. Where a choice of loading impedance is available, however, it should be arranged to be of the same order as the lowest amplifier input impedance which can be easily obtained. The desirability of low unit input impedance is shown in the chapter on Error Analysis. In general, the amplifier input impedance, the summing impedance, the feedback impedance, and the load impedance are all of comparable magnitudes at some middle frequency of interest.

(4) Higher current gain is synonymous with improved operational accuracy, as described in the Error Analysis chapter. It is desirable for this reason. High gain must be balanced against reduced bandwidth after stabilization, for given transistors, and against the allowable noise

limit, in any system and operational amplifier design.

(5) Temperature stabilization is an important facet of using transistors in DC amplifiers. Because leakage current increases greatly with temperature, the signal swing of a DC amplifier may soon be saturated by amplified leakage. Any desired signal would be swamped and entirely lost. A good treatment of this subject, with possible remedies, is given by Shea[7, p. 169] where both linear subtractive compensation and non-linear element compensation are employed. He reports considerable success in temperature-stabilizing two-stage transistor combinations. It will be well to consider these methods in any final amplifier design, especially when the computer is to be used outside the laboratory.

(6) An effective answer to DC drift and to some degree to temperature effects is accomplished by chopper stabilization[4]. Such techniques are particularly helpful in building a DC integrator. In normal integration any offset is treated by the unit as a constant input, so that when amplified it may swamp the signal-handling capabilities of the amplifier.

The circuit in Figure 3-6 has been designed to provide the amplifier of Figure 3-1 with chopped stabilization against drift or offset. The connections between amplifiers are shown in Figure 3-7. The chopper stabilization technique has been proven effective in reducing such difficulties in applications involving high-gain DC computing amplifiers.

The chopper amplifier of Figure 3-6 has been built with an application of temperature compensation in mind. The DC gain of the circuit in Figure 3-6 is 1200 at room temperature. Measurements have shown this gain to drop less than three decibels when the unit is operated in an elevated ambient temperature of 85 degrees Centigrade.

Thorough tests have not been made on the combination of amplifiers as shown in Figure 3-7 to ascertain the net temperature behavior. At room temperature the chopper amplifier did operate successfully to remove offset which the direct-coupled amplifier of Figure 3-1 had otherwise exhibited, for example, if not correctly balanced.

The chopper itself which will be used with this technique

CHOPPER D C TRANSISTOR AMPLIFIER

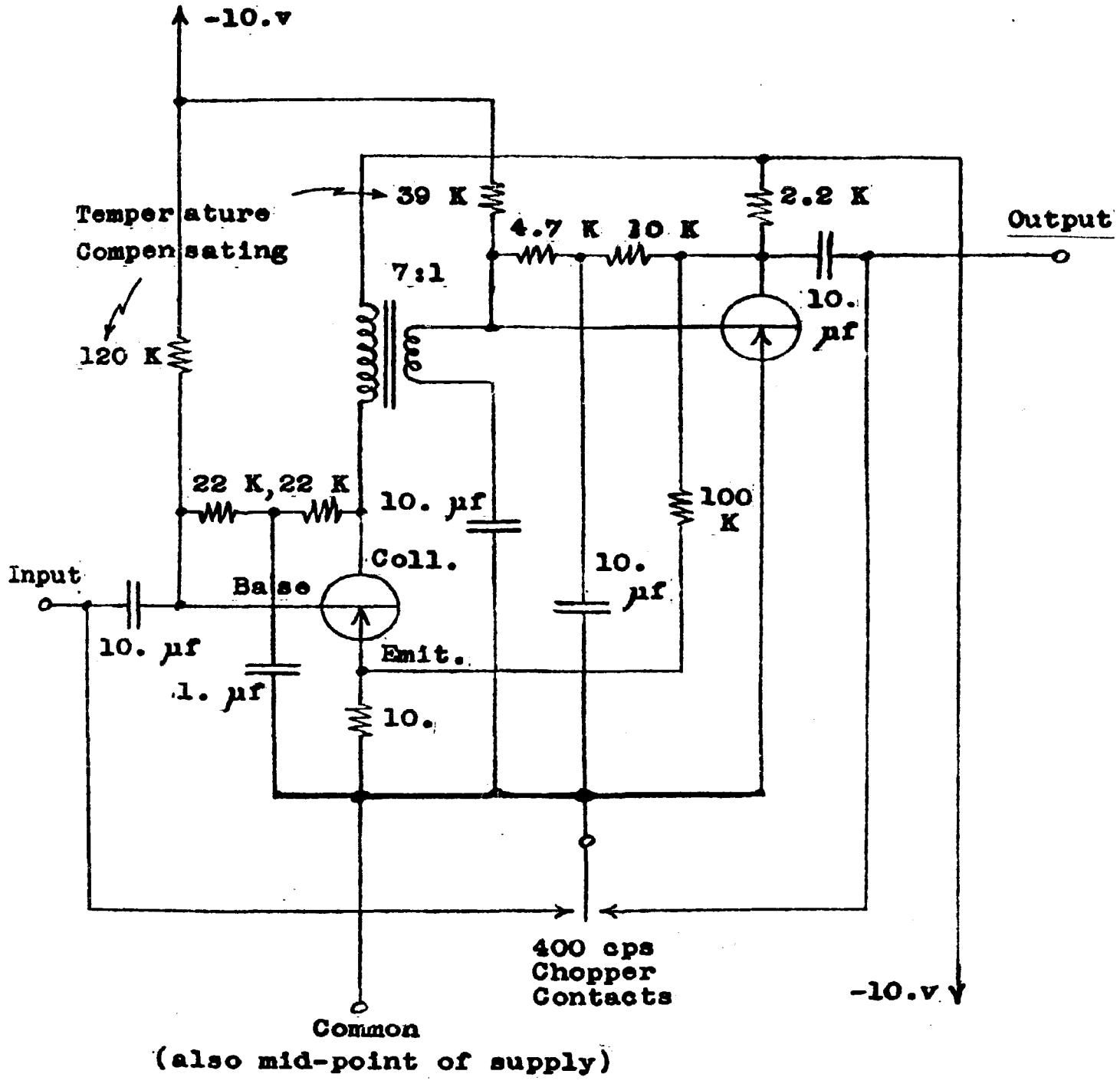


Figure 3-6

APPLICATION OF CHOPPER D C AMPLIFIER

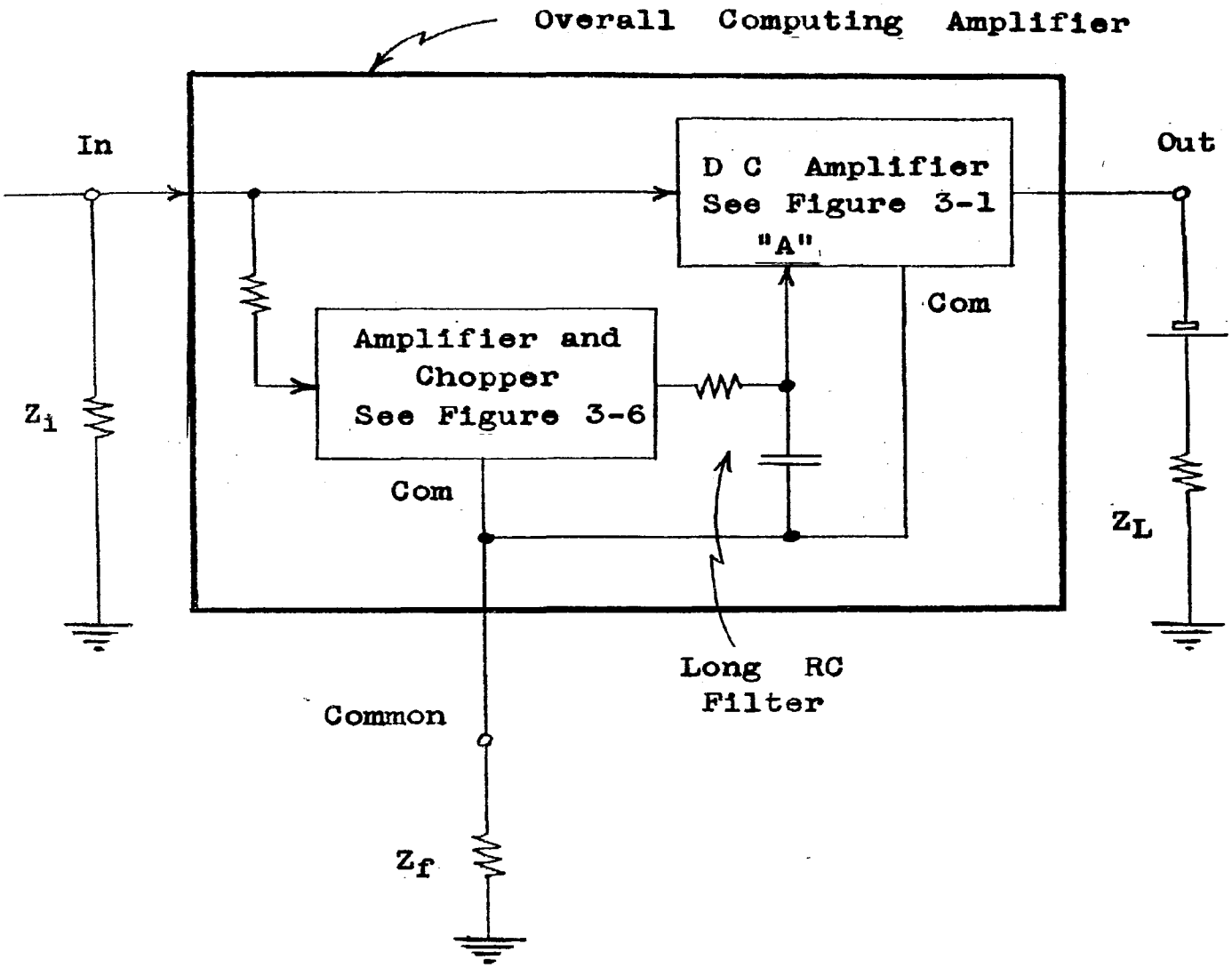


Figure 3-7

for current-computing can be much less critically designed than that which is used for voltage computing. In the latter system, if the armature in its travel is not touching either contact, then capacitance between stationary contacts forms a direct degenerative feedback path from AC amplifier output to input. To prevent this effect elaborately shielded choppers have always been used with high-gain amplifiers, or else a make-before-break chopper is necessary. For transistors the AC amplifier impedance levels are much lower, as is the gain of the AC amplifier illustrated here, so that capacitance between the contacts is most likely not sufficient to cause regeneration. Thus inexpenseive miniature choppers should be adequate for this application.

It is here recommended that the use of a supplementary chopper amplifier be given serious and early consideration in all anticipated applications of current analogue computing which depend upon transistors.

(7) From the circuit engineer's viewpoint there are several properties of transistors which seem more important than

others in the design and fabrication of the transistor itself. It is realized that great credit is already due the developers of present transistors, in the high rate of advance and level of the art today. It does seem, at the same time, that the prospective needs of one type of consumer should be expressed and made a matter of record.

Obviously the well-known technical limitations of the transistor should be overcome, as improved techniques become available. The following list states the author's rating of the priority for improvements:

(a) Reduce unit-to-unit variations, not stopping at vacuum tube standards.

(b) Reduce temperature sensitivity so that 10% or less change of each parameter is expected over the operating range.

(c) Provide essentially constant gains (current and voltage) as frequency goes up to one megacycle, or more.

(d) Make available matched PNP and NPN types.

(e) Reduce cost.

(f) Increase power handling to approximately one watt while preserving linearity for large signal swings.

It is also felt that very complete data could profitably be made available to the circuit engineer on each transistor type, to include such relations as how the equivalent circuit parameters vary with frequency, temperature, and biases.

CHAPTER FOUR

System Error Analysis

The purpose of this chapter is to propose in detail a method of expressing the accuracy with which any single operational unit, such as an integrator, handles the analogue variable. Mathematical examples of the proposed method are shown in Appendix IV. This chapter also serves to describe and explain the procedures used there.

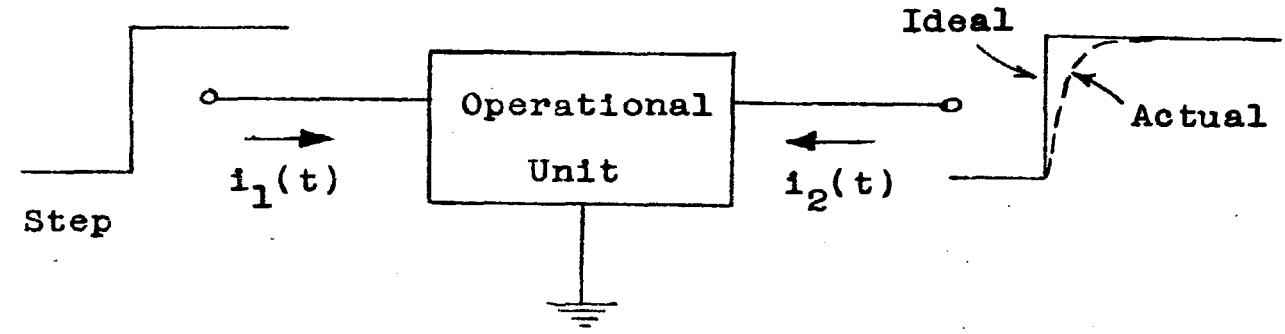
For the general analysis a specific waveform is chosen which permits practical qualitative interpretation of errors as well as being suitable for exact calculation of the error itself. It is felt that this technique can then be used by those people working with these units for either rapid appraisal, in which gross errors become obvious, or else for subtler examination of the computing unit, to evaluate its exact capabilities.

The criterion of accuracy which has been chosen is the faithfulness with which any unit can deliver a square wave of output signal (here current) for a simple input wave of appropriate

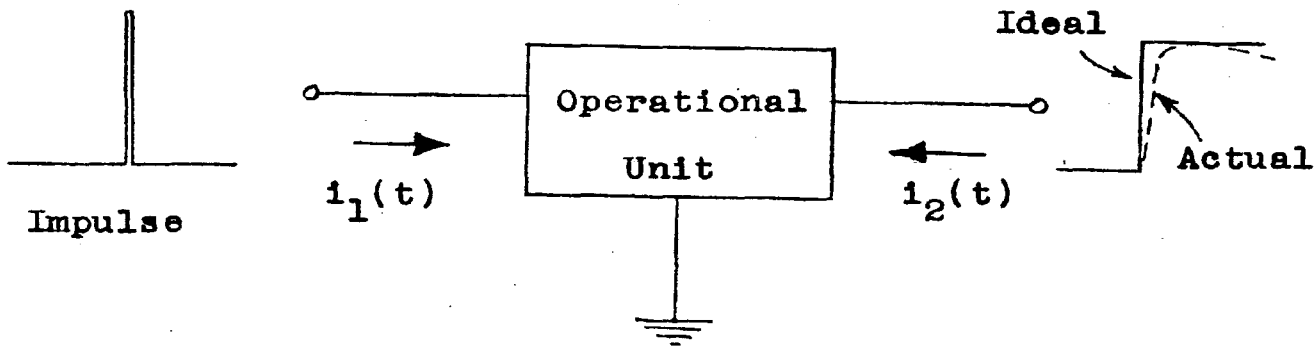
shape. The method will be illustrated only for the case of single operational units, although powerful results are expected if it were used for interconnected units, such as occur in the solution of a differential equation. For single units, the input signal to produce square-wave output varies with the type of operation involved. For example, a unit which performs the operation of integration must be supplied with an impulse waveform of known mathematical time integral for the desired output. The waveforms required for three basic operations are sketched in Figure 4-1.

The output from a real amplifier and associated precision components will not be an exact square wave. The dotted lines of Figure 4-1 show qualitatively the outputs expected. The difference, or error, from the perfect square wave may often be displayed visually on an oscilloscope for rough evaluation, or this error may be calculated more exactly from the known unit transfer function and other properties. This transfer function contains the effects of all first-order imperfections of the unit which are due to its being built necessarily of physically realizable components.

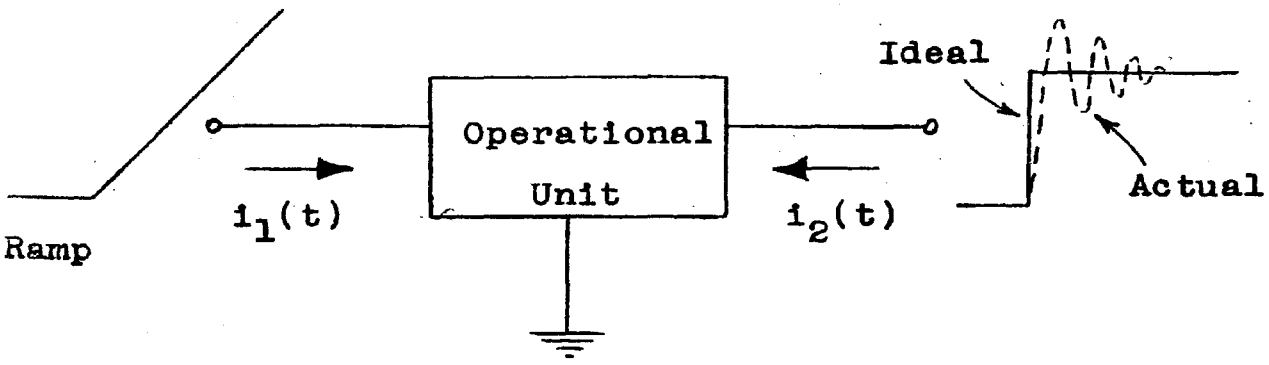
WAVEFORMS CONSIDERED IN ERROR ANALYSIS



a) Operation of Isolation



b) Integration



c) Differentiation

Figure 4-1

The error signal at the unit's output is thus, in the time domain, an instantaneous deviation from the ideal step. The error may be normalized or simply expressed in terms of Frational Error, FE, where a ratio is formed between the actual error amplitude and the ideally expected output amplitude. This FE is itself a function of time. It is shown for each operation in Figure IV-1 of Appendix IV. For practical operations the unit cannot be expected to follow the zero rise time of a mathematical step, although this type of waveform represents the "upper limit" of the response that will ever be expected of the unit in following a single transient. The fact that the unit does not perfectly follow this wave is never crucial in analogue operations performed on finite time scales. Some measure of its ability to handle such a signal, however, is to be found. The instantaneous FE is often not a fair test of unit accuracy in this case.

Much more to the point, it seems, is an evaluation of cumulative error over some specified time period, which can be made the computing interval. A simple, practical, and meaningful expression of cumulative error is obtained by finding the root-mean-square of the instantaneous fractional error. The

mean is taken over a period of time in which the unit's output will be observed or used. For the general evaluation and appraisal of a computing unit, a plot of this RMS FE versus time interval of averaging, such as shown in Figure 4-2, permits easy interpretation. For example, the intervals in which this computation can be performed to a specified accuracy are shown. The time interval, or period of averaging, as used here, is considered a parameter of the operation of the whole system, not as a variable. The result of the analogue computation may in practice be viewed continuously over the interval, rather than at just an instant of it, so that a cumulative description of error for the whole interval is needed. The length of the interval necessarily enters this description as a parameter. A single quantity, RMS FE, describes the composite error due to the computing operation.

In general the accuracy of the unit in handling more complex waveshapes can be interpreted directly from its ability to produce the square wave, and thus from its RMS FE shown here, depending on the waveform and time scale which are involved[18].

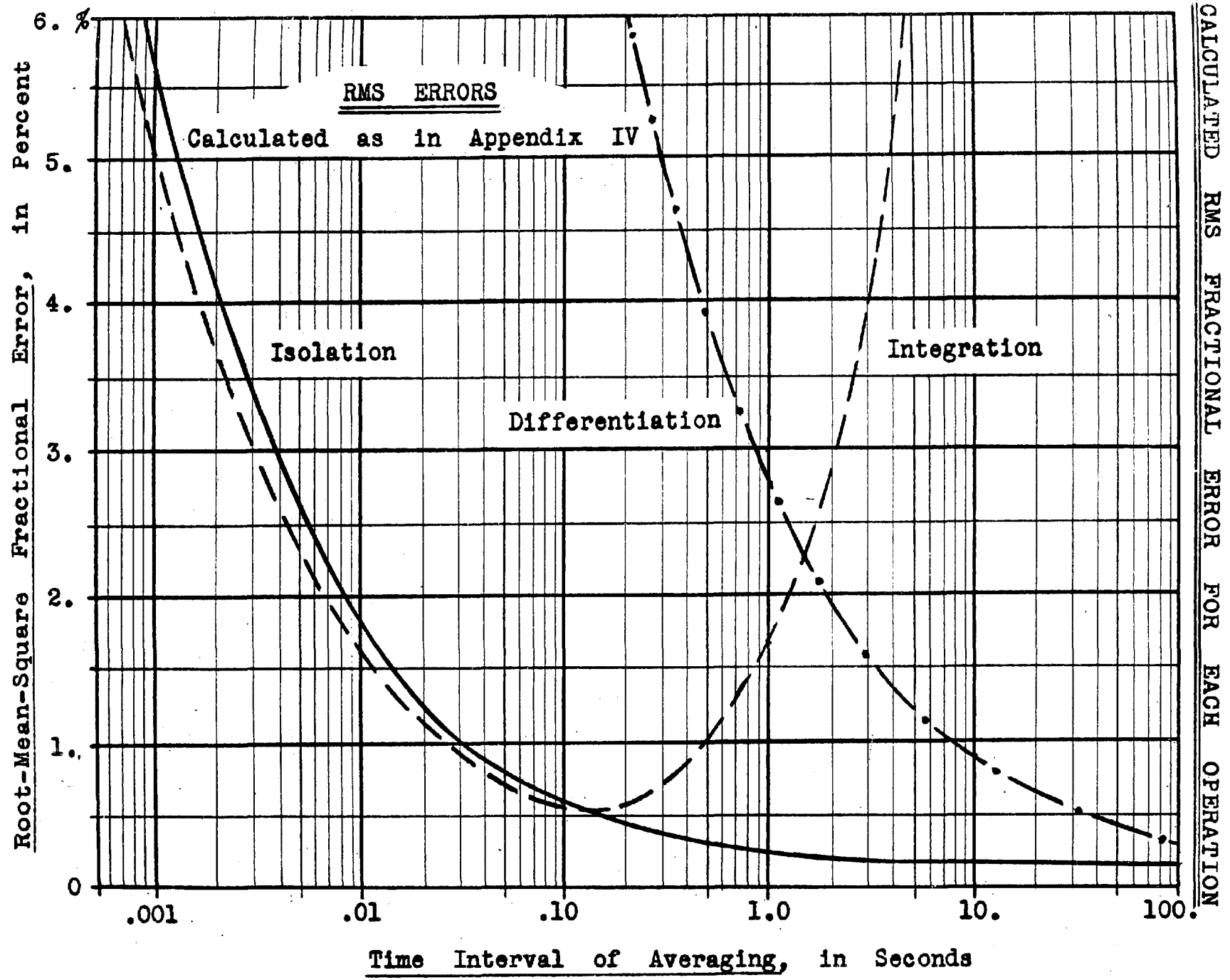


Figure 4-2 CALCULATED RMS FRACTIONAL ERROR FOR EACH OPERATION

In the design of an amplifier to fit a particular computing time scale, as, for example, in a fixed installation operating on real time, the RMS FE curve must be positioned along the time scale for suitable accuracy in the anticipated interval. This result can be achieved by preliminary calculations of RMS FE which involve such variables as computing impedances and required amplifier gain. The latter are changed and designed to yield a satisfactory RMS FE curve for the specific problem.

Three examples are given in Appendix IV of calculating the RMS FE curve for existing components. Typical curves are found for the operations of Isolation, Integration, and Differentiation, based on the parameters of one transistor current amplifier built for the current-computing system. These examples do not represent the highest obtainable state of the design art in their numerical values of accuracy, but they are rather pursued for illustration of the method.

For Appendix IV derivations, the first-order error sources have been considered to be: finite amplifier gain (less than infinite) and the presence of amplifier input resistance (greater than zero). These effects are introduced via the unit

transfer function defined in Section III of Chapter Three.

Some basic and reasonable assumptions have been made to provide useful results. The reactive elements in the units considered have been idealized to be purely reactive, and they are assumed to have no stored energy initially. The computing units themselves are loaded by essentially short circuits in comparison to their output impedances. Since the output impedances are shown to be quite high by Equation (3-11b) in Chapter Three, a useful range of real load impedances is permitted in practice.

The procedure followed in Appendix IV to find RMS FE is straightforward. Into the transfer function is inserted an expression for the variation of amplifier gain with complex frequency. The actual response of any multistage amplifier is complicated, especially after additional networks have been added to control gain and phase with frequency, as is the case here. The complicated response can be usefully and adequately approximated, however, by curve-matching with an analytic expression such as Equation (2) in Appendix IV. This expression itself is a reasonable and possibly conservative approximation

constructed from the amplifier's measured frequency response curve such as shown in Figure 3-2.

The choices of numerical values for the constants K_{I_o} and ω_o, for the example given there, are largely at the discretion of the design engineer. These two values determine how the experimentally-derived gain curve of Figure 3-2 is matched by Equation (2) in Appendix IV. In the design of a particular system, however, the choice of these two values, which are involved in the accuracy calculations and weigh heavily upon the numerical results of these calculations, should be based on some insight about the application of the computer. For example, where computer solutions will contain predominately fast transients and high-frequency components, and where it is essential that full predicted accuracy be available for these components, then ω_o, expressed as frequency, must be located well to the left of Figure 3-2. In this way the gain, K_I, of the actual amplifier will in fact be comparable to or somewhat higher than, in all frequency ranges of special interest, the value of gain assumed for calculating accuracy. The calculated error itself will be somewhat higher than actually occurs and the predicted accuracy will thus be conservative, although

realistic, for such an application.

This conservative appraisal of error may, on the other hand, be overly pessimistic for low-frequency signals. For constants chosen on the above basis, the assumed curve would be much below actual gain response in an important range of frequencies, so that calculated error would be unfairly high. The curve-matching constants should be differently selected for this second application.

Engineering judgment is an essential ingredient in applying these error analysis techniques to best advantage in individual applications. Once the transfer and the amplifier response characteristics of any particular operational unit have been established, their effects upon the signals can be resolved.

A suitable input signal form, of infinite bandwidth, and which would ideally yield the square wave of output signal is assumed and inserted (in transform form). The actual output in the time domain is derived from the preceding ingredients, and this signal is compared to an ideal square wave of comparable scale factor. RMS FE is found from the instantaneous error in the manner described previously. In general, the process is

somewhat simplified for a specific case by introducing known numerical values early in the analysis.

A point-by-point calculation of RMS error for various time intervals provides information for the error plot such as in Figure 4-2.

The other unit imperfections and sources of errors are usually secondary in comparison to the effects which have been incorporated in the numerical examples of Appendix IV. Errors which are due to imperfections of the precision computing impedances, such as the finite Q of realizable reactive elements, may be evaluated by direct substitution of actual values into the derivation of the error expressions. For example $R_i + pL_i$ might be used for Z_i in the differentiation operation described in Section IV of Appendix IV. Such a change considerably complicates the task of finding the inverse transform and of solving for error, but it might be warranted in some solutions.

Throughout these analyses the amplifiers have been assumed to be operated in their regions of linear transfer. Loop feedback acts to reduce distortion greatly, but care is necessary, as with any analogue computer installation, that the amplifiers

are not driven to saturation or signal-clipping levels. As expected, greatly increased errors are generated when the amplifier is operated beyond its linear range.

It is worth noting here that offset and drift in a DC amplifier may be considered as forms of "noise" introduced by the amplifier into the passband of computation. These unwanted DC signals, like noise, lower the system's dynamic range.

The frequency spectrum of noise has different effects upon different computing operations. For example, differentiation accentuates the high-frequency components of any signal. If the incoming signal contains a large quantity of higher-frequency components, such as sharp transients, they will contribute heavily toward the net RMS output of that operation. Similarly, such transients generated within noisy transistors may enter and be similarly emphasized by the operational unit.

Since the integration process effectively filters and accentuates the lower-frequency components of an input signal, DC offset and drift from the amplifier or from outside sources have important effects upon the accuracy of integration.

The integral of a constant offset is an error signal of growing magnitude with time.

Both transistor noise and DC drift act to restrict the minimum discernible signal which can be used for computing. They form one limit of the usable dynamic range, and their individual effects upon accuracy can usually be estimated.

Noise is treated as a supplement to the ideal input signal by referring its magnitude to the input point. Offset would be handled for the analysis here by assigning initial conditions and stored energies to the resistive and reactive components in the transfer function. Drift of a known magnitude should be referred to the input and treated as a slowly varying quantity added to input signal.

While the numerical values calculated in Appendix IV have not included all these error sources, it is felt that the more urgent ones are considered. The qualitative picture which Appendix IV gives of this particular method of error analysis illustrates just how it is applied to practical circuits.

CHAPTER FIVE

Conclusions

1. Specific Results

(1) Present transistors have been demonstrated in DC analogue computing circuits. By using the techniques of current computing, the low impedance and current-gain properties of transistors can be incorporated into useful operational units.

(2) As transistors themselves improve, the usefulness of current computing should increase. Present transistors have some limitations, such as useful bandwidth and dissipation, which form frontiers for any analogue applications. Each limitation is a matter of degree, rather than being absolute, so that it is expected that each will be eventually improved.

(3) It has been shown that the requirements of the current-computing system in order to obtain high computing accuracy, may be specified in practical terms. Other

properties, such as impedance levels and stability, have been investigated, and criteria are suggested for overall performance.

(4) Qualitative tests show that current computing satisfactorily performs the analogue operations of Isolation, Summing, Scale-Factor Change, Integration, and Differentiation. Combinations of these operations alone are adequate for the solution of analogue problems and of many types of differential equations.

(5) The method of determining the RMS accuracy of current-computing performance over some interval has been examined in detail and tried on a sample basis for all the important operations. The choice of components and scale factors for optimum accuracy is a straightforward procedure when based on the analytic methods which have been developed here.

(6) Subminiature operational amplifiers have been built and packaged in two forms, one for printed-circuit, dip-soldering techniques, and the other for encapsulation in protective resin. These have been constructed to follow a modular form.

(7) This study has indicated that point-contact transistors are unsatisfactory for use in voltage-analogue computing. Attempts to build linear amplifiers with the required high input impedance were not successful. Various transistor circuit combinations and feedback methods were investigated, but instability and unit-to-unit variations precluded useful input impedance above a few thousand ohms. Junction transistors are only somewhat better for voltage-analogue computing.

II. Discussion

Some emphasis is warranted on the engineering judgment which will be required in evaluating current computing for a specific application. This dissertation outlines what is believed to be a thorough and an effective method of determining the ability of given physical elements to perform analogue computations. One principal conclusion of this study is that the method is worthwhile. Its application, however, for particular components and hardware, lies in the hands of the design engineer. The author cannot state that the circuits presented here are the optimum in design for use in a fire-control radar computer, for example. The circuits here do illustrate, though,

the important parameters and the method of evaluating a proposed specific design. Each design must be evaluated in terms of the demands of one application.

For this reason, some of the necessary decisions, such as the degree of conservatism or pessimism in, for example, curve-matching the measured amplifier response as in Appendix IV, have significant effects on the numerical results. These effects, in turn, determine whether the results are acceptable for one application. Such a decision, and the one or two others required in predicting accuracy as listed on the following pages, mean that the ultimate design engineer retains his prerogative of using responsible engineering judgment. Now, however, he may be aided by a specialized tool.

Figure 4-2 summarizes the method of error analysis used in the dissertation. It plots the cumulative error, RMS FE, which will occur in the output of each computing operation. For the three different operations this RMS FE varies with the interval over which the answer is measured. Often the interval used will be the period of observation of the computing result. In that case an interval may be read directly from Figure 4-2 which

provides a predetermined maximum RMS FE for a test step output waveform. For the isolation and differentiation operations shown here the interval of averaging would be made larger than that which yields maximum allowed error. For integration some interval where RMS FE is below the specified maximum must be chosen, and the choice of intervals is narrower than for the other two operations.

For the design of new equipment or for the use of existing equipment the above steps are taken. Based on a test signal of the form necessary to yield a step function output the errors are found for various intervals of averaging. That interval of sufficiently accurate computation is identified and used.

For new equipment the designer has at his disposal a great many of the system variables, such as the quantites used in Appendix IV. He modifies and chooses these and his time scales so that operation takes place within the desirable range of a plot similar to Figure 4-2. The experimenter using existing equipment must, in a like manner, alter the variables at his disposal to reach the needed accuracy given by a curve such as in Figure 4-2. In the latter case the main parameter to bring this condition about will be his choice of time scale, and so of computing interval.

The decisions which an engineer must make in applying the accuracy predicting technique are:

(1) Choice of representation of the amplifier's characteristics by an analytic expression, as was done in Appendix IV, Equation (2). This choice need not be seriously pessimistic in order to result in the best engineered design. Rather it should be realistic, while perhaps somewhat conservative, in order to use given equipment to its utmost capabilities. If this choice were always made on a pessimistic basis, for conservatism, a more realistic design could later be found which would easily outperform the conservative unit.

On the other hand, the design engineer must know his equipment, and so be able to state that the predicted accuracy will be slightly better than he really needs for the majority of his applications.

(2) The major frequency components of the signals to be handled. A number of design economies, such as in balancing the relative importance of gain versus bandwidth, are possible if the signals are carefully analyzed beforehand.

(3) The terms which are inserted into the transfer function, as in Appendix IV. In some thorough analyses, for example, the change of amplifier input loop impedance with frequency must be considered. Since this move greatly complicates the solution for RMS FE, it should only be done if necessary. There are other quantities which might be elaborated to give more elegant predictions of error, such as exact generator and load-impedance effects.

In conclusion, a realistic appraisal of existing transistors indicates that for use in a current-computing system they presently have decided limitations. These include unit-to-unit variations, poor frequency response, temperature dependence, and low power capabilities. Transistors in this system thus could be used in rather undemanding applications where only moderate accuracies are needed.

The promises of improved transistors seem to offer bright hope for future potentialities.

The error analysis procedure seems on firm foundation, however, and its methods are applicable in different forms to defining a predicted error for analogue computing in general and for similar transfer operations.

APPENDIX I

List of Symbols

See references 13, 19, 20.

I. Major Quantities

A, B, D, E, F, G, H, M, N, R, T_1	Letters used in the derivations of Appendix IV to simplify the mathematics; defined there.
I_o	DC signal amplitude used for error analysis in Appendix IV.
K_{I_o}	DC gain for current signals.
α	Current gain with short-circuit load.
α_{cb}	Transistor current gain from base to collector.
e_n and $e_n(t)$	Instantaneous voltage signal
i_n and $i_n(t)$	Instantaneous current signal
E_n and $E_n(p)$	Laplace transform of $e_n(t)$

I_n and $I_n(p)$	Laplace transform of $i_n(t)$ where "n" denotes circuit location.
j	$\sqrt{-1}$
p	Complex frequency variable and operational symbol.
t	Time as a continuous variable.
T	Time interval over which an operation takes place.
ω	2π times frequency.
Ω	Ohms.
FE(t)	Fractional Error (instantaneous)
RMS FE	Root-mean-square of FE(t) over a specified interval.
K_m	Gain, as a ratio, where "m" denotes the quantities entering the ratio.



K	Kilohms.
R_{11}, R_{12}, R_{21}, R_{22} (Z_{11}, Z_{12}, Z_{21}, Z_{22})	Four-terminal network equivalent lumped resistance (or impedance) parameters.
R_n, (Z_n)	Resistance (impedance) of a circuit element or of an equivalent circuit element, where "n" signifies circuit location.
$\overline{\phi}$	Loop gain.
$\equiv$	Is defined as.

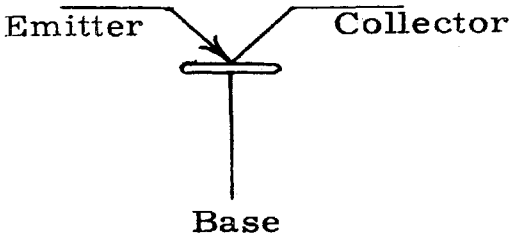
II. Subscripts

g	Of an equivalent generator
i	Used as summing element
f	Used as feedback element
L	Of an equivalent load
in	Equivalent input property
out	Equivalent output property
oc	For an open-circuit condition

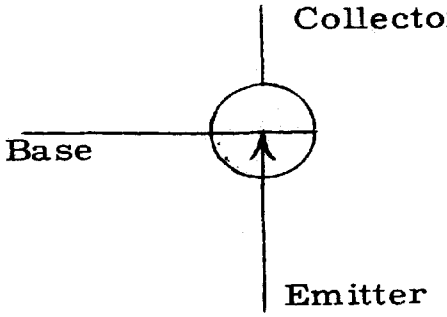
sc	For a short-circuit condition
I	Property involving currents
P	Property involving powers
R	Property involving resistances
V	Property involving voltages

III. Transistor Diagrams

Point-Contact Types



Diffused-Junction Types



Other symbols which have local applications in the text are defined or explained when used.

APPENDIX II

Early Transistor Tests

In order to emphasize the need for the current-computing system and to provide a background picture of the early work done here, a brief outline is presented in this Appendix of important preliminary attempts to use transistors in analogue computing.

Beginning in 1951 with the availability of early point-contact transistor samples, a number of theoretical and experiment approaches were tried in the hope of applying these units in the design of an operational amplifier for computing along the normal voltage-analogue principles. Although point-contact transistors proved entirely unsatisfactory for this application, a number of interesting circuits were developed in the course of the investigation. The main problem was that of obtaining the high amplifier input impedance which is desirable for voltage-analogue systems. Point-contact units, in general, exhibited poor stability when feedback and other means were used to raise the input terminal impedance of each stage or combination of

stages.

Since even moderately high impedance could not be obtained reliably in actual tests, and similar results had been indicated for junction transistors by other RCA groups, it seemed that no anticipated transistor could be expected to duplicate the relatively infinite low-frequency input impedance of the vacuum tube. It was, therefore, necessary to reappraise analogue computing in terms of the basic roles of passive and active component units, which together perform elementary computing operations. This reappraisal resulted, in January, 1953, in the current-computing system which has been discussed and which seems to utilize advantageously the same transistor properties which are drawbacks in use for voltage-analogue computing.

I. Point-contact Transistors as Linear Amplifiers

(1) Tests were made on all available samples of experimental and early commercial point-contact units. Both RCA type TA-165 and General Electric type G11 transistors were used. One primary interest was the

unit-to-unit variation between samples. The spread between samples was shown to be very large. Percentage-wise and for practical uses the wide distribution at low values of collector current was especially troublesome.

(2) The distributions of values for the important equivalent circuit parameters were measured, and they indicated again that considerable dispersion should be expected in these early units.

(3) For analytic studies of linearity it was desirable to express the average measured transistor output characteristics as functions relating the three independent current and voltage variables. An analytic expression was found by curve-matching. This form for the characteristics emphasized the departures from linearity to be expected in the transfer of signal variables through a stage which uses the transistor in any of its circuit connections.

(4) Several common-base stages were tested in cascade to form a simple AC amplifier. In spite of the

recognized poor impedance match from the output of one stage to the input of the next, no transformers were used, because it was hoped that this AC amplifier could later be revised for DC response by direct coupling between stages. Even though the AC amplifier provided useful signal gain, due solely to the current gain of each stage, it was not useful. The very low input impedance of common-base point-contact transistor stages could not be used in voltage analogue computing systems because of extreme attenuation. The common-base connection was the only one found stable, as tested, for point-contact units.

(5) Attempts were made to utilize the base-input connections with point-contact transistors[21]. The common-emitter connection looked especially promising in overcoming impedance mismatch difficulties when either cascaded in like stages or alternately with common-base stages.

Experimental results with seven point-contact samples

were as follows. Only positive input resistances were found, which is contrary to predictions based on the measured average equivalent circuit parameters and network relations. Both positive and negative output resistance values were measured, but they were not of the expected values due to the variation of each transistor from its published data. The most important and sought-for effect of all, that of input resistance higher than obtainable with common-base stages, was noted to only a slight degree. Input resistances of more than a few thousand ohms could not be obtained.

In summary, the common-emitter, or base-input, connection for point-contact transistors seems to offer some improvement in raising input impedance for computing and for better impedance matching between stages. The price seems to be, however, an accentuation of unit-to-unit transistor variations due to positive feedback.

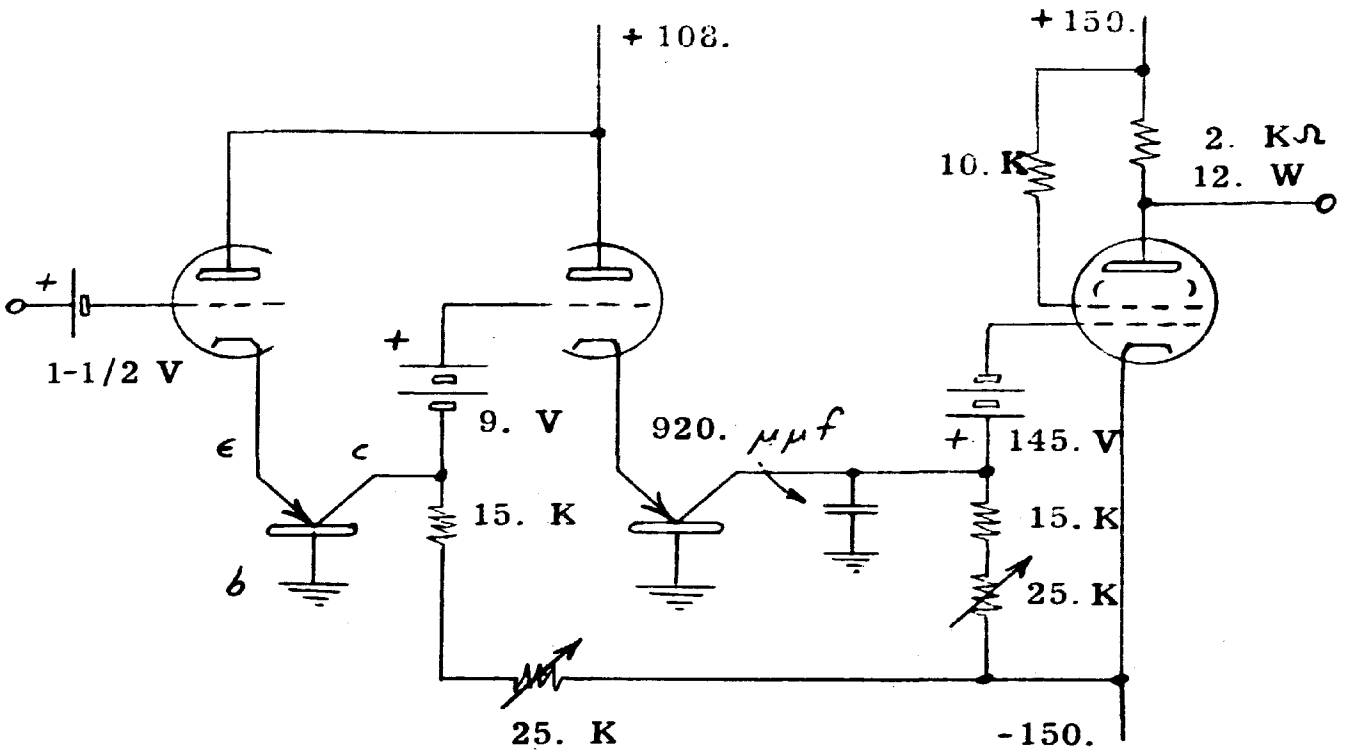
(6) As a concession in a weak moment to the earlier art,

a higher-gain DC amplifier was designed which combined transistors and vacuum tubes. This circuit was reasonably successful in that a low-frequency open-loop gain of 4500 was obtained with a vacuum tube providing high input impedance and a beam-power tube giving large output signal in comparison to transistors alone. As shown in Figure II-1(a), two triode cathode-follower stages were alternated with two common-base point-contact transistor stages. The feedback loop for voltage analogue computing was closed as illustrated in Figure II-1(b) without additional phase-control networks. The resulting operational amplifier exhibited good stability. Open-loop voltage gain was down six decibels at just below 50 kc.

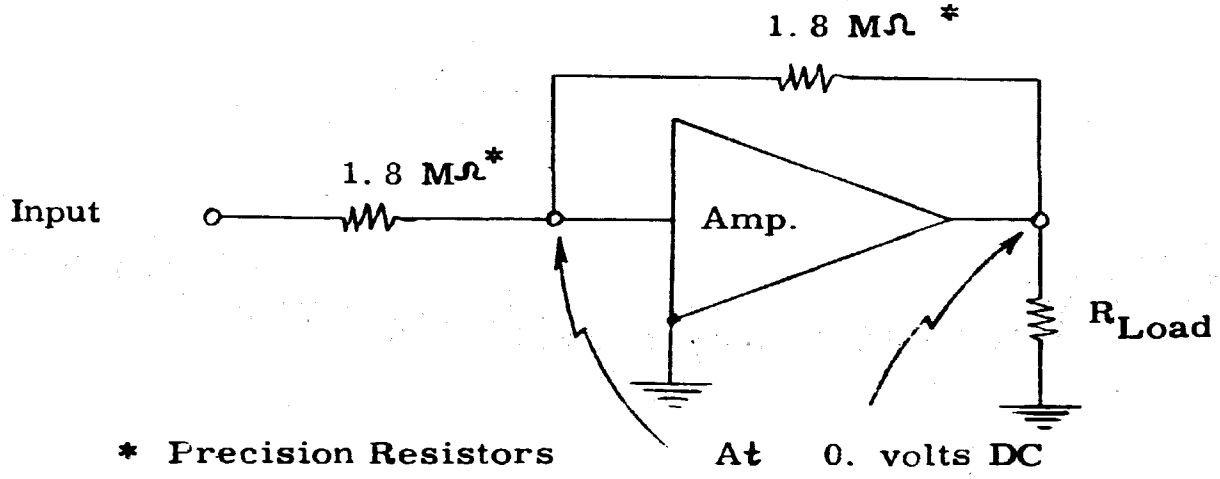
It was felt that the combining of transistors and vacuum tubes in one amplifier resulted in no new advantages, and that it retained the limitations of both devices.

(7) Several feedback methods were evolved from the four-terminal network relations applicable to a

TRANSISTOR - VACUUM TUBE DC AMPLIFIER



(a) Amplifier Schematic Diagram



(b) Amplifier in Closed Feedback Loop

Figure II-1

transistor (see Appendix III). These methods promised higher input resistance and lower output resistance than obtainable from the transistor alone.

One method applied input signal between emitter and base, and then connected load between collector and an intermediate point between input terminals. Input resistance was indeed raised, but at the expense of stability and the loss of a common input and output terminal.

Another method of feedback used two transistors effectively with their inputs in series and their outputs in parallel. The same results were obtained, along with an extreme difficulty of adjusting each transistor's operating point satisfactorily because of direct coupling throughout.

In summary of all the tests made upon point-contact transistors, it is felt that they are not suitable for direct-coupled use in linear amplifiers. It is not expected that point-contact transistors will be modified or improved to make them much better than they are now for this application. Their

attractive high-frequency response and early availability are more than offset by circuit drawbacks as discussed here. While the input resistance of a stage (containing one or more transistors) could be raised to a few thousand ohms, the power gain per stage and stability generally suffered significantly. Unit-to-unit variations made the design of cascaded, direct-coupled stages impractical for applications which require high amplifier gains.

II. Some Possible Methods of Using Transistors in Voltage-Analogue Computing

The complete lack of success encountered in building an operational amplifier of the conventional type with point-contact transistors has made necessary a reappraisal of computing fundamentals. A system had to be found which permits and works with low amplifier input resistance. It will be noted that the functional purpose of the operational amplifier is essentially to provide a power gain of significant magnitude.

(1) The first possible revision of conventional analogue techniques to be considered, to allow using transistor amplifiers, is based upon altering all the system impedances downward by a fixed proportion. For

example, the input resistance of a vacuum tube amplifier may be 100 Mohms. The input resistance of an amplifier using junction transistors may be reliably made of the order of 100 Kohms. Suppose, then, that all impedances used as passive computing elements are reduced by the factor 1000.

In spite of scaling down all impedances, the power gain requirements of the operational amplifier remain the same. For a typical load resistance of 10 Kohms for vacuum tubes, the power gain might typically be above 10^{13}, or over 130 decibels. Cascaded transistors could conceivably develop this high gain with perhaps five or six stages of 2N34 transistors. The scaled-down load resistance for use with transistors would be 10 ohms.

The difficulties to be expected with five or six stages, which are connected as described above, made this arrangement seem impractical. For example, carefully isolated power supplies are needed for these stages to prevent interaction between high-level and

low-level stages. The frequency-control networks required for five or six stages, in order to prevent regeneration in any or all conditions of feedback, cause great loss of useful pass band. Phase control must begin at a very low frequency, with concurrent attenuation, in order to maintain phase and to lower amplifier gain to unity before the cumulative phase shift reaches 180 degrees, as discussed in Chapter Three. The noise and drift levels of present transistors preclude such a magnitude of gain for any bandwidth.

For reduced magnitudes of power gain it seems that a workable transistor voltage-analogue computing system might be developed on the basis of reducing component impedance magnitudes throughout. It would also require, though, the redesign of associated precision equipment and expensive transducers and source and loading elements, such as precision potentiometers, in order to provide their resistance magnitudes within a compatible range. High-current, low-voltage power supplies would be needed.

(2) Analogue computing by conventional voltage techniques may be built around amplifiers which have low input impedances, for many applications, without scaling down all associated impedances. Transistor voltage amplifiers, where input impedance can be reliably made of the order of 100 Kohms by using junction transistors, would be entirely practical for these particular uses.

For Isolation, Summing, Integration and Differentiation, as shown in Figures 1-1(a), 1-2(a), 1-3(a), and 1-4(a), the input impedance of the operational amplifier acts like another input summing resistor whose generator is grounded. This resistance to ground lowers the amount of the effective forward, open-loop voltage gain of the operational amplifier as compared to an amplifier of infinite input resistance. That does not mean, however, that sufficiently accurate computation cannot be obtained in the processes listed above. The known finite input resistance must be considered and allowed for in designing the operational amplifier for a specified accuracy of computing.

Variations of amplifier input resistance are expected with time, temperature, and signal level. Whether vacuum tube or transistor input stage is used for the computing amplifier, variations of the input-resistance value will have less effect on accuracy when it is many times larger than the input summing resistors.

All in all, a lowered input resistance of the operational amplifier, as transistors would necessitate, requires increased amplifier gain for a given accuracy in all of the operations. Amplifiers which have low input resistance, such as those built with transistors, can be used for those voltage-analogue computing operations where the above effects are not important.

III. Early Current-Computing Circuit Tests

As soon as the principles of computing with current as the analogue variable had been resolved, methods were sought to confirm its operation in the laboratory. Because of the simplicity, compared to a DC amplifier, of designing and building a junction-

transistor AC amplifier (where bias and signal paths are isolated from each other), such an AC circuit was first undertaken. It had low input impedance, high output impedance, and reasonably high current gain, as noted desirable in Chapter Three, Section I. The design of this amplifier was based upon the following specifications:

(1) Maximum class A output within the limit of 50 milliwatts collector dissipation.

(2) Three common-emitter stages (yielding a phase reversal) to provide a net current gain of 1000 (60 decibels).

(3) An input impedance for each stage of 1000 ohms for a loading resistance of 1000 ohms. Iterative cascading is thus possible.

(4) Stability when overall gain has been reduced to unity by negative feedback.

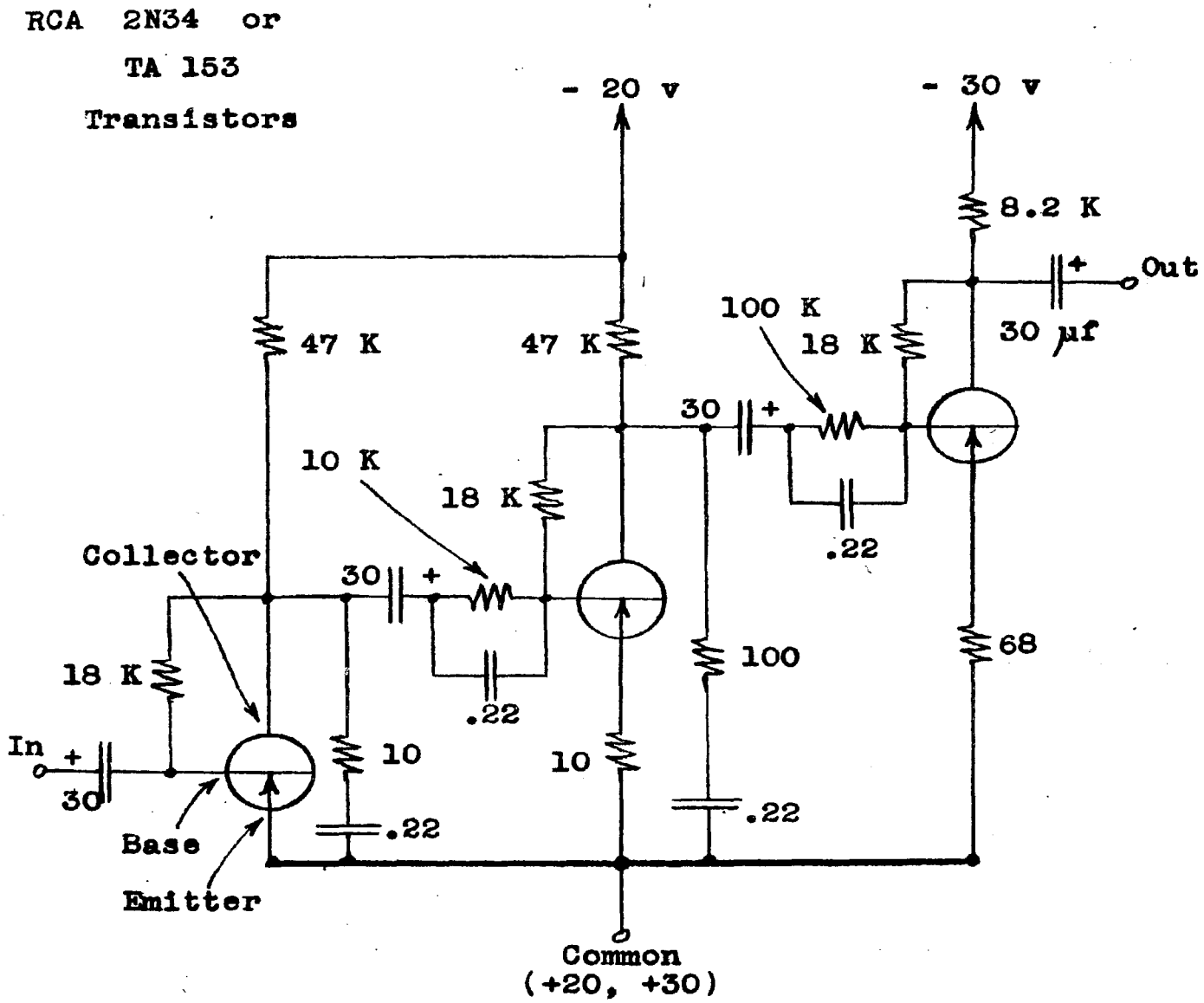
Based on sinusoidal signals such a circuit was tested with feedback in the current-computer connection of Figure 1-1(b). Considerable stabiliziation was necessary at both high and low frequencies to control gain and phase responses. Four control networks were added.

The resultant circuit is shown in Figure II-2. It has a measured current gain of 65 decibels over a bandwidth of two-and-a-half decades at the three-decibel points. It is stabilized for any amount of degenerative feedback in the isolation or summing operation.

Using sinewave signals the basic concepts of current computing were proven reliable, and work then began on the direct-coupled amplifier shown in Figure 2-1. The AC amplifier itself might be useful for the repeated-solution type of analogue computer where bandwidth requirements are moderate.

A C TRANSISTOR CURRENT-COMPUTING AMPLIFIER

For Narrow Bandwidth Uses



Resistance is in ohms, Capacitance in microfarads.

Figure II-2

APPENDIX III

Pertinent Four-Terminal Network Relations

On several occasions throughout the thesis study it has proven advantageous to use modified 4-terminal network parameters to express the apparent properties of a 3-terminal device. This method has been applied to the following devices:

(1) The simple transistor, of both point-contact and junction types;

(2) The basic computing amplifier without precision computing components;

(3) The overall operational unit consisting of high-gain amplifier and precision passive computing elements.

Figure III-1 shows the modified network form which has been used as a general tool in circuit analysis.

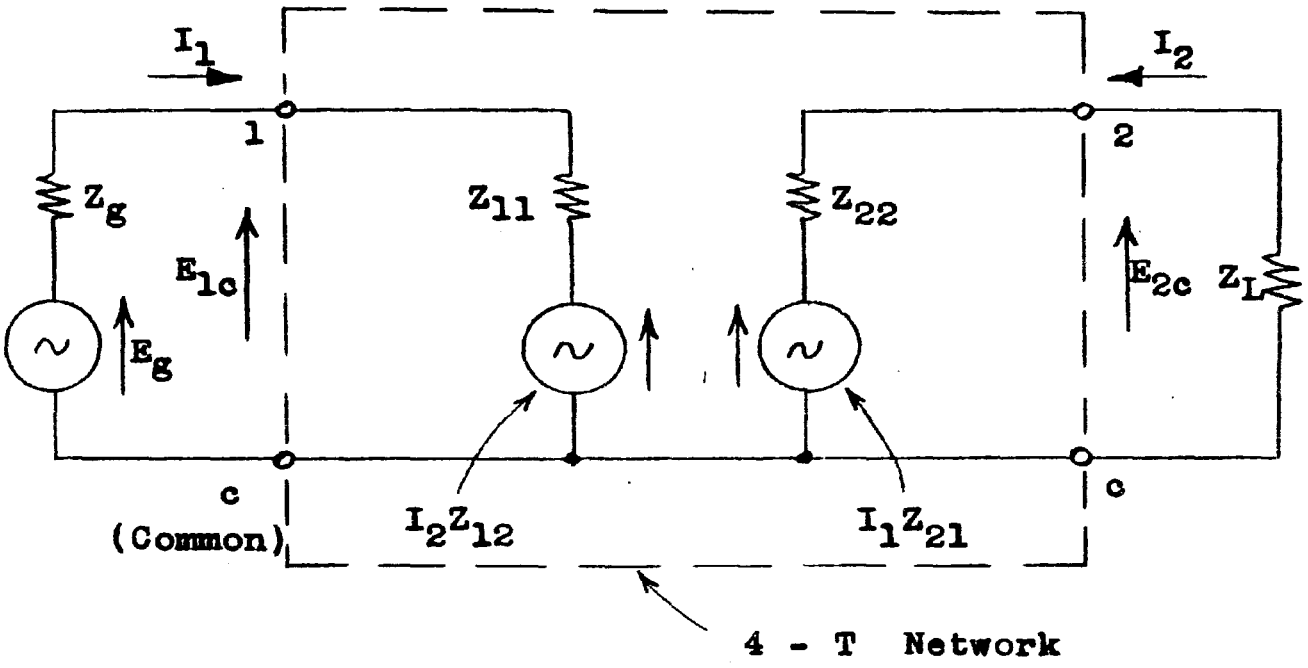
The two loop equations

$$E_{1c} = I_1 Z_{11} + I_2 Z_{12}^{*} \qquad (1)$$

$$E_{2c} = I_1 Z_{21} + I_2 Z_{22} \qquad (2)$$

* The symbols used are listed in Appendix I.

MODIFIED FOUR - TERMINAL NETWORK



$$E_{1c} = I_1Z_{11} + I_2Z_{12} = E_g - I_1Z_g \qquad (1)$$

$$E_{2c} = I_1Z_{21} + I_2Z_{22} = - I_2Z_L \qquad (2)$$

Figure III-1

are supplemented by the equivalent generator and load as shown in the Figure to provide, by direct manipulation of the equations, the following useful relationships:

(1) Input impedance, Z_{in}, seen between the terminals marked "1" and "c" toward the right

$$Z_{in} = Z_{11} - \frac{Z_{12} Z_{21}}{Z_{22} + Z_L} \tag{3a}$$

$$Z_{in,\ oc} \equiv Z_{in}\Big|_{Z_L \to \infty} = Z_{11} \tag{3b}$$

$$Z_{in,\ sc} \equiv Z_{in}\Big|_{Z_L = o} = \frac{Z_{11} Z_{22} - Z_{12} Z_{21}}{Z_{22}} \tag{3c}$$

(2) Output impedance, Z_{out}, seen to the left of terminals 2-c

$$Z_{out} = Z_{22} - \frac{Z_{12} Z_{21}}{Z_{11} + Z_g} \tag{4a}$$

$$Z_{out,\ oc} \equiv Z_{out}\Big|_{Z_g \to \infty} = Z_{22} \tag{4b}$$

$$Z_{out,\ sc} \equiv Z_{out}\Big|_{Z_g = o} = \frac{Z_{11} Z_{22} - Z_{12} Z_{21}}{Z_{11}} \tag{4c}$$

(3) Voltage gain, K_V, with load Z_L

$$K_V \equiv \frac{E_{2c}}{E_{1c}} = \frac{Z_{21}\, Z_L}{(Z_{22} + Z_L)\, Z_{11} - Z_{12}\, Z_{21}} \qquad (5a)$$

$$\mu \equiv K_V \Big|_{Z_L \to \infty} = \left.\frac{\partial E_{2c}}{\partial E_{1c}}\right|_{\substack{I_2 \\ \text{constant}}} = \frac{Z_{21}}{Z_{11}} \qquad (6)$$

$$K_V = \frac{\mu Z_L}{Z_{22} + Z_L - \mu Z_{12}} = \frac{Z_{21}\, Z_L}{Z_{in}\,(Z_{22} + Z_L)} \qquad (5b)$$

(4) Current gain, K_I, with load Z_L

$$K_I \equiv -\frac{I_2}{I_1} = \frac{Z_{21}}{Z_{22} + Z_L} \qquad (7a)$$

$$\alpha \equiv K_I \Big|_{Z_L = o} = -\left.\frac{\partial I_2}{\partial I_1}\right|_{\substack{E_{2c} \\ \text{constant}}} = \frac{Z_{21}}{Z_{22}} \qquad (8)$$

$$K_I = \frac{\alpha Z_{22}}{Z_{22} + Z_L} = \frac{Z_{in}}{Z_L} K_V \qquad (7b)$$

(5) Power gain, K_P, with load Z_L

$$K_P = K_V K_I = \frac{Z_{21}^2 Z_L}{(Z_{22} + Z_L)^2 Z_{11} - (Z_{22} + Z_L) Z_{12} Z_{21}} \qquad (9)$$

(6) Impedance gain, K_R

$$K_R \equiv \frac{Z_L}{Z_{in}} = \frac{(Z_{22} + Z_L)\, Z_L}{Z_{11}\, Z_{22} - Z_{12}\, Z_{21} + Z_{11}\, Z_L}$$

$$= \frac{K_V}{K_I} = \frac{K_P}{K_I^2} \qquad (10)$$

(7) Transconductance, G_m

$$G_m \equiv - \left.\frac{\partial I_2}{\partial E_{1c}}\right|_{\substack{E_{2c} \\ \text{constant}}} = \frac{Z_{21}}{Z_{11}\, Z_{22} - Z_{12}\, Z_{21}} \qquad (11)$$

(8) Stability and Circuit Determinant, Δ

$$\Delta \equiv \begin{vmatrix} Z_{11} + Z_g & Z_{12} \\ Z_{21} & Z_{22} + Z_L \end{vmatrix} > 0 \qquad (12)$$

(9) The four equivalent lumped impedance parameters may conveniently be measured for a given network in terms of the following relations:

$$Z_{11} = Z_{in,\ oc} \qquad (3b)$$

$$Z_{12} = \frac{Z_{in,\ oc} - Z_{in,\ sc}}{\alpha} \tag{13}$$

$$Z_{21} = \mu Z_{in,\ oc} \tag{14}$$

$$Z_{22} = \frac{\mu}{\alpha} Z_{in,\ oc.} \tag{15}$$

APPENDIX IV

Error Deviations

I. General Definitions

(1) Operational Unit Transfer Function is given for current computing by

$$\frac{I_2(p)}{I_1(p)} = -K_I' \cong \frac{-Z_i K_I}{Z_i + Z_{11} + (1-K_I) Z_f} \qquad (1)$$

from Equation (3-8) of Chapter Three, where:

$I_2(p)$ is the Laplace transform of output current.

$I_1(p)$ is the Laplace transform of input current.

K_I' is the overall complex current gain.

K_I is the current gain of amplifier alone.

Z_i is the summing element impedance.

Z_{11} is the four-terminal network equivalent input circuit loop impedance of the amplifier.

Z_f is the feedback element impedance.

(2) Complex current gain of the amplifier along with

approximately a zero impedance load is assumed to have the form

$$K_I(p) = \frac{K_{I_o}}{1 + \frac{p}{\omega_o}} \qquad (2)$$

where:

K_{I_o} is the current gain of the amplifier at zero frequency.

p is a complex variable.

ω_o is 2π times the "break" frequency or half-power point of amplifier's steady-state gain response.

K_{I_o} and ω_o are assigned numerical values by curve-matching the empirical curve of amplifier frequency response, such as Figure 3-2, as well as possible. The matching curve might be deliberately located below the measured curve in all significant areas to result in a conservative appraisal of error.

(3) Fractional Error, FE

$$\text{Instantaneous FE} = \frac{\text{Ideal } i_2(t) - \text{Actual } i_2(t)}{\text{Ideal } i_2(t)} \qquad (3)$$

where

$i_2(t)$ is instantaneous unit output current.

$$\text{RMS FE} = \sqrt{\frac{1}{T}\int_0^T \text{FE}^2(t)\,dt} \qquad (4)$$

where

T is the computing interval measured from the application of the input waveform.

(4) The following numerical values are typical of those measured and used in the experiments with current computing. These values will be used in calculating the typical numerical results of error analysis which are shown here.

Conservative minimum values assumed from Figure 3-2:

$$\begin{cases} K_{I_o} = -2000 \\ \omega_o = 2\pi\, 40 \end{cases}$$

Measured maximum value for the amplifier:

$$Z_{11} = 3200.\,\Omega = R_{11}$$

For Isolation let: $Z_i = 2000.\ \Omega = R_i$

$Z_f = 2000.\ \Omega = R_f$

Input waveform is a Step, expressed by its Laplace transform. $I_1(p) \equiv I_o/p$

For Integration let: $Z_i = \frac{1}{pc} = \frac{10^5}{p}\ \Omega$

thus $C = 10.\ \mu f$

$Z_f = 2000.\ \Omega = R_f$

Input is an Impulse, $I_1(p) \equiv I_o$

For Differentiation let: $Z_i = pL = 13.5\,p\ \Omega$

thus $L = 13.5$ hen.

$Z_f = 2000.\ \Omega = R_f$

Input is a Ramp, $I_1(p) \equiv I_o/p^2$

where I_o is a constant throughout.

II. Operation of Isolation

(Same operational unit and Z_i and Z_f may be used for Summing and for Phase Inverting)

$$\frac{I_2(p)}{I_1(p)} = \frac{-R_i \omega_o K_{I_o}}{(R_i + R_{11} + R_f)(\omega_o + p) - R_f \omega_o K_{I_o}} \qquad (5)$$

from Equations (1) and (2).

Z_i, Z_{11}, and Z_f are assumed purely resistive, as in Figure 2-4.

$$I_1(p) \equiv I_o/p$$

The Laplace transform of the actual output signal is given by

$$I_2(p) = \frac{-R_i I_o K_{I_o} \omega_o}{p\left[pR + \omega_o (R - R_f K_{I_o})\right]} \qquad (6)$$

where $$R \equiv R_i + R_{11} + R_f \qquad (7)$$

Finding the inverse transform,

$$i_2(t) \text{ (Actual)} = \frac{-R_i I_o K_{I_o}}{R - R_f K_{I_o}} \left[1 - e^{-\omega_o (1 - \frac{R_f}{R} K_{I_o}) t}\right] \qquad (8)$$

Ideally, for this input waveform, $i_2(t)$ would have the form

$$\frac{R_i}{R_f} I_o \tag{9}$$

From Equation (3):

$$FE(t) = 1 + \frac{R_f K_{I_o}}{R - R_f K_{I_o}} \left[1 - e^{-\omega_o \left(1 - \frac{R_f}{R} K_{I_o}\right) t} \right] \tag{10a}$$

For a specific case it is convenient to substitute actual numerical values at this point. Using the values of I (4)

$$FE(t) = .0016 + .9984\ e^{-155,000\,t} \tag{10b}$$

FE (t) is sketched for these values in Figure IV-1(a) on the next page.

By substitution into Equation (4):

$$(\text{RMS FE})^2 \simeq (.0016)^2 - \frac{2 \times .0016 \times .9984}{155,000\,T} \left(e^{-155,000\,T} - 1 \right) - \frac{.9984^2}{2 \times 155,000\,T} \left(e^{-2 \times 155,000\,T} - 1 \right) \tag{11}$$

RMS FE is plotted from this expression as a function of T, the period of averaging, in Figure 4-2.

INSTANTANEOUS FRACTIONAL ERRORS

With Calculated Numerical Values

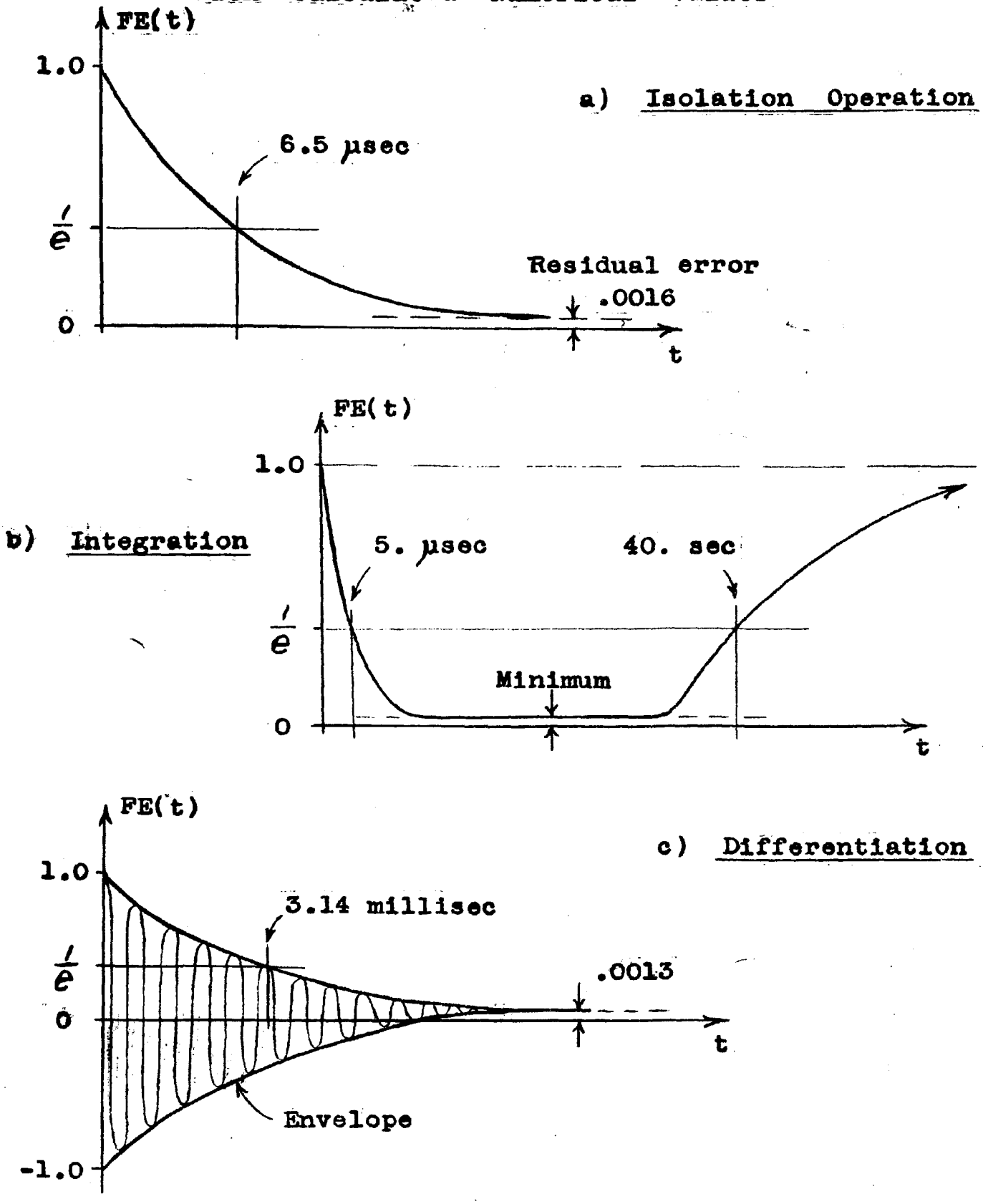


Figure IV-1

III Operation of Integration

$$\frac{I_2\,(p)}{I_1\,(p)} = -\frac{-\omega_o K_{I_o}}{(1 + pCR_{11} + pCR_f)(\omega_o + p) - pCR_f \omega_o K_{I_o}} \qquad (12)$$

from Equations (1) and (2).

$Z_i = \frac{1}{pC}$, and Z_{11} and Z_f are resistive, as in Figure 2-8.

$I_1\,(p) \equiv I_o$

The Laplace transform of the output is

$$I_2\,(p) = \frac{-\omega_o K_{I_o} I_o}{p^2 T_1 + p\,(T_1 \omega_o + 1 - CR_f \omega_o K_{I_o}) + \omega_o} \qquad (13a)$$

$$= \frac{-\omega_o K_{I_o} I_o}{T_1} \frac{1}{(p + A)(p + B)} \qquad (13b)$$

where the following terms are defined here:

$$T_1 \equiv C\,(R_{11} + R_f)$$

$$A \equiv + \frac{D}{2} + \sqrt{\frac{D^2}{4} - \frac{\omega_o}{T_1}}$$

$$B \equiv + \frac{D}{2} - \sqrt{\frac{D^2}{4} - \frac{\omega_o}{T_1}}$$

$$D \equiv \omega_o + \frac{1}{T_1} - \frac{CR_f\, \omega_o K_{I_o}}{T_1}$$

The inverse transform yields

$$i_2\ (t)\ (\text{Actual}) = \frac{-\omega_o K_{I_o} I_o}{T_1} \cdot \frac{e^{-Bt} - e^{-At}}{A-B} \tag{14a}$$

$$= \frac{\omega_o K_{I_o} I_o}{T_1\sqrt{D^2 - \frac{4\omega_o}{T_1}}} \left(e^{-At} - e^{-Bt}\right) \tag{14b}$$

$$i_2(t)\ (\text{Ideal}) = \frac{I_o}{CR_f} \tag{15}$$

$$FE\ (t) = 1 - G\left(e^{-At} - e^{-Bt}\right) \tag{16a}$$

where we let

$$G \equiv \frac{CR_f \omega_o K_{I_o}}{T_1\sqrt{D^2 - \frac{4\omega_o}{T_1}}}$$

$$(\text{RMS FE})^2 = 1 - \frac{2G}{T}\left(\frac{e^{-BT}}{B} - \frac{e^{-AT}}{A}\right) +$$

$$\frac{2G(A-B)}{ABT} - \frac{G^2}{T}\left(\frac{e^{-2BT}}{2B} + \frac{e^{-2AT}}{2A} -\right.$$

$$\left.\frac{2e^{-(A+B)T}}{A+B}\right) + \frac{G^2}{T}\left(\frac{A+B}{2AB} - \frac{2}{A+B}\right) \tag{17a}$$

where T is again the whole interval in which this computation is observed.

Substituting numerical values from I (4):

$$T_1 = .052 \text{ sec.}, \qquad D = 61,680\ \pi \text{ sec.}^{-1}$$

$$\sqrt{\frac{D}{4} - \frac{\omega_o}{T_1}} = \frac{D}{2} - \frac{\omega_o}{DT_1} - \frac{\omega_o^2}{D^3 T_1^2} - \cdots\cdots$$

by series expansion. It converges very rapidly for the values involved.

$$A = 61,680\ \pi = 194,000 \text{ sec}^{-1}$$

$$B = .008\ \pi = .025 \text{ sec}^{-1}$$

$$G = -.99881$$

$$FE(t) = 1 + .99881 \left(e^{-194,000t} - e^{-.025t} \right)$$

It is noted that FE (t) is described by two exponentials, one having a short-time effect and the other a long-time effect upon accuracy. The components of this function are sketched in Figure IV-1(b).

The operation of integration, as described here, has a single optimum choice of the averaging period "T" for minimum RMS error. The fact that this minimum exists is observed intuitively from the sketch in Figure IV-1(b). Equation (17a) may be solved

for this T of minimum error by equating to zero the derivative of RMS FE with respect to T.

Both Equation (17a) and the expression for the T of minimum RMS error can often be greatly simplified in practical use. For example, for the numerical values used here, when T is a reasonable time interval of interest

$$e^{-At} \ll 1.0.$$

Then

$$(\text{RMS FE})^2 \cong 1 - \frac{G}{2AT}(4 + 3G) + G(2+G) - GBT\left[(1+G) - \frac{BT}{3}(1+2G)\right] \qquad (17b)$$

$$\cong \frac{2.58 \times 10^{-6}}{T} + \frac{T}{120}(.00357 + .02944\,T). \qquad (17c)$$

The square root of Equation (17c) is plotted in Figure 4-2 as RMS FE versus the interval T.

The value of T for minimum RMS error may be most easily found by a graphical method from the derivative of Equation (17c). For these values it is single-valued and is given by:

T (minimum RMS FE) = .1546 seconds.

When T has this value, Equation (17c) yields RMS FE = .52%.

IV Operation of Differentiation

$$\frac{I_2(p)}{I_1(p)} = \frac{-pL\omega_o K_{I_o}}{(R_{11}+R_f+pL)(\omega_o+p)-R_f\omega_o K_{I_o}} \qquad (18)$$

$Z_i = pL$ Z_{11} and Z_f are resistive,

as illustrated in Figure 2-7.

$$I_1(p) = \frac{I_o}{p^2}$$

Substituting to obtain the Laplace transform of output signal,

$$I_2(p) = \frac{-LI_o\omega_o K_{I_o}}{p(R_{11}+R_f+pL)(\omega_o+p)-pR_f\omega_o K_{I_o}} \qquad (19a)$$

$$= \frac{-LI_o\omega_o K_{I_o}}{p\left[p^2L+p(R_{11}+R_f+\omega_o L)+\omega_o(R_{11}+R_f-R_f K_{I_o})\right]} \qquad (19b)$$

Completing the square in the denominator of $I_2(p)$,

$$I_2(p) = \frac{-I_o\omega_o K_{I_o}}{p\left[(p+E)^2+F^2\right]} \qquad (19c)$$

where

$$E \equiv \frac{1}{2}\left(\frac{R_{11}+R_f}{L}+\omega_o\right) \qquad (20)$$

and

$$F^2 \equiv \omega_o\left(\frac{R_{11}+R_f-R_f K_{I_o}}{L}\right)-\frac{1}{4}\left(\frac{R_{11}+R_f}{L}+\omega_o\right)^2 \qquad (21)$$

The inverse transform is found as

$$i_2(t)\ \text{(Actual)} = \left(-I_o\,\omega_o\,K_{I_o}\right)\left\{\frac{1}{E^2+F^2} + \frac{1}{F\sqrt{E^2+F^2}}\,e^{-Et}\sin\left[Ft - \arctan\frac{F}{(-E)}\right]\right\} \quad (22)$$

The Ideal output would be

$$i_2(t) = \frac{I_o L}{R} \quad . \quad (23)$$

$$FE(t) = 1 + \frac{R_f\,\omega_o\,K_{I_o}}{L}\left\{\frac{1}{E^2+F^2} + \frac{1}{F\sqrt{E^2+F^2}}\,e^{-Et}\sin\left[Ft - \arctan\frac{F}{(-E)}\right]\right\} \quad (24a)$$

Upon substitution FE (t) is expressed in terms of the measured quantities:

$$FE(t) = \frac{R_{11}+R_f}{R_{11}+R_f-R_f K_{I_o}} + \frac{2R_f\,K_{I_o}}{R_{11}+R_f-R_f K_{I_o}} \times \sqrt{\frac{L\omega_o\,(R_{11}+R_f-R_f\,K_{I_o})}{-4\,L\omega_o\,R_f\,K_{I_o} - (R_{11}+R_f-\omega_o L)^2}} \times e^{-\frac{1}{2}\left(\frac{R_{11}+R_f}{L}+\omega_o\right)t}$$

$$\sin\left\{t\sqrt{\frac{\omega_o}{L}\,(R_{11}+R_f-R_f\,K_{I_o}) - \frac{1}{4}\left(\frac{R_{11}+R_f}{L}+\omega_o\right)^2} \right. -$$

$$\arctan \left\{ - \sqrt{\frac{4\omega_o L (R_{11} + R_f - R_f K I_o}{(R_{11} + R_f + \omega_o L)^2} - 1} \right\} \quad (24b)$$

Inserting numerical values at this point from I (4)

$$E = 318.\ \text{sec.}^{-1} \qquad F = 8610.\ \text{sec.}^{-1}$$

$$E^2 + F^2 = 74.6 \times 10^6$$

$$FE(t) = .00130 + .9994\, e^{-318t} \cos (8610t - 2.113°) \quad (24c)$$

The major components of this function are sketched in Figure IV-1(c). The time constant of exponential decay of the envelope of FE(t) is 3.14 milliseconds. One cycle of the oscillatory transient takes only .116 milliseconds, or 1/27 as long.

Let

$$FE(t) = H + M\, e^{-Et} \cos (Ft - N) \quad (24d)$$

where, for this example

$$H \equiv .0013 \qquad M \equiv .9994$$

$$E = 318. \qquad F = 8610.$$

$$N \equiv 2.113° = .037 \text{ radian}$$

The quantities H, M, and N can, of course, be expressed in general, analytical form from Equation (24b).

The exact form for mean-square error is given by:

$$(\text{RMS FE})^2 = H^2 + \frac{M}{4T\,(E^2+F^2)} \left\{ \frac{MF^2}{E}\left(1-e^{-2ET}\right) + \right.$$

$$2M\cos^2 N \left[e^{-2ET} \cos FT \ (F \sin FT - E \cos FT) + E \right] -$$

$$2M \sin^2 N \ e^{-2ET} \sin FT \ (E \sin FT + F \cos FT) +$$

$$M \sin 2N \left[F - (E \sin 2FT + F \cos 2FT)\, e^{-2ET} \right] +$$

$$8H \cos N \left[E + (F \sin FT - E \cos FT)\, e^{-ET} \right] +$$

$$\left. 8H \sin N \left[F - (E \sin FT + F \cos FT)\, e^{-ET} \right] \right\} \qquad (25a)$$

A reasonable approximation for FE(t) in Equation (24d) is considerably simpler for the usual design purposes. It depends on the period of the oscillations being short compared to the exponential decay, where the effective value of FE(t) is given by

$$FE(t) \cong \sqrt{H^2 + \frac{M^2}{2}\, e^{-2ET}} \qquad (24e)$$

Then the simplified mean-square error expression for our example is:

$$(\text{RMS FE})^2 \cong H^2 + \frac{M^2}{4ET}\left(1-e^{-2ET}\right) \qquad (25b)$$

$$= 1.69 \times 10^{-6} + \frac{774 \times 10^{-6}}{T}\left(1-e^{-636.T}\right) \qquad (25c)$$

The square root of this expression is plotted as RMS FE versus the time interval of averaging, T, in Figure 4-2.

BIBLIOGRAPHY

1. Becker, J. A. and Shive, J. N., "The Transistor--A New Semiconductor Amplifier", Electrical Engineering, pages 215-221, March, 1949.

2. Macnee, A. B., "Some Limitations on the Accuracy of Electronic Differential Analyzers", Proceedings of the I. R. E., pages 303-308, March, 1952.

3. Meneley, C. A. and Morrill, C. D., "Application of Electronic Differential Analyzers to Engineering Problems", Proceedings of the I. R. E., pages 1487-1496, October, 1953.

4. Goldberg, Edwin A., "Stabilization of Wide-Band Direct-Current Amplifiers for Zero and Gain", RCA Review, June 1950, 296-300.

5. Korn, G. A. and T. M., "Electronic Analog Computers", first ed., 1952, McGraw-Hill Book Co., New York.

6. M. I. T. Radiation Laboratory Series, Volume 21, Greenwood, Holdam, and MacRae, "Electronic Instruments", first ed., 1948, McGraw-Hill Book Co., New York.

7. Shea, Richard F. (Editor), "Principles of Transistor Circuits", first ed., 1953, John Wiley and Sons, New York.

8. Hellerman, H., "Some Transistor Building Blocks for Analogue Computers", Communications and Electronics (AIEE), pages 410-413, September, 1954.

9. Bode, H. W., "Relations Between Attenuation and Phase in Feedback Amplifier Design", Bell System Technical Journal, pages 421-454, July, 1940.

10. Ragazzini, J. R., Randall, R. H., and Russell, F. A., "Analysis of Problems in Dynamics by Electronic Circuits", Proceedings of the I. R. E., pages 444-452, May, 1947.

11. Wallace, R. L., Schimpf, L. G., and Dicten, E., "A Junction Transistor Tetrode for High-Frequency Use", Proceedings of the I. R. E., pages 1395-1400, November, 1952.

12. Angell, J. B. and Keiper, F. P., "Circuit Applications of of Surface-Barrier Transistors", Proceedings of the I. R. E., pages 1709-1712, December, 1953.

13. M. I. T. E. E. Staff, "Applied Electronics", 1943, John Wiley and Sons, New York.

14. Nyquist, H., "Regeneration Theory", Bell System Technical Journal, 11, pages 126-147, July, 1932.

15. Mueller, C. W. and Pankove, J. I., "A PNP Triode Alloy-Junction Transistor for Radio-Frequency Amplification", Proceedings of the I. R. E., pages 386-391, February, 1954.

16. Sziklai, G. C., "Symmetrical Properties of Transistors and Their Applications", Proceedings of the I. R. E., pages 717-724, June, 1953.

17. Ghandi, S. K., "Design of Transistor Power Amplifiers", Electronics, pages 146-149, March, 1954.

18. Bode, H. W. and Shannon, C. E., "A Simplified Derivation of Linear Least Square Smoothing and Prediction Theory", Proceedings of the I. R. E., pages 417-425, April, 1950.

19. Shockley, W., "Electrons and Holes in Semiconductors", second printing, 1951, D. VanNostrand Co., New York.

20. Giacoletto, L. J. "Terminology and Equations for Linear Active Four-Terminal Networks Including Transistors", RCA Review, March, 1953.

21. Webster, W. M., Eberhard, E., and Barton, L. E., "Some Novel Circuits for the Three-Terminal Semiconductor Amplifier", RCA Review, pages 5-10, March, 1949.