Investigation of Dielectric Reliability with β–Gallium Oxide for Future Power Devices

by

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To my parents.
Thank you for everything.

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ABSTRACT

The growing dependence on electrical energy has made the development of high-performing power electronics crucial; this has led to significant interest in the use of ultra-wide bandgap semiconductors (UWBG) in power devices as they demonstrate improved efficiencies compared to silicon. Research in β-Gallium Oxide or β-Ga_2O_3 has grown in popularity due to its large bandgap (4.6 – 4.9 eV) and high expected breakdown field (>6 MV/cm). The development of high-performing, stable β-Ga_2O_3 metal-oxide-semiconductor (MOS) devices requires the optimization of the gate dielectric-semiconductor interface. The unique aspects of β-Ga_2O_3, including its ultra-large bandgap and its self-trapping hole behavior, presents many questions about the impact of the UWBG semiconductor on MOS reliability. In this thesis I will investigate the impact of dielectric material, deposition technique, and nonplanar MOS structure on interface defects, reliability and photo-response with β-Ga_2O_3.

First, I demonstrated a solution-processed high-κ dielectric, $(Y_{0.6}Sc_{0.4})_2O_3$, with β-Ga_2O_3 in MOS capacitors (MOSCAPs) and analyzed the interface quality between the ternary dielectric and the UWBG semiconductor. A low total interface trap charge (D_{it}) of $< 10^{12}\ cm^{-2}$ was extracted using the photo-assisted capacitance - voltage (*C-V*) technique, which indicates a clean interface between $(Y_{0.6}Sc_{0.4})_2O_3$ and β-Ga_2O_3. Due to the need of a conformal dielectric for non-planar structures, I next investigated the reliability of atomic layer deposited (ALD) HfO_2/β-Ga_2O_3 MOSCAPs. Positive bias stress measurements were used to investigate charge trapping in these MOSCAPs, and a comparison to HfO_2/Si was made to determine how the unique characteristics of β-Ga_2O_3 impacted the charge trapping and recovery observed here as opposed to a smaller bandgap semiconductor (i.e. Si). β-Ga_2O_3 MOSCAPs are shown to be more susceptible to charge trapping at lower electric stress fields, and border traps play a significant role in the initial flatband

voltage shifts observed when *C*-*V* sweeps are repeated due to the lack of mobile holes in β-Ga_2O_3.

Next, the thermal reliability of the ALD HfO_2/β-Ga_2O_3 interface was investigated due to the known diffusion issues β-Ga_2O_3 has with many materials including Al_2O_3. Secondary ion mass spectrometry (SIMS) depth profile showed negligible Ga diffusion in the HfO_2 layer up to annealing temperatures of 850°C in N_2 environment, but increases in forward bias leakage and D_{it} were observed in MOSCAPs annealed at 700°C compared to MOSCAPs annealed below 500°C. Annealing at 900°C resulted in significant Ga diffusion into the HfO_2 layer providing poor electrical insulation for the UWBG semiconductor. Lastly, I studied vertical MOS structures on etched β-Ga_2O_3, inspired by the vertical fin-MOSFET structure, which shows promising enhancement-mode behavior as a β-Ga_2O_3 MOS device. A fabrication process for HfO_2/β-Ga_2O_3 fin MOSCAPs arrays has been developed, and initial analysis shows that the MOSCAPs on plasma-etched fin sidewalls of β-Ga_2O_3 may have significantly higher D_{it} compared to planar MOSCAPs using the same ALD dielectric. The techniques used throughout this thesis can be utilized in future UWBG semiconductor MOS device research.

CHAPTER 1

Introduction

1.1 Introduction to β-Gallium Oxide

Power electronics have become a crucial research interest as the dependence on electrical energy has increased. An estimated 30% of all electrical energy is converted through power electronics, and this is expected to increase significantly over the next decade [14]. There has been a major push towards using wide bandgap semiconductors (WBG) in power devices for their improved efficiencies compared to Si devices. WBG semiconductors have large critical breakdown fields, E_C, which contributes significantly to their high Baliga's Figure of Merit (BFOM). BFOM, determined by $\sim \epsilon_s \mu_n E_C^3$, is based on the specific resistance of an ideal drift region and is an excellent indicator for the material's promise in power devices [15]. As Figure 1.1 shows, using a WBG semiconductor can greatly reduce the specific on-resistance of the device when compared to a Si device with the same breakdown voltage. This has led to the development of WBG semiconductor devices including SiC and GaN.

Over the last decade interest in Gallium Oxide or β-Ga_2O_3, an ultra-WBG (UWBG) semiconductor, has grown tremendously for its potential in future power devices. β-Ga_2O_3 is the most stable of the five Ga_2O_3 polymorphs, which has a monoclinic structure (Figure 1.2). Depending on growth conditions, this material can be either semiconducting or insulating [3]. β-Ga_2O_3 is seen as a promising competitor to 4H-SiC and GaN for use in power devices, due to its ultra-wide bandgap of 4.6 – 4.9 eV and its high expected breakdown field of 8 MV/cm. These impressive material

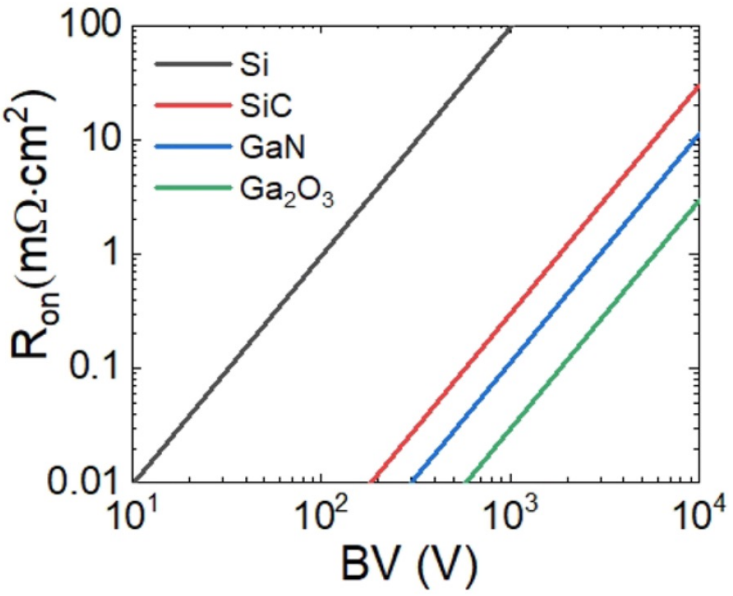


Figure 1.1: Ideal specific on-resistance vs. breakdown voltage

properties (shown in Table 1.1) result in a significantly larger BFOM, compared to 4H-SiC and GaN.

While β-Ga_2O_3 was first reported in the 1950s [16], it was the impressive advances in various growth methods resulting in large-area single crystal substrates that led to the research community's excitement for potential β-Ga_2O_3 devices. β-Ga_2O_3 crystals can be grown by many common melt-growth techniques that are already implemented in industry. These techniques include Czochralski [17], floating-zone [18], edge-defined film fed (EFG) [19], and vertical Bridgman growth methods [20]. This is a key benefit of β-Ga_2O_3 over SiC and GaN, which require more costly growth methods including sublimation, vapor phase epitaxy, and high-pressure synthesis [21]. Single-crystalline wafers as large as 4 inches can be purchased from Novel Crystal Technology, Inc., which has been the pioneer in β-Ga_2O_3 substrates with the research help of Tamura Corporation and the National Institute of Information and Communications Technology (NICT) in Japan. Commercial substrates are also available in the United States from Kyma/Synoptics, and bulk substrates for research purposes are available from Leibniz Institute for Crystal Growth (IKZ) in Berlin, Germany.

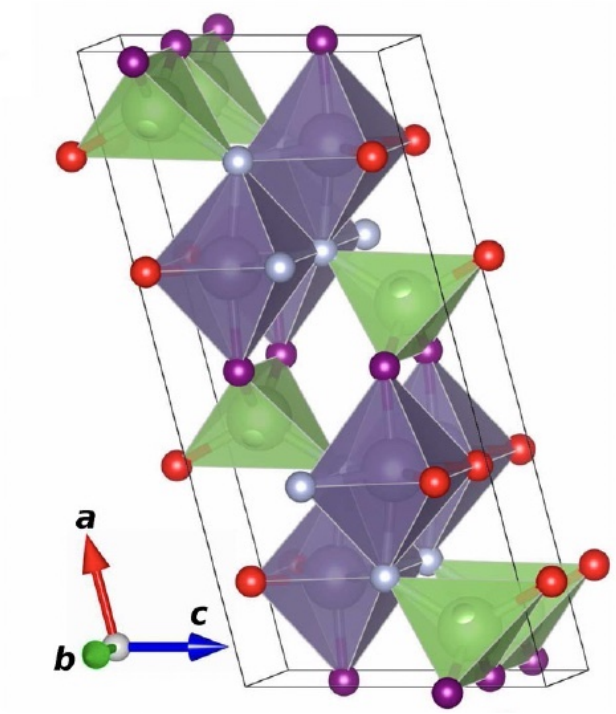


Figure 1.2: Atomic unit cell of β-Ga_2O_3 showing its monoclinic crystal structure. Larger spheres represent Ga and smaller spheres represent O. Reprinted from [1], with the permission of John Wiley and Sons.

Material parameters	**Si**	**4H-SiC**	**GaN**	**β-Ga_2O_3**
Bandgap (eV)	1.1	3.25	3.4	4.6-4.9
Breakdown field, E_C (MV/cm)	0.3	2.5	3.3	8
Electron mobility, μ_n (cm^2/Vs)	1480	1000	1250	300
Dielectric constant, ϵ_s	11.8	9.7	9	10
Thermal conductivity, λ ($W/cm*K$)	1.5	4.9	2.3	0.1-0.3
Saturation velocity, V_s ($10^7 cm/s$)	1	2	2.5	1.8-2
Baliga's FOM ($\sim\epsilon_s\mu_n {E_C}^3$)	1	317	846	3214
Johnson's FOM ($\sim {E_C}^2 {V_s}^2/(4\pi^2)$)	1	278	1089	2844
Combined's FOM ($\sim\lambda\epsilon_s\mu_n V_s {E_C}^2$)	1	249	354	37
Baliga high frequency ($\sim\mu_n {E_C}^3$)	1	46	101	142
Keyes's FOM ($\sim\lambda[cV_s/(4\pi\epsilon_s)]^{1/2}$)	1	3.6	1.8	0.2

Table 1.1: Properties of β-Ga_2O_3 compared to Si and other wide bandgap semiconductors. Adapted from [13].

1.2 Difficulties with β-Ga_2O_3

While there are many properties that make β-Ga_2O_3 a fascinating material for future power devices, there are a few characteristics that present challenges in this area of research. One of the most notable challenges, as displayed in Table 1.1, is the low thermal conductivity. The thermal conductivity varies in the different crystal directions with its peak at 0.27 W/cm K in the [010] direction; this is significantly lower than its WBG competitors [13]. The low thermal conductivity can hinder the device performance as well as negatively affect the long-term reliability of the device. This has led to the investigation of thermal management solutions, such as bonding the Ga_2O_3 substrate to a semiconductor substrate, like SiC, with improved thermal properties [22]. Due to the typical high operating temperatures of power devices, more research in temperature reliability and the effect of the low thermal conductivity in β-Ga_2O_3 needs to be conducted.

Controllable n-type doping has been demonstrated on β-Ga_2O_3 with concentrations of 10^{15} – 10^{19} cm^{-3}, but p-type doping has yet to be demonstrated. This provides an additional challenge to β-Ga_2O_3 devices [13]. The difficulty of p-type doping stems from a few key issues: many traditional acceptor dopants have large activation energies within β-Ga_2O_3 [23], β-Ga_2O_3 has a relatively flat valence band (as shown in the band structure in Figure 1.3) leading to holes of heavy effective mass and low mobilities [2], and this UWBG semiconductor exhibits hole self-trapping behavior [24, 25]. These issues have led many researchers to question if p-type doping in β-Ga_2O_3 will ever be achieved. The lack of p-type doping creates difficulty in fabricating enhancement-mode (normally-off) devices. Enhancement-mode versus depletion-mode refers to the state of current conduction at a gate voltage of 0 V. An enhancement-mode device will show negligible current conduction at 0 V and a positive gate voltage (in the case of n-channel devices) is required to turn the device on, as shown in the top figures of Figure 1.4 [3]. In contrast, depletion-mode devices

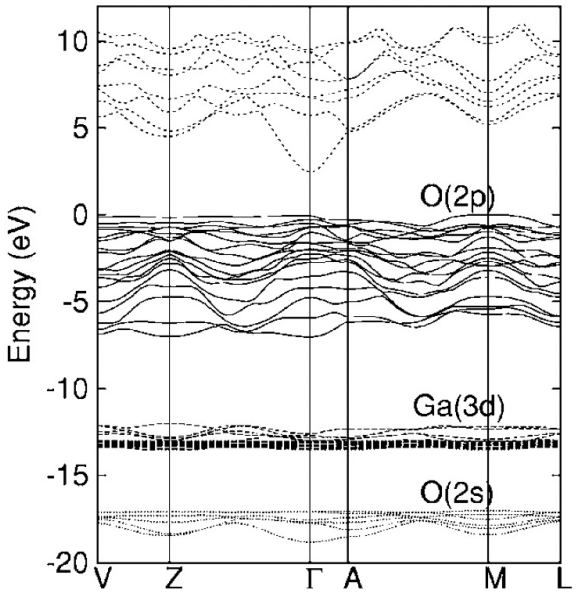


Figure 1.3: Band structure of β-Ga_2O_3 showing the flat valence band, which greatly contributes to the difficulty of p-type doping and hole mobility. Reprinted from Appl. Phys. Lett. **88**, 261904 (2006), with the permission of AIP Publishing. [2]

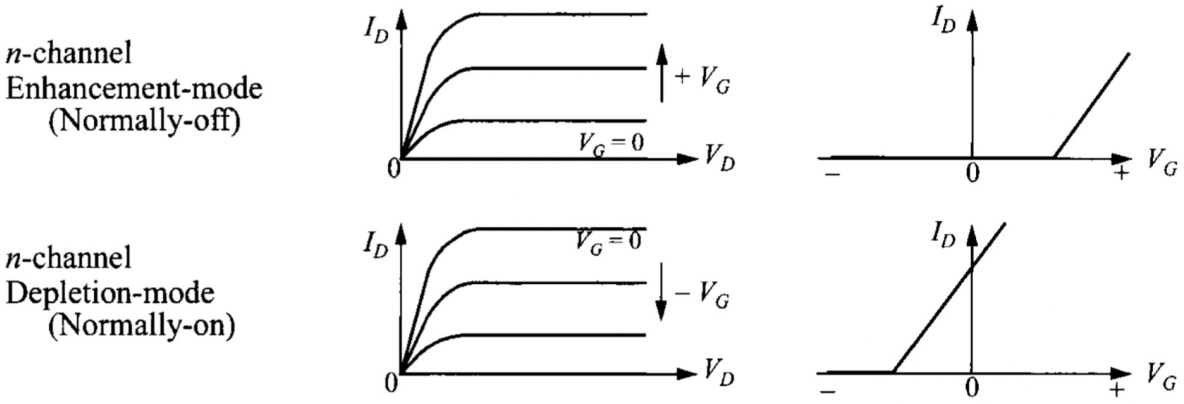


Figure 1.4: Output and transfer *I-V* curves of n-channel enhancement-mode and depletion-mode MOSFETs. Reprinted from [3] with permission from John Wiley and Sons.

will have current flowing in the channel at 0 V and require and negative gate voltage to turn off the device (bottom figures of Figure 1.4) [3]. The use of depletion-mode devices will result in high conduction loss due to the non-negligible current at 0 V. Enhancement-mode devices are desired as they enable fail-safe operation and simplified circuit designs [23]. Device structures that do not require p-n junctions have been heavily focused on due to this drawback.

1.3 Current state of β-Ga_2O_3 devices

Even with the challenges of this WBG semiconductor, tremendous progress has been made in β-Ga_2O_3 devices. The first transistor with β-Ga_2O_3, a metal-semiconductor field-effect transistor (MESFET), was demonstrated by Higashiwaki, et al., in 2012. Excellent characteristics were displayed for this first FET device, but issues with high contact resistance and low on/off current ratios were observed [26]. Progress was made quickly, and the first depletion mode (normally-on) metal-oxide-semiconductor field-effect transistors (MOSFETs) were fabricated with β-Ga_2O_3. By incorporating Si–ion implanted regions for source/drain ohmic contacts, and an Al_2O_3 gate insulator, which had a dual role as a surface passivation layer, Higashiwaki et al., achieved a β-Ga_2O_3 depletion-mode MOSFET with an on/off current ratio of $>10^{10}$ and a breakdown voltage (V_{br}) of 370 V [27]. Since these first β-Ga_2O_3 devices were reported, many groups have been working on various β-Ga_2O_3 device structures and have achieved many impressive device goals quickly.

For example, enhancement-mode β-Ga_2O_3 wrap-gate finFETs achieved V_{br} of $>$500 V in 2016 [28]; the same year, a β-Ga_2O_3 MOSFET displayed a gate-to-drain electric field strength $>$3.8 MV/cm, which surpasses the theoretical bulk critical field strengths of GaN and SiC [29]. Thin β-Ga_2O_3 nano-membranes have been utilized in FETs to achieve high drain current [30], and heterostructure metal-insulator-semiconductor FETs (MISFETs) have been developed with exfoliated β-Ga_2O_3 flakes [31]. There has been significant development in modulation doped FETs (MODFETs) with β-$(Al_xGa_{(1-x)})_2O_3$/Ga_2O_3 structures to achieve a high electron density and an electron mobility of 150 cm^2/V s [32]. Large V_{br} have been achieved with field-plated lateral

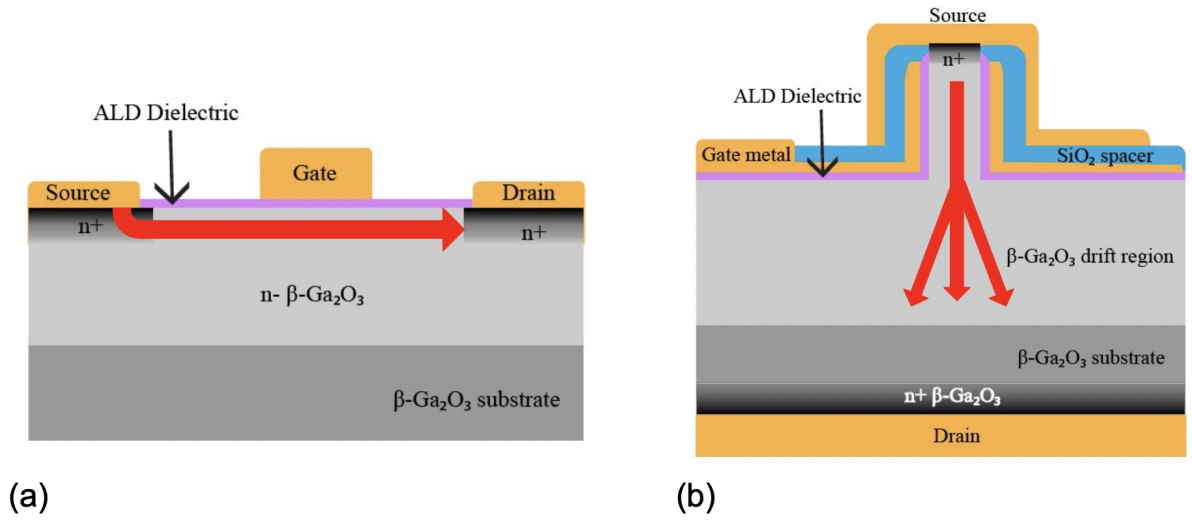


Figure 1.5: Example cross-section schematics of (a) lateral and (b) vertical β-Ga_2O_3 MOSFETs, where the red arrows show the flow of electrons from the source contact to the drain contact.

β-Ga_2O_3 MOSFETs, with recent devices showing >8 kV with polymer passivation [33].

The devices previously mentioned are lateral transistor structures where current is flowing in the lateral direction (Figure 1.5 (a)). While these devices have shown excellent device characteristics, vertical device structures are much more ideal for high-power applications where the voltage and current requirements are >1 kV and >100 A, respectively [11]. Vertical device structures, in which electrons flows from the top (source contact) to the bottom of the substrate (drain contact), as shown in Figure 1.5 (b), have many benefits. The vertical structure can support larger voltages and currents, while maintaining good chip area utilization [15]. The drift layer thickness determines the breakdown voltage, instead of a lateral gate-to-drain distance. The peak electric field is located within the bulk of the device, as opposed to at the surface, reducing the possibility of premature breakdown due to surface defects [23]. The difficulty of fabricating many of the vertical structures, which were previously developed for Si power devices, with β-Ga_2O_3 is the lack of p-type doping capabilities. With this limitation, two vertical device structures have shown to be promising for future β-Ga_2O_3 vertical power devices, current aperture vertical MOSFETs and vertical fin MOSFETs [23].

The current aperture vertical MOSFET structure contains a planar gate with a buried current

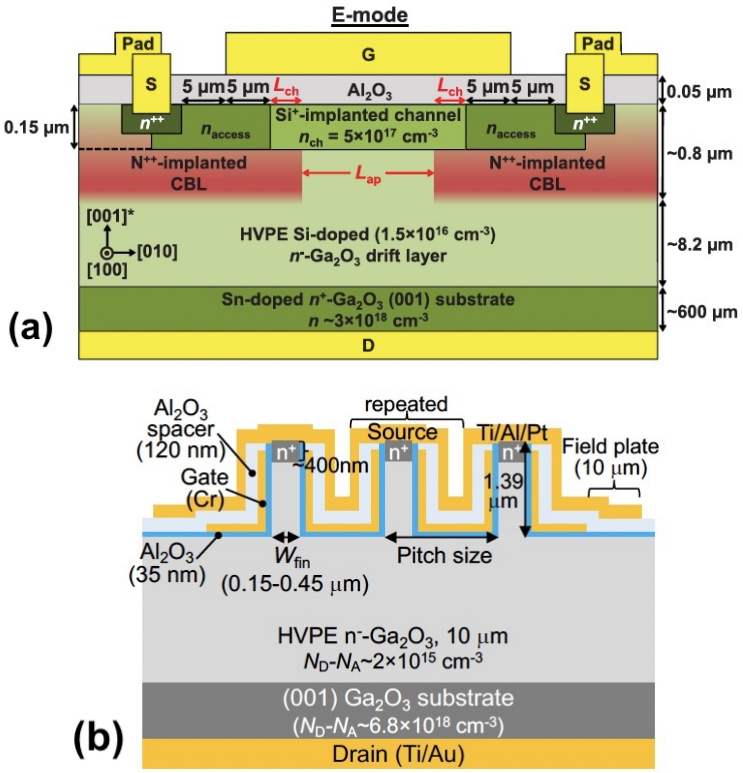


Figure 1.6: Cross-section schematics of (a) current aperture vertical MOSFETs from [4] © 2020 IEEE and (b) vertical fin MOSFETs from [5] © 2019 IEEE.

blocking layer (CBL) that electrically isolates the source and the drain contacts, except at the aperture opening in the CBL. CBLs are formed through ion implants of deep acceptor dopants; originally Magnesium ions were used, but greater success was seen with Nitrogen [34–36]. While initial devices showed depletion-mode behavior, the first enhancement-mode current aperture β-Ga_2O_3 MOSFET (shown in Figure 1.6 (a)) has been demonstrated with the help of a lower electron concentration in the channel region. Premature breakdown, though, was observed at 263 V due to leakage of the CBL [4].

Currently, the vertical fin-MOSFET, or finFET, has shown to be more promising for future β-Ga_2O_3 enhancement-mode vertical power devices. The fin device structure, which is shown in Figure 1.5 (b), adopted from the GaN finFET, allows for enhancement-mode behavior without the need of p-type doping [37]. The etched fin acts as the vertical channel for the current to flow from the top of the fin (source contact) to the bottom of the substrate (drain contact). The current is controlled by the gate voltage, which is applied to the MOS stack on both sides of the fin [23]. With a thin fin ($\sim$ 100 – 400 nm in width) the gate can successfully deplete the fin channel at 0 V. The first reported vertical β-Ga_2O_3 finFET with enhancement-mode behavior showed V_{br} of $>$1 kV [37]. More recently, a V_{br} of $>$2.6 kV was demonstrated on a multi-fin transistor with a source-connected field-plate; the cross-section schematic is shown in Figure 1.6 (b) [5]. The vertical β-Ga_2O_3 finFET has seen fast development and promising results, but the vertical gate structure on an etched surface presents new challenges for optimizing device performance.

1.4 Dielectric – β-Ga_2O_3 interface in MOS devices

A high-quality oxide-semiconductor interface is extremely important for all MOSFETs. The beautiful interface of SiO_2-Si is one of the key reasons for the advancement and superiority of Si devices. A poor interface between the gate dielectric and semiconductor can lead to large leakage currents, threshold voltage instability, and premature breakdown [38]. Before a new device can be commercialized, these reliability issues must be resolved. When developing new devices, especially

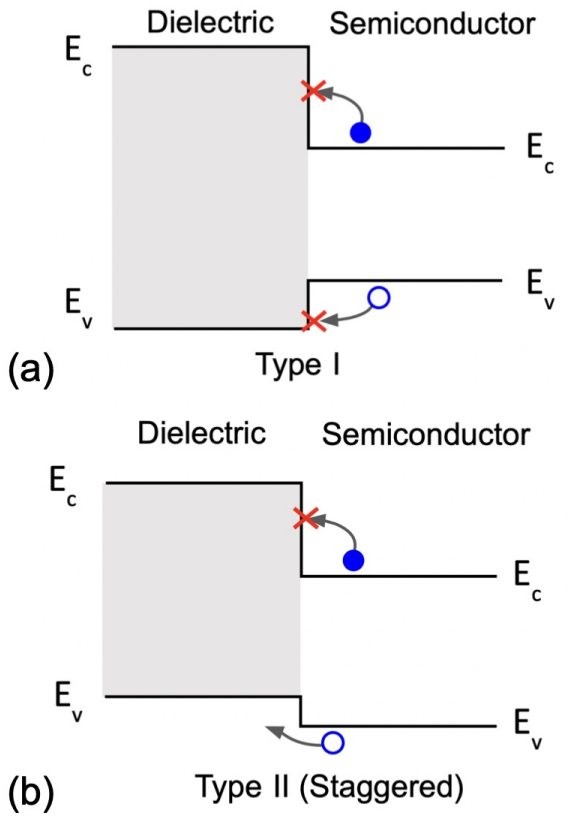


Figure 1.7: (a) Type I band alignment is ideal for impeding both electron and hole movement from the semiconductor to the dielectric. (b) Type II or staggered band alignments only impedes the flow of one type of charges, in this case electrons. This thesis will mainly focused on the type II band alignment with β-Ga_2O_3.

with new semiconductor materials, various dielectrics must be tested for their compatibility to the semiconductor. A new material, whether it is a new semiconductor or dielectric in the MOS stack, results in different interfaces band alignment and trap states. In order to achieve stable, high performing β-Ga_2O_3 MOSFETs, we must understand and optimize dielectric interfaces with β-Ga_2O_3.

There are several criteria to be considered when choosing a gate dielectric. One of the first to consider is the band alignment between the dielectric and semiconductor, which includes the conduction band offset (ΔE_C) and valence band offset (ΔE_V). Ideally, the dielectric would have a large ΔE_C and ΔE_V ($>$1 eV) to the semiconductor in order to minimize thermal leakages (type I alignment shown in Figure 1.7 (a)), but the large bandgap of β-Ga_2O_3 significantly reduces the

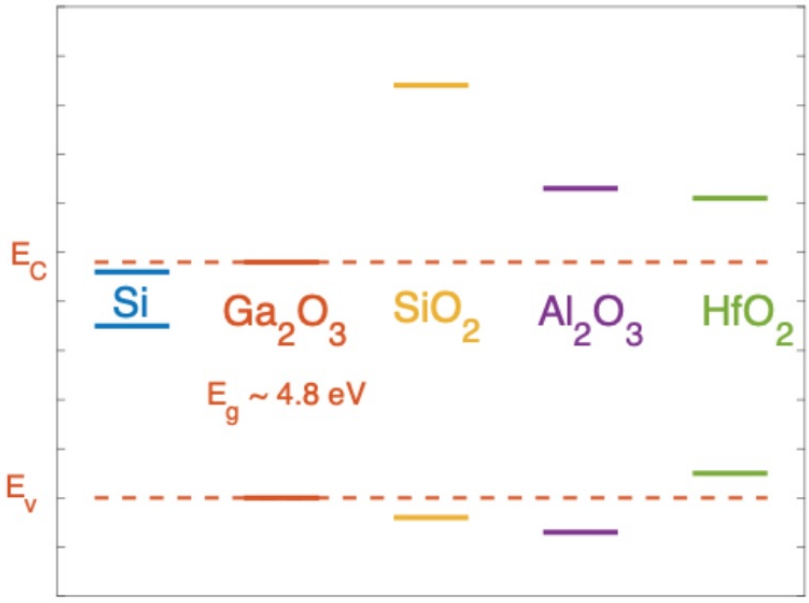


Figure 1.8: Band alignments of several dielectrics to β-Ga_2O_3 and with a comparison to Si. Y axis units are in eV, and the bandgap (E_g) of β-Ga_2O_3 is set to 4.8 eV.

choice of dielectric materials that can achieve this [13]. Figure 1.8 shows the relative conduction and valence band alignments of three frequently used dielectrics to β-Ga_2O_3: SiO_2 [39], Al_2O_3 [40], and HfO_2 [7]. Si is included in this figure to show the contrast in band offsets of dielectrics to WBG semiconductors versus to Si. The figure highlights two different types of band alignment: type I and type II (staggered). SiO_2 and Al_2O_3 both provide a type I band alignment to β-Ga_2O_3, which means they provide an electron and hole barrier for the semiconductor, as shown in Figure 1.6 (a). HfO_2, which has a type II alignment to β-Ga_2O_3, provides only an electron barrier and no hole barrier (Figure 1.7 (b)). While this is seen as a disadvantage, the lack of mobile holes in the β-Ga_2O_3 could indicate a positive ΔE_V may not be necessary.

Another important criterion when choosing a dielectric is ensuring it has a clean interface to the semiconductor; this can be measured in density of interface traps or states (D_{it}). Interface traps are defects or electrically active traps located between the semiconductor and dielectric. These traps can normally be filled and emptied relatively quickly during device operation and can lead to threshold voltage instabilities [41]. Interface traps can also degrade MOSFET performance by

lowering subthreshold swing and reducing output current. A low D_{it} indicates a clean interface, which is ideal. D_{it} can be estimated from a device's transfer curves, but several capacitance-voltage (*C-V*) techniques can be used with a metal-oxide-semiconductor capacitor (MOSCAP) to extract the distribution of interface traps without the need of a three-terminal device [41]. *C-V* D_{it} techniques, like Terman method, AC conductance method, and high-low method have been demonstrated to extract an average D_{it} for several dielectrics with β-Ga_2O_3 [7, 38, 39, 42]. The downside to these traditional D_{it} techniques is the limited range of β-Ga_2O_3 trap levels that can be detected due to the long electron emission time constants for traps at the mid-gap level and near the valence band. This limitation has led to some researchers of WBG semiconductors to supplement the D_{it} techniques with the photo-assisted *C-V* technique, which uses deep ultraviolet (DUV) illumination to excite electrons, ensuring those deeper traps will respond to the *C-V* sweep [6, 38, 43–45]. Chapter 2 will provide a review on how to extract D_{it} using Terman and AC Conductance (the traditional techniques), which will be used within this thesis. Chapter 3 explains in detail the photo-assisted *C-V* technique.

In addition to interface traps, oxide traps and especially border traps are important to investigate in relation to UWBG semiconductors. Border traps are charge traps within the dielectric located a few nanometers from the interface. These traps can also impact the performance of devices [46], and many have reported evidence of border traps within β-Ga_2O_3 MOSCAP studies [38, 44, 47, 48]. The large bandgap and lack of mobile holes (Figure 1.9) may cause border traps and interface traps to behave differently compared to other semiconductors, like Si; therefore, it is necessary to perform various analyses on traps within MOS structures on β-Ga_2O_3. Other ideal characteristics of dielectrics in power devices are high dielectric relative permittivity (κ), low leakage, high breakdown field, high temperature stability, and resistance to stress-induced charge trapping. Much of the focus for dielectrics in β-Ga_2O_3 devices has been SiO_2, Al_2O_3, HfO_2, and combinations of these dielectrics [13]. While there have been many studies of these dielectrics with planar β-Ga_2O_3 MOSCAPs, there is still much to learn about the relationship between dielectrics and the WBG semiconductor in order to optimize the MOS structure for future β-Ga_2O_3 devices.

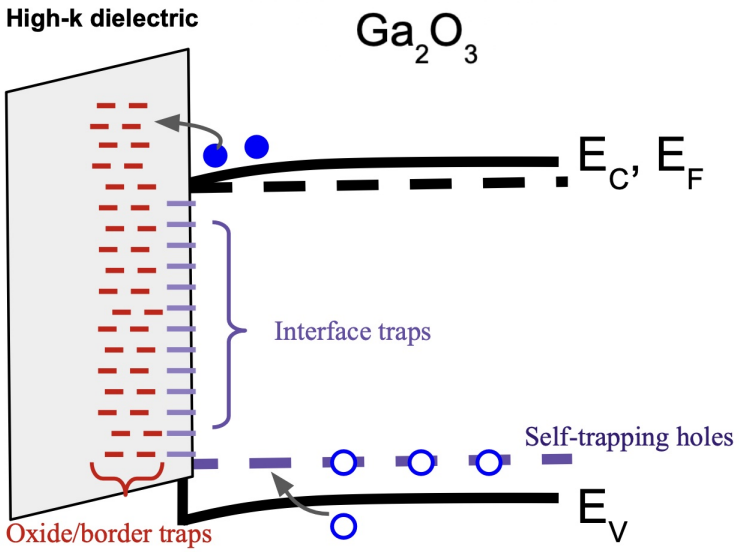


Figure 1.9: Example band alignment of β-Ga_2O_3 to a high-κ dielectric illustrating electron trapping into the dielectric and holes self-trapping within the substrate.

1.5 Thesis Objectives

β-Ga_2O_3 devices have made great progress thanks to the borrowing of many GaN technologies (e.g. epilayer growth, ohmic contacts, plasma etching, and device structures), but still many of these areas and others need significant improvements before we will see the commercialization of β-Ga_2O_3 power devices. The development of reliable, high performing β-Ga_2O_3 power MOSFETs will require an excellent dielectric interface to the UWBG semiconductor. There are many important aspects to the dielectric-β-Ga_2O_3 relationship that have not been fully investigated and understood yet. The following questions will be investigated in this thesis:

1. **What new/modified characterization techniques are needed to quantify MOS traps with the UWBG semiconductor, β-Ga_2O_3?** These techniques will be necessary to use when determining the best dielectric process, which includes pre-deposition cleaning, deposition process, and post-deposition annealing, required to create a low-defect interface to β-Ga_2O_3.

2. **How does a type II band alignment at the β-Ga_2O_3 MOS interface affect the proper-**

ties and performance of the MOS device? What role do holes play, if any? Very few dielectrics provide the ideal type I band alignment to β-Ga_2O_3; this would limit us to SiO_2, Al_2O_3, and combinations of these two, but we also know that β-Ga_2O_3 shows self-trapping hole behavior, as well as, a low hole mobility [2, 24]. Can we forgo a positive valence band offset in order to utilize a higher-κ dielectric due to these features of holes within β-Ga_2O_3?

3. **Given the known diffusion/redox issues with β-Ga_2O_3 (Ti for ohmic contacts, Al_2O_3, Mg, etc.), what dielectrics or dielectric stacks are suitable to form a stable MOS against temperature and bias stress?** Stability in the MOS structure is critical, so all dielectric-semiconductor interfaces should be tested against electrical bias stress and thermal stress. In particular with thermal stress, the interdiffusion of Al_2O_3 and β-Ga_2O_3 has been shown at elevated temperatures [11, 49]. Will the same observations be seen with HfO_2, and how would an intermixed layer impact the MOS performance?

4. **How do the above MOS properties on β-Ga_2O_3 vary when moving from a planar gate stack to a fin structure?** With the promising fin MOSFET structure, normally-off β-Ga_2O_3 vertical transistors can be realized, but sidewall defects on the etched semiconductor can be detrimental to the device [50]. The various types of reliability testing normally performed on planar MOS structure must also be performed on these etched non-planar structures.

The objective of this thesis is to investigate the trapping and emission of charges in MOS structures with the UWBG semiconductor, β-Ga_2O_3, and its effects on MOS reliability. First, I demonstrate an alternative high-κ dielectric, $(Y_{0.6}Sc_{0.4})_2O_3$, with β-Ga_2O_3 in MOSCAPs and analyze the interface quality between the solution-processed dielectric and the UWBG semiconductor. Analyzing this new MOS stack presented the opportunity to develop a vast set of techniques and analyses, which can be utilized for further dielectric - UWBG semiconductor research. The photo-assisted *C-V* technique is demonstrated to extract a distribution of interface states in the $(Y_{0.6}Sc_{0.4})_2O_3/\beta$-$Ga_2O_3$ MOSCAPs and is compared to traditional D_{it} extraction methods. Illumi-

nation and temperature-dependent current – voltage (J-V) measurements are used to examine the conduction mechanisms in both forward and reverse bias. Reverse bias photo-current is observed in the MOSCAPs indicating the excitement and movement of previously trapped holes facilitated by the deep ultraviolet illumination and negative ΔE_V between the dielectric and UWBG semiconductor. Due to the need for a conformal gate dielectric and to further investigate the effect of a negative ΔE_V, ALD HfO_2/β-Ga_2O_3 MOSCAPs are fabricated and analyzed. The reliability under positive bias stress is tested, and a comparison to HfO_2/Si MOSCAPs is made to investigate the charge trapping differences between the UWBG semiconductor and Si MOS stacks. Along with electrical stability under stress, the thermal stability of the HfO_2 interface to β-Ga_2O_3 is investigated. I used several material and electrical characterization techniques to study the impact of high temperature annealing processes (between temperatures of 500°C to 900°C) on the ALD HfO_2 layer and its interface to β-Ga_2O_3. The impacts that will be discussed include Ga-diffusion into HfO_2, HfO_2 crystallization, current leakage and interface traps. Lastly, the focus shifts from planar β-G a_2O_3 MOS structures to vertical MOS structures on etched β-Ga_2O_3. I develop a fabrication process for HfO_2/β-Ga_2O_3 fin MOSCAPs in order to investigate the dielectric interface quality on the sidewalls of etched β-Ga_2O_3. The fin MOSCAPs are tested in a similar fashion to the planar MOSCAPs to achieve an understanding of the sidewall traps and how these traps vary from planar MOS structures. Due to the importance of the MOS structure, the results from this thesis will support the development of high-performing, stable β-Ga_2O_3 power MOSFETs.

1.6 Thesis Overview

In Chapter 2, we will review MOSCAP basics and various C-V and J-V measurement techniques. In Chapter 3, we investigate a novel, solution-processed, dielectric, $(Y_{0.6}Sc_{0.4})_2O_3$, for its compatibility with β-Ga_2O_3 through the fabrication and electrical testing of MOSCAPs. Initially, the interface quality of $(Y_{0.6}Sc_{0.4})_2O_3$ and β-Ga_2O_3 is analyzed through multiple interface trap density (D_{it}) extraction methods including the photo-assisted C-V method. A low total D_{it}

charge of $< 1 \times 10^{12}$ cm^{-2} is extracted which indicates a clean interface between the dielectric and semiconductor. The $(Y_{0.6}Sc_{0.4})_2O_3$/β-Ga_2O_3 MOSCAPs are then analyzed with several *J-V* techniques to identify the conduction mechanisms in the MOSCAPs. Hole generation in β-Ga_2O_3 with the help of illumination and thermal leakage studies will also be discussed . In Chapter 4, we shift our focus to HfO_2/β-Ga_2O_3 MOSCAPs partially due to the ability to deposit the dielectric through atomic layer deposition (ALD). Positive bias stress testing is performed on these MOSCAPs and compared to HfO_2/Si MOSCAPs to better understand the role of the WBG semiconductor in charge trapping at the dielectric interface. Border traps within the HfO_2 dielectric will be discussed as significant flatband voltage shifting is observed in fresh MOSCAPs with repeated *C-V* sweeps. Lastly, the impact of the type-II band alignment between HfO_2 and β-Ga_2O_3 is considered as it may help enable photo-current in depletion, as well as expedite recovery from stress-induced charge trapping with illumination. In Chapter 5, I investigate the temperature reliability of the HfO_2/β-Ga_2O_3 interface. The results from secondary ion mass spectrometry (SIMS) depth profile and electrical measurements of MOSCAPs are compared to understand the impact of high temperature annealing processes on this dielectric and its interface to the UWBG semiconductor. In Chapter 6, I demonstrate fin MOSCAPs as a method of investigating the dielectric interfaces with etched β-Ga_2O_3. Previously demonstrated *C-V* techniques are used to analyze the sidewall traps caused by the plasma etching process. The initial conclusions from this study will be discussed, as well as, the various questions that still need to be investigated. I will suggest some future steps for optimizing the fin MOSCAP structure; creating more reliable fin MOSCAPs will be necessary to answer these remaining questions on β-Ga_2O_3 sidewall traps. This thesis concludes with Chapter 7, reviewing the contributions of this work and suggesting future research endeavors, which would further explore and improve the state of gate dielectrics for β-Ga_2O_3 power MOS devices.

CHAPTER 2

Methods of Dielectric - Semiconductor Interface Analysis

The goals of this thesis require the use of many capacitance - voltage (C-V) and current density - voltage (J-V) techniques for analyzing the dielectric - wide bandgap (WBG) semiconductor interfaces. This chapter is included to provide a review of various capacitance - voltage (C-V) and current density - voltage (J-V) methods used with metal-oxide-semiconductor capacitors (MOSCAPs) to analyze the MOS structure. This review will assume the semiconductor is n-type, due to the n-type nature of β-Ga_2O_3.

2.1 Basic capacitance – voltage measurements

At the core of all MOSFETs is the MOS stack, which acts as the gate or switch to these devices; this structure significantly influences the device performance and can provide great insight into the semiconductor surface. The MOSCAP structure, which is used throughout this thesis, is illustrated in Figure 2.1. On top of the semiconductor is the blanket insulator (or dielectric) film and a patterned metal contact, which forms the anode. On the backside of the semiconductor is a blanket metal film, which forms an ohmic contact (linear J-V relationship) with the semiconductor and is called the cathode. Included in the illustration (Figure 2.1.) is details of how we probe these MOSCAPs. Due to the cathode backside contact, we place the sample on a gold-coated glass slide and probe the glass slide with the low or grounded potential/current probe. Then the high

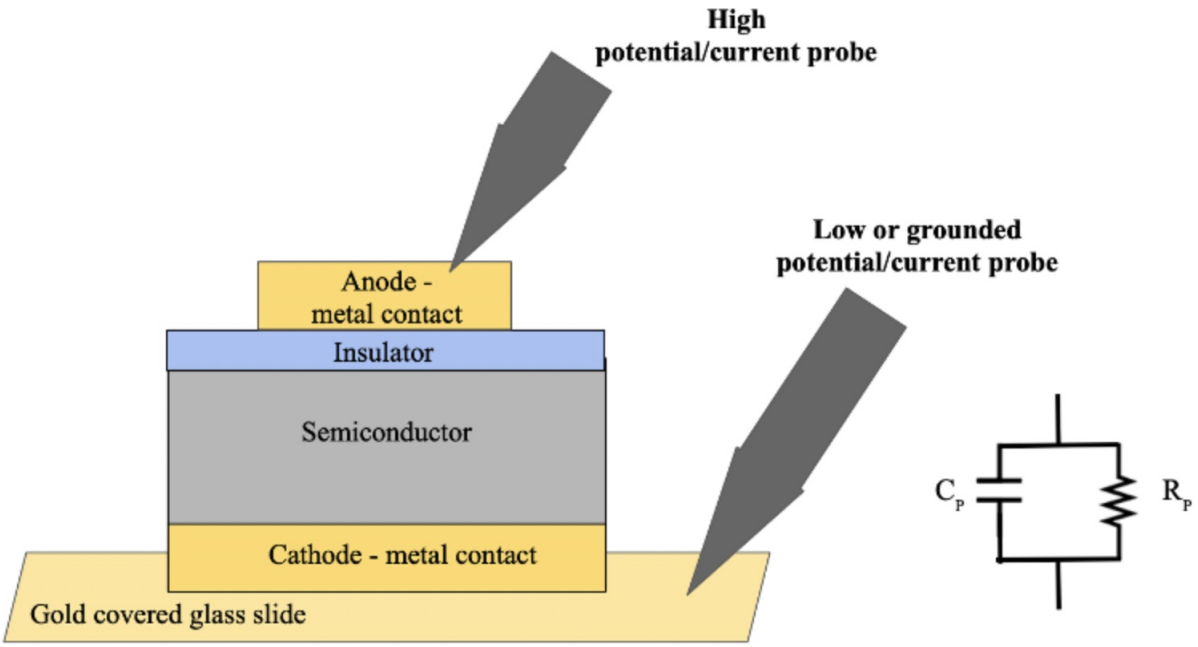


Figure 2.1: Cross-section diagram of a MOSCAP structure with added details of the probes. The diagram to the right shows the circuit model (C_P-R_P) used throughout this work.

potential/current probe is landed on the anode metal contact; the pressure from the landed probe on the MOSCAP ensures a good contact between the cathode and the gold-coated slide.

Capacitance is the change in charge due to a change of voltage (dQ/dV) and is given in units of farad/unit area (F/cm^2) [41]. For this work, the C-V curves are measured with a HP4284A LCR meter. A small-signal ac voltage, in this case with an amplitude of 50 mV, is applied to the MOSCAP, and capacitance is recorded while sweeping a dc voltage bias. In this work the capacitance results come from the circuit model of parallel capacitance – parallel resistance (C_P-R_P); a diagram of the circuit model is shown in Figure 2.1.

A typical C-V curve for a n-type MOSCAP is shown in Figure 2.2 (a). Unless it is otherwise specified, these measurements are being performed in the dark at a high frequency of 1 MHz, and the dc voltage bias (applied to the anode) is being swept from a negative voltage bias to positive. There are three regions of the C-V curve, which are labeled in Figure 2.2 (a): depletion, flatband, and accumulation. Figure 2.3 (a)-(c) show the corresponding energy band diagram of these regions. At a -V applied to the anode, the bands are bent down to cause any electrons in the conduction band (E_C)

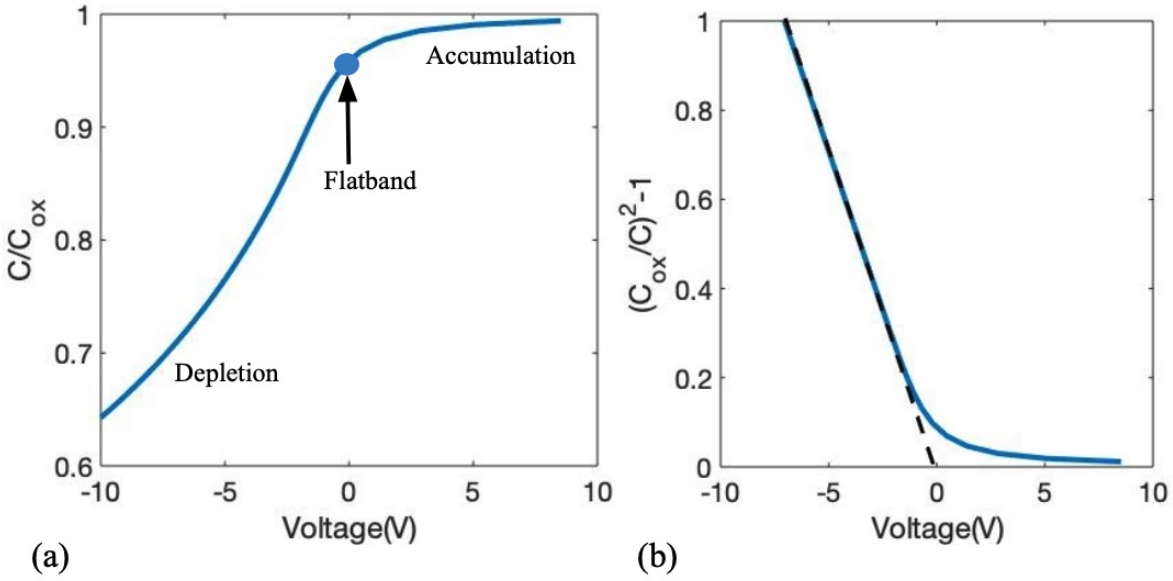


Figure 2.2: (a) Typical *C-V* curve of a n-type MOSCAP. The three regions of the curve are labeled in the graph: depletion, flatband, accumulation. (b) $(C_{ox}/C)^2$-1 versus *V* data, which the V_{fb} can be extracted from.

at the insulator-semiconductor interface to move away from the interface; this is called depletion (Figure 2.3 (a)). In this depletion region, the doping concentration (N_d) of the semiconductor can be extracted using the slope of the measured $1/C^2$ data. N_d is calculated by the following equation,

$$N_d = \frac{-2}{q\varepsilon_0\varepsilon_s \frac{d(1/C^2)}{dV}}, \tag{2.1}$$

where q, ε_o, and ε_s are the electron charge, vacuum permittivity, and the semiconductor permittivity.

As the voltage bias is swept in the positive direction, the band bending will ease, and at a specific voltage bias called flatband voltage (V_{fb}), the energy bands will be flat, as shown in Figure 2.3(b) [3]. This is determined by the metal-semiconductor work function differences and charges in the dielectric and at the interface; ideally, V_{fb} will be around 0 V [41]. The V_{fb} can be extracted from the *C-V* curve by taking the x-intercept of the extrapolated line of $(C_{ox}/C)^2 - 1$ [44], shown in Figure 2.2 (b). As the voltage bias continues to increase, the MOSCAP will move into the accumulation region, which bends the energy bands in the semiconductor upward and causes

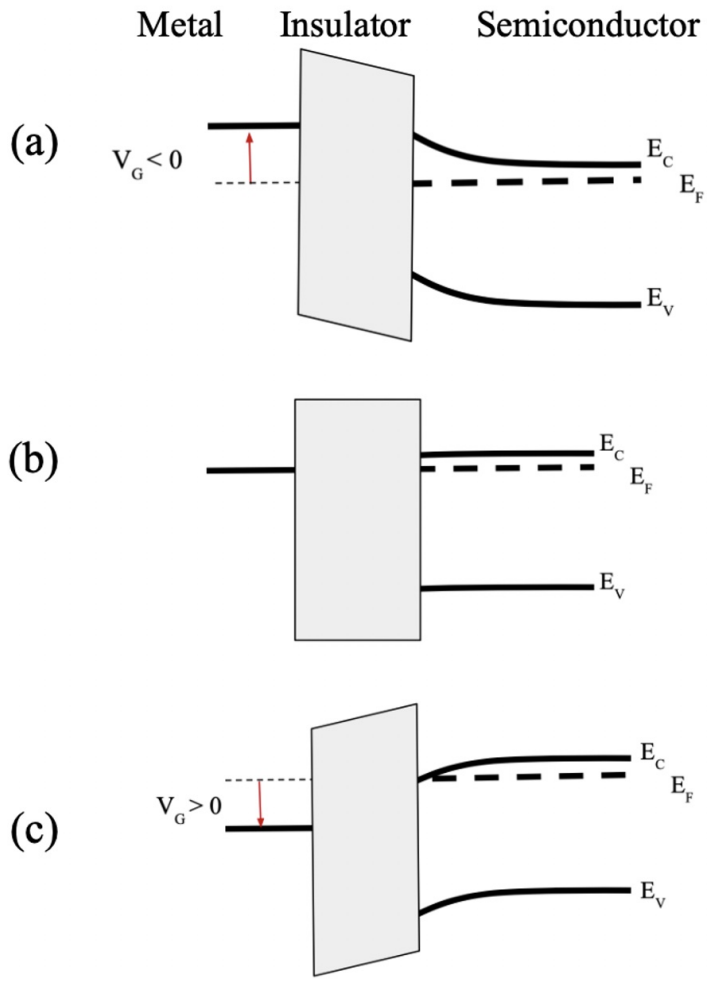


Figure 2.3: Energy band diagrams of n-type MOS structure: (a) depletion, (b) flatband, and (c) accumulation.

electrons to accumulate at the interface (Figure 2.3(c)). In this region the capacitance saturates to the oxide capacitance (C_{ox}), which is determine by the insulator or dielectric characteristics. C_{ox} is defined by the following equation,

$$C_{ox} = \frac{\varepsilon_{ox} * \varepsilon_o}{t_{ox}}, \tag{2.2}$$

where ε_{ox} and t_{ox} are the dielectric permittivity and the thickness of the dielectric or insulator layer. In some cases, ε_{ox} may be noted as κ; ideally, a dielectric would have a high dielectric permittivity (also known as a high-κ dielectric), which would allow thicker dielectric layers to achieve the same C_{ox} [3].

2.2 MOS traps with *C-V* techniques

2.2.1 MOS traps

C-V measurements are extremely useful to investigate the type and quantity of traps or defects within the MOS structure. As explained in Chapter 1, these traps can greatly affect MOSFET device performance and stability. There are three types of traps we will discuss throughout this work: oxide traps, border traps, and interface traps. Figure 2.4 provides an illustration of where these traps are located within the MOS stack. Oxide traps, which can be further separated into fixed oxide traps, mobile oxide traps, and oxide trapped charges, are defects within the dielectric layer. These traps can provide pathways for leakage and affects the threshold voltage. Usually, these traps are not changing occupancy during standard device operation. We can observe the effect of oxide traps within *C-V* curves through flatband voltage shifts (V_{fb}). Figure 2.5 shows when including oxide traps, the shape of the *C-V* curve remains the same but is now shifted to the right. The quantity of the traps (N_{ox}) can be calculated by the following equation,

$$N_{ox} = \frac{|\phi_{ms} - V_{fb}| \times C_{ox}}{q}, \tag{2.3}$$

where ϕ_{ms} is the metal-semiconductor work function difference. A shift to the right (+V_{fb}) indicates a net negative oxide charge (electrons), and a shift to the left (-V_{fb}) indicates a net positive oxide charge (holes) [30].

Border traps are a type of oxide trap that are located within a few nanometers away from the dielectric-semiconductor interface (shown in figure 2.4). Other names for these traps include 'slow states' and 'near-interfacial traps' [51]. Due to their proximity to the interface, these traps can be more easily filled and emptied during device operation. These traps affect the *C-V* curves in a similar way as other oxide traps resulting in a V_{fb}. Border traps have been observed in β-Ga_2O_3 MOSCAPs with shifting *C-V* curves with repeated *C-V* sweeps [38, 47, 48]. The quantity of border

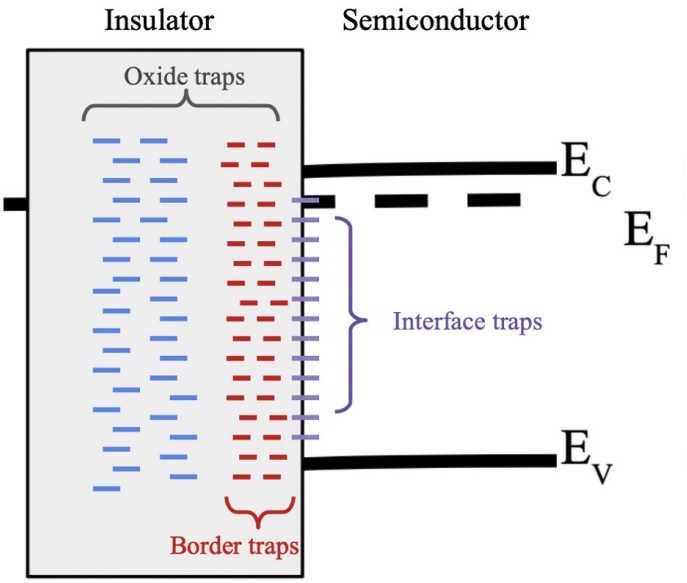


Figure 2.4: Energy band diagram of the insulator-semiconductor stack showing oxide, border, and interface traps.

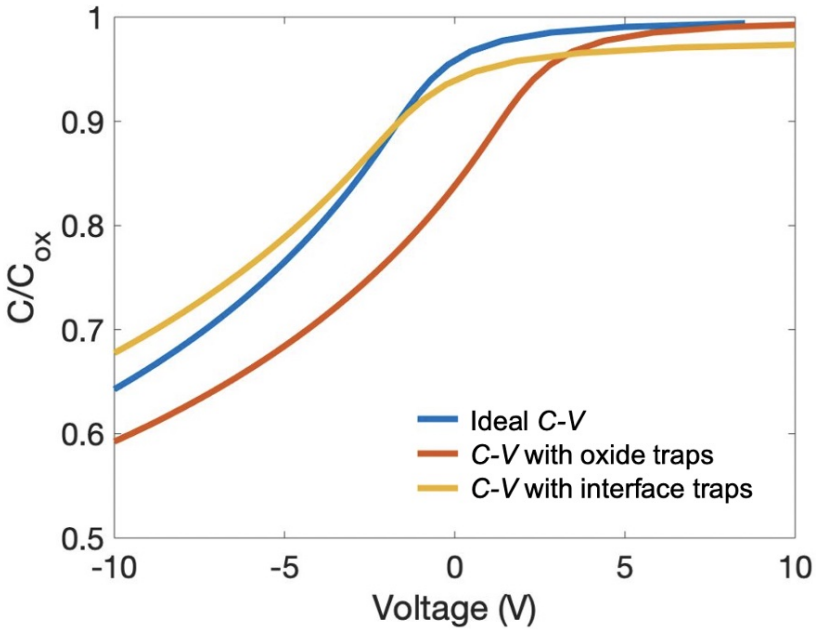


Figure 2.5: Example of *C-V* curves showing the effects of oxide traps and interface traps.

traps (N_{bt}) can be calculated with the following equation,

$$N_{bt} = \frac{\Delta V_{fb} \times C_{ox}}{q}. \tag{2.4}$$

Interface traps are located at the dielectric-semiconductor interface (Figure 2.4), which are caused by dangling bonds at this interface possibly due to metal impurities and/or structural defects. These traps are sometimes called 'fast traps'; like this name suggests, these traps can be rapidly filled and emptied causing significant effects on MOSFETs. In MOSCAPs, interface traps show themselves through the 'stretch-out' of the *C-V* curve, as shown in Figure 2.5. As the MOSCAP is swept from depletion to accumulation, interface traps change occupancy causing changes in the charge at the interface. In MOSFETs, we can observe an increase in subthreshold swing with an increase of interface traps; interface traps also cause threshold voltage instability in MOSFETs [51]. When developing MOS structures, it is crucial to estimate and minimize the amount of interface traps.

2.2.2 Interface trap density extraction techniques

There are several *C-V* techniques, developed for Si MOSCAPs, frequently used to extract a density of interface traps (D_{it}). The Terman method is a room temperature, high frequency (HF) *C-V* method that compares the experimental HF *C-V* curve to an ideal *C-V* curve. Interface traps will not respond to the ac frequency but will respond to the slow dc voltage sweep causing the 'stretch out' of the *C-V* curve as shown in Figure 2.5. D_{it}, which the units are in $\text{cm}^{-2}\text{eV}^{-1}$, can be calculated with the following equation,

$$D_{it}(\psi_s) = \frac{C_{ox}}{q}\Big(\frac{d\Delta V}{d\psi_s}\Big), \tag{2.5}$$

where ΔV is the change in voltage between the ideal and experimental *C-V* data, and ψ_s is the surface potential in the semiconductor. ψ_s can be calculated from,

$$\psi_s = \frac{q\varepsilon_s\varepsilon_0 N_d}{2C_{sc}^2}, \tag{2.6}$$

where C_{sc} is a semiconductor capacitance and can be calculated from $C_{sc} = (C \times C_{ox})/(C_{ox} - C)$ [41]. This technique will be used in this thesis and have been used by other researchers on β-Ga_2O_3 MOSCAPs [7], [52], [39]. Another *C-V* method similar to the Terman method is the high-low or quasi-static technique. This technique compared a HF *C-V* curve to a low frequency curve, where the interface traps will contribute to the overall capacitance in depletion due to the low frequency. This technique has been demonstrated with β-Ga_2O_3 MOSCAPs in [38] and [42], but currently has not been used during the work of this thesis.

The AC conductance method is another frequently used D_{it} measurement method, that is calculated from the conductance of the MOSCAP, which represents the loss due to the capture and emission of charges in the traps within a few kT/q of the Fermi level. The normalize conductance can be determined by the following equation,

$$\frac{G_p}{\omega} = \frac{qD_{it}}{2\omega\tau_{it}} ln[1 + (\omega\tau_{it})^2] \tag{2.7}$$

where D_{it} is the density of interface traps at that energy location within the semiconductor bandgap, ω is the frequency, and τ_{it} is the interface trap time constant given by the product of R_{it} and C_{it}. Figure 2.6(a) shows the equivalent circuit for the AC conductance method, with the simplified circuit shown in Figure 2.6(b) [41]. A frequency sweep of the measured parallel capacitance (C_m) and parallel conductance (G_m) data should be collected for multiple voltage biases (Figure 2.6 (c)). The resulting data (Figure 2.6 (c)) can be converted to the circuit model in Figure 2.6 (b) using the following equation,

$$\frac{G_p}{A\omega} = \frac{\omega G_m {C_{ox}}^2}{A(G_m^2 + \omega^2(C_{ox} - C_m)^2)}, \tag{2.8}$$

where A is the area of the MOSCAP. The resulting $G_p/A\omega$ versus ω data will show peaks at various frequency values; an example of this is shown on HfO_2/β-Ga_2O_3 fin MOSCAPs from Chapter 6. D_{it} is then calculated from the maximum $G_p/A\omega$ value for each voltage bias using the relation [41]

$$D_{it} = \frac{2.5}{q} \times max\Big(\frac{G_p}{A\omega}\Big). \tag{2.9}$$

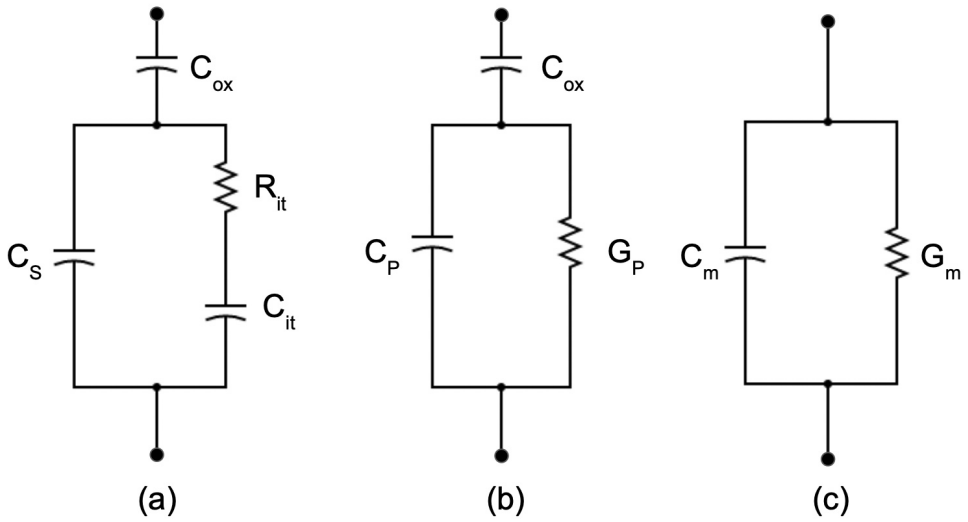


Figure 2.6: Equivalent circuits for conductance measurements; (a) MOSCAP with interface states, (b) simplified circuit of (a), and (c) the measured circuit.

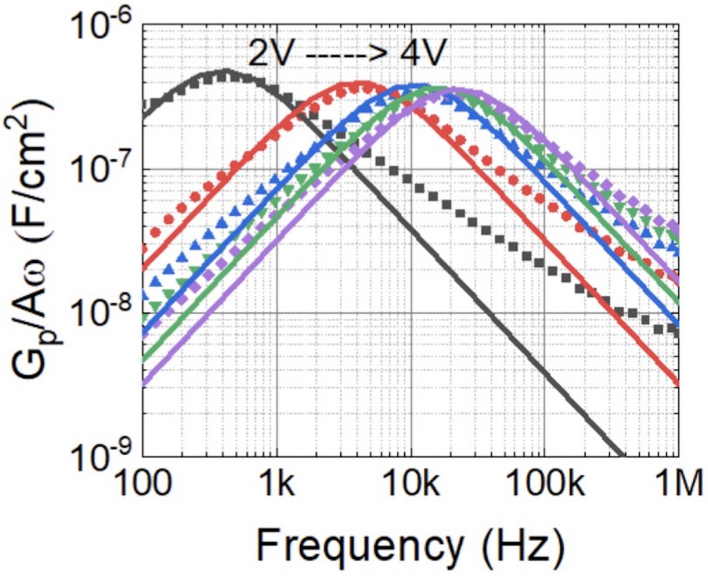


Figure 2.7: Examples of $G_p/A\omega$ versus frequency data from the AC conductance method performed on [001]-oriented HfO_2/β-Ga_2O_3 fin MOSCAPs from Chapter 6. Experimental data are the symbols and lines show the fitting to equation 2.7.

2.3 Current density – voltage measurements

In addition to *C-V*, *J-V* measurements are useful to ensure a reliable MOS structure. The dielectric needs to provide a good barrier to current leakage. With *J-V* measurements we can better understand the leakage mechanisms and the limitations of the MOS structure (i.e. breakdown electric field, E_{br}). For *J-V* data collection, the MOSCAPs are probed using the same setup as shown in Figure 2.1. A voltage bias is applied to the anode, while the current from the anode is recorded. The probe connected to the cathode is grounded. Voltage sweeps start at 0 V bias and are increased or decreased to a specified voltage. In this thesis, *J-V* measurements were taken with an HP4156A semiconductor parameter analyzer using continuous measurements with a long integration time and usually in the dark at room temperature. Ideally, we would see very low leakage current in both forward bias (+*V*) and reverse bias (-*V*) for the MOSCAPs, but defects within the dielectric can cause the leakage to increase. An example of *J-V* data from this work on β-Ga_2O_3 MOSCAPs is shown in Figure 2.8 (a) and (b). Figure 2.8 (b) also includes breakdown of the MOSCAP, which is indicated by the current reaching compliance. E_{br} is determined by the breakdown voltage (V_{br}) divided by t_{ox}. In some instances, throughout this thesis, illumination or varying temperature environments have been used when collect *J-V* data. The illumination setup will be explained in detail in Chapter 3. Temperature-dependent *J-V* measurements have been demonstrated to determine the leakage mechanisms in β-Ga_2O_3 MOSCAPs and to extract the barrier height of the dielectric to semiconductor [7], [8]. In this work, temperature-dependent *J-V* measurements were performed in a Lake Shore Cryotronics TTPX probe station. The samples are probed in a similar fashion to Figure 2.1, but under vacuum. The temperature is controlled with a Model 336 Temperature Controller and is recorded throughout the measurements. The sample can be cooled down to the 4 K or 77 K depending on if liquid He or liquid N_2 is used with the system. This technique is demonstrated in Chapter 3.

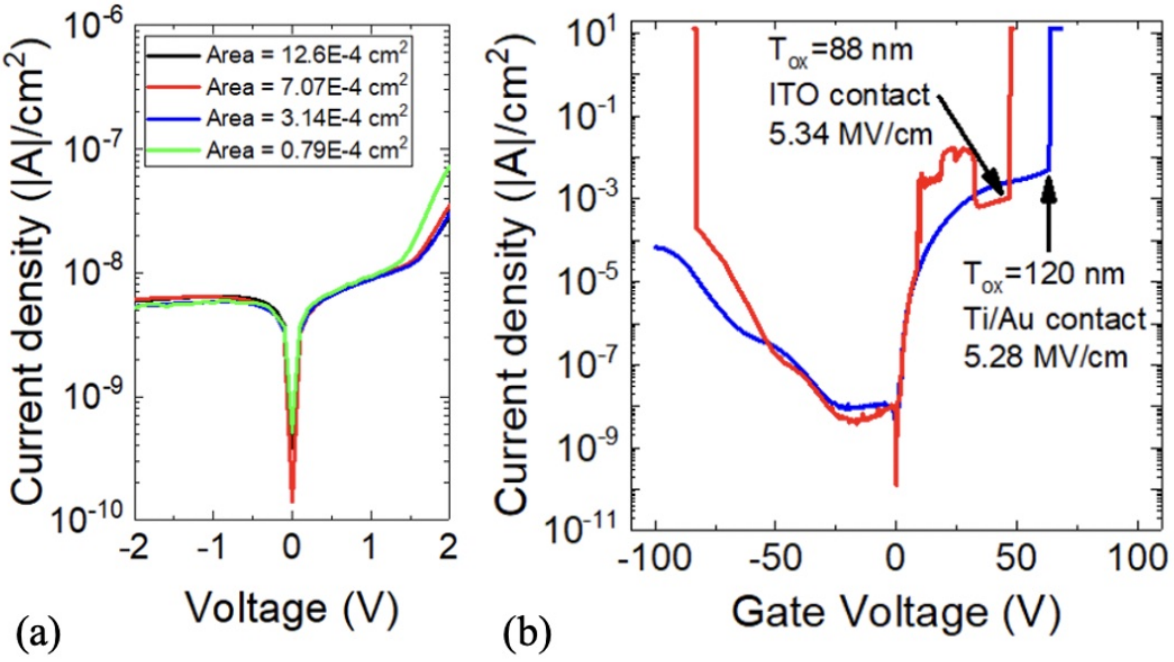


Figure 2.8: Example of *J-V* measurements of $(Y_{0.6}Sc_{0.4})_2O_3/\beta$-$Ga_2O_3$ (010) MOSCAPs of various sizes at low voltages. (b) *J-V* at high fields, including breakdown. Reprinted with permission from [6].

2.4 Conclusion

In this chapter, general MOSCAP knowledge and various *C-V* and *J-V* measurement techniques were reviewed. These techniques will be utilized throughout the thesis to investigate the various β-Ga_2O_3 MOS structures. Other techniques that are used, which are unique to wide bandgap semiconductors, will be explained in future chapters.

CHAPTER 3

Ternary Alloy Rare-Earth Scandate as Dielectric for β-Ga_2O_3 MOS Structures

3.1 Introduction

Great progress has been made in the development of β-Ga_2O_3 MOSFETs, but optimal gate dielectric materials have not yet been clearly identified. Currently, Al_2O_3, SiO_2, and HfO_2 have been the primary gate dielectrics reported for β-Ga_2O_3 MOSFETs [13], while a few additional dielectrics have been studied in the form of β-Ga_2O_3 metal-oxide-semiconductor capacitors (MOSCAPs) including ZrO_2, Al_2O_3/HfO_2 alloys and Al_2O_3/HfO_2 bilayer stacks [9, 53, 54]. Further investigation on dielectric materials for β-Ga_2O_3 devices is needed to realize the material's full potential.

An excellent dielectric-semiconductor interface is crucial for optimizing a MOSFET's performance, and this can be achieved with a large conduction band offset (ΔE_C) and a low interface trap density (D_{it}). A large ΔE_C is ideal for minimizing the thermal leakage in the device [55]. The large bandgap of β-Ga_2O_3 limits the number of dielectrics that fit this criterion, which is why much of the focus has been on SiO_2 and Al_2O_3 [13]. A low D_{it} indicates a clean interface between the dielectric and the semiconductor, minimizing electrically active traps that can severely degrade MOSFET performance. Such interface traps cause threshold voltage variation, lower sub-threshold swing, and lower output current; therefore, D_{it} should be as low as possible [38, 42].

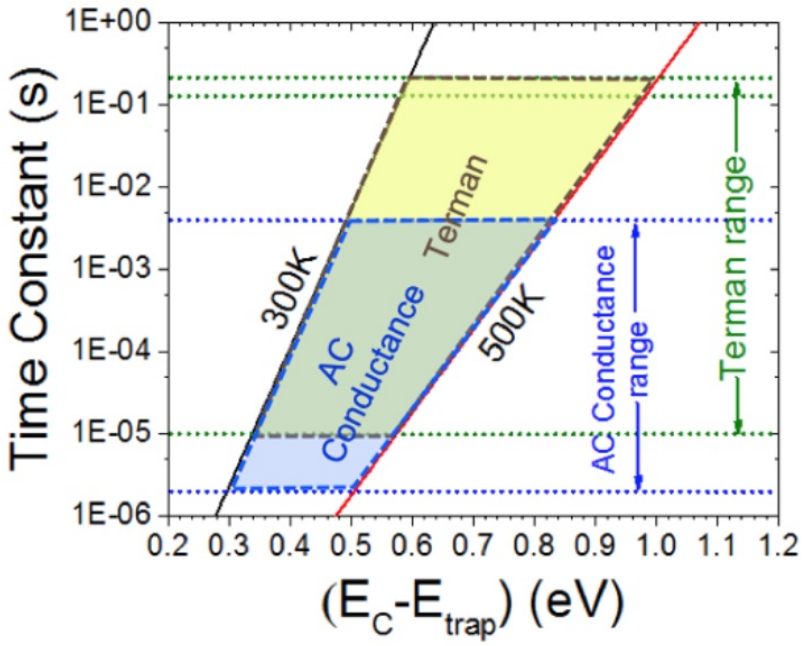


Figure 3.1: Electron emission time constant vs distance of trap level to conduction band for Terman and AC conductance methods.

3.1.1 Need for improved interface trap extraction techniques

D_{it} can be extracted using several techniques with capacitance-voltage (C-V) measurements of MOSCAPs. Standard D_{it} extraction techniques, including Terman method and AC conductance method, have been used to characterize SiO_2 and HfO_2 with β-Ga_2O_3 [39], [7]. These techniques alone, however, are insufficient for characterizing the distribution of the interface traps throughout the bandgap of β-Ga_2O_3 due to the long electron emission time constants of traps near the valence band [42], [56]. The frequency and temperature ranges normally used for these techniques, combined with the large bandgap of β-Ga_2O_3, only allow these techniques to accurately detect traps close to the conduction band. Figure 3.1 shows the interface trap level limits for the Terman and AC conductance method from 300K to 500K. While sufficient for Silicon MOSCAPs, these techniques could only access $\sim$1/5th of 4.5-4.9 eV bandgap of β-Ga_2O_3 with the help of elevated temperatures.

The photo-assisted C-V technique has been demonstrated as an alternative D_{it} extraction method for wide-bandgap semiconductors including β-Ga_2O_3 [6, 38, 43–45, 57]. This technique

uses deep ultraviolet (DUV) illumination during a depletion bias to ensure all traps can be extracted from the *C-V* sweeps. Illumination helps to empty the interface traps, resulting in a flatband voltage shift (V_{fb}) between the *C-V* curves taken before and after illumination [43]. V_{fb} can then be used to extract a distribution of interface states along a wider energy level range compared to the traditional methods. This same technique has been demonstrated on Si_3N_4/GaN MOSCAPs [43].

3.1.2 Motivation for ternary scandate-based dielectric

Several other factors outside of ΔE_C and D_{it} also need to be considered when choosing a dielectric for β-Ga_2O_3 power MOSFETs including low leakage, high breakdown field, environmental stability and high crystallization temperature. Scandate-based oxides are particularly interesting because of their non-hygroscopic behavior. Binary Y_2O_3 and Sc_2O_3, despite having smaller bandgap and lower relative permittivity than other high-κ dielectrics such as HfO_2, have successfully been used as a MOSFET gate dielectric with ZnO, ZnSnO, and GaN [58–60]. Ternary alloy dielectrics offer the potential to engineer the bandgap and dielectric constant, while also showing higher crystallization temperatures in comparison to many binary oxides due to inhibited crystallization. The PetersonLab Group had previously developed a solution-deposition method to achieve $(Y_{0.6}Sc_{0.4})_2O_3$ films with low leakage current, a high relative dielectric constant (κ) of 9.6, a large breakdown field of 4.0 MV·cm^{-1}, and a crystallization temperature of $>$600°C. The ternary films also showed lower leakage after crystallizing compared to crystallized binary Y_2O_3 and Sc_2O_3 films [61].

Due to the dielectric's beneficial properties, I investigated the potential of the solution-processed $(Y_{0.6}Sc_{0.4})_2O_3$ dielectric for future β-Ga_2O_3 MOS structures. In the beginning of this chapter, I describe our fabrication process of $(Y_{0.6}Sc_{0.4})_2O_3$/β-Ga_2O_3 (010) MOSCAPs, as well as, our process for extracting D_{it} using the photo-assisted *C-V* method. The analysis of the interface quality of $(Y_{0.6}Sc_{0.4})_2O_3$ with β-Ga_2O_3 shows this dielectric has promise as a good gate dielectric, but more importantly, indicates the usefulness of the photo-assisted *C-V* method for extracting a more thorough D_{it} energy distribution. This method will be used in later chapters. $(Y_{0.6}Sc_{0.4})_2O_3$/β-

Ga_2O_3 (010) MOSCAPs were further analyzed using multiple current density - voltage (*J-V*) studies. The unexpected differences between forward and reverse bias leakage led to the investigation of the current mechanisms using illuminated *J-V* and temperature-dependent *J-V* measurements. These results encouraged more investigations in dielectrics with type II band alignment with β-Ga_2O_3.

3.2 Experimental section

3.2.1 MOSCAP fabrication

$(Y_{0.6}Sc_{0.4})_2O_3$/β-Ga_2O_3 MOSCAPs were fabricated using Sn-doped β-Ga_2O_3 (010) substrates from Tamura Corporation. This crystal orientation was selected because the [010] direction shows the highest thermal conductivity reported for β-Ga_2O_3 of 0.27 W/(cm*K) [62]. The substrates were diced and cleaned before dielectric deposition. Cleaning included solvent cleaning followed by a 10-minute piranha etch (98% H_2SO_4: 30% H_2O_2=1:1), and a 1-minute buffered HF dip. The $(Y_{0.6}Sc_{0.4})_2O_3$ films were formed following the same recipe as previously reported [61]. A 0.5 M solution was filtered and spin-coated on the β-Ga_2O_3 piece inside a moisture-controlled glovebox at 3000 rpm for 40 s [63]. The sample was placed on a hotplate inside a heat box within the glovebox at 520°C for one minute to dry. A second layer of the solution was spin-coated on the sample, and a final one hour anneal was performed at 520°C. The temperature and relative humidity within the glovebox were 21°C and 32% during the spin coating process, and 35°C and 11% during the annealing steps. The final thickness of the $(Y_{0.6}Sc_{0.4})_2O_3$ film was 88 nm measured with a J A Woollam M-2000 Ellipsometer. Thinner $(Y_{0.6}Sc_{0.4})_2O_3$ films ($<$20 nm) were formed on silicon by lowing the molarity of the solution to 0.05 M, but were not used for the studies described herein.

After dielectric deposition, the metal contacts of the MOSCAPs were formed. First, the backside contact was formed with a 5-minute ion mill etch before depositing Ti/Au (20 nm / 230 nm) by electron beam evaporation. Top contacts were created by sputtering 100 nm of indium tin oxide (ITO) and patterned with photolithography and lift-off. At the end of the fabrication process, a one-minute N_2 anneal at 470°C was performed to make the backside contact more ohmic [27],

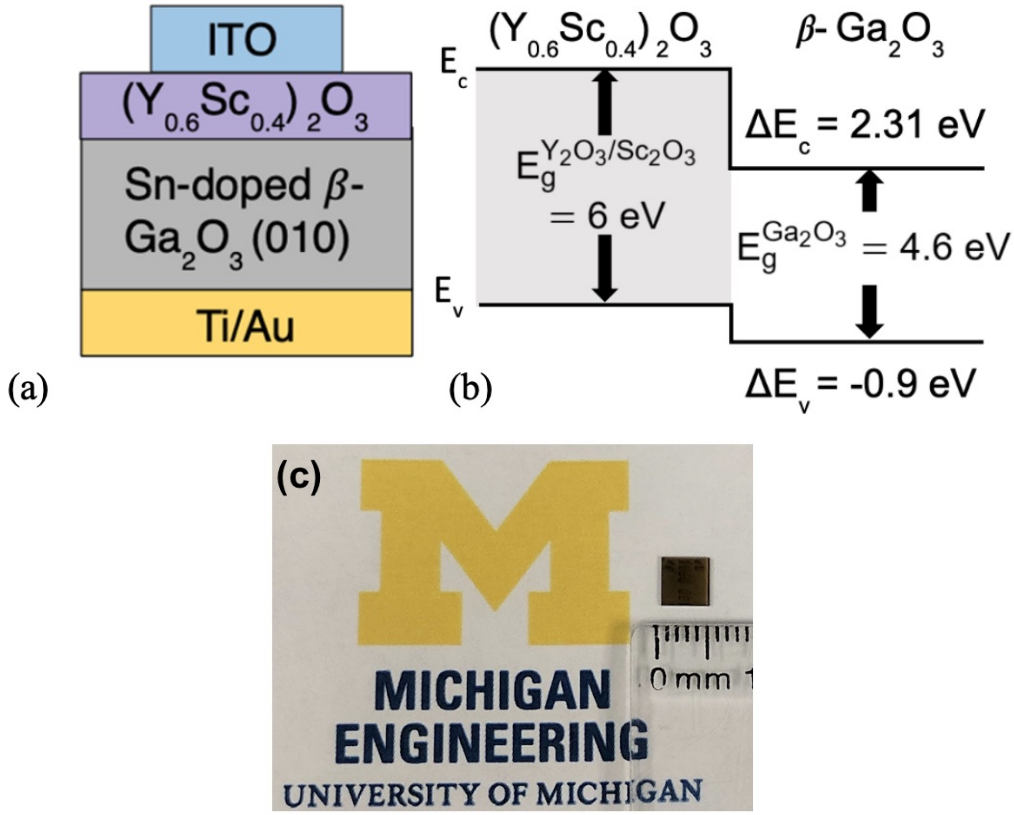


Figure 3.2: (a) Cross-sectional diagram of final MOSCAP structure, (b) energy band alignment of $(Y_{0.6}Sc_{0.4})_2O_3$ to β-Ga_2O_3 under flatband conditions, and (c) photograph of final 5 by 5 mm MOSCAP sample

and a five-minute forming gas anneal at 450°C was used to lower the contact resistance of the ITO [64]. ITO was chosen for the top contacts due to its optical transparency. The cross-sectional diagram of the final MOSCAP structure is shown in Figure 3.2 (a) and a photograph of the finish sample is shown in Figure 3.2 (c). The energy band lineup is shown in Figure 3.2 (b) under flatband conditions. Calculations, based on the electron affinities of β-Ga_2O_3[56] and Si and the ΔE_C of Y_2O_3 and Sc_2O_3 to Si [65], give a ΔE_C of 2.31 eV and a valence band offset (ΔE_V) of -0.9 eV to β-Ga_2O_3. A negative ΔE_V has also been observed in the band alignments of HfO_2 and ZrO_2 to β-Ga_2O_3 [9].

3.2.2 Measurement methods

All capacitance measurements were taken with an HP4284A LCR meter. Capacitance-Voltage (*C*-*V*) sweeps were performed in the dark at 1 MHz, sweeping from depletion (-*V*) to accumulation (+*V*) with the sweep rate of 0.5 V$\times$s^{-1}. A donor doping density, N_d, of 1.7 $\times$ 10^{18} cm^{-3} was extracted from the experimental *C*-*V* curve. Relative permittivity values, κ, of 8.3 to 8.5 were obtained for $(Y_{0.6}Sc_{0.4})_2O_3$ from the experimental data, which are similar to the value previously reported [61]. Current-voltage (*J*-*V*) measurements were taken with an HP4156A semiconductor parameter analyzer in the dark at room temperature. Temperature-dependent *J*-*V* measurements were performed in a Lake Shore Cryotronics TTPX probe station.

In our photo-assisted *C*-*V* setup, a 265 nm light-emitting diode (LED) was used for band-to-band excitation. The LED was positioned above the sample as shown in Figure 3.3(a). Although transparent, the ITO top contact will block some of the light from the LED. In order to determine an accurate optical power density of the light on the β-Ga_2O_3 substrate, a few optical power measurements were performed. A photodiode power sensor was placed in the sample position as the $(Y_{0.6}Sc_{0.4})_2O_3$/β-Ga_2O_3 sample and used to measure the optical power of the LED. A second measurement was made with a glass piece sputtered with 100 nm of ITO placed on top of the sensor as shown in Figure 3.3 (b). Lastly another measurement was made with a bare glass piece on top of the sensor. An optical power density of 0.1 mW$\times$cm^{-2} was calculated by the following equation:

$$P_{optical} = P_{LED} \times \frac{P_{glass+ITO}}{P_{glass}}. \tag{3.1}$$

Our photo-assisted *C*-*V* measurements were taken following the method of Swenson and Mishra [43]. A three-minute accumulation bias (+12 V) is applied to the MOSCAP in the dark to ensure all traps are filled with electrons (Figure 3.4 (a)). The *C*-*V* sweep is then measured; the interface traps do not respond to this measurement because of the high ac frequency used (1 MHz) (Figure 3.4 (a)-(b)). Next, the MOSCAP is biased in depletion at -15 V and illuminated with the LED. During top-side illumination, electron-hole pairs are generated near the insulator/semiconductor

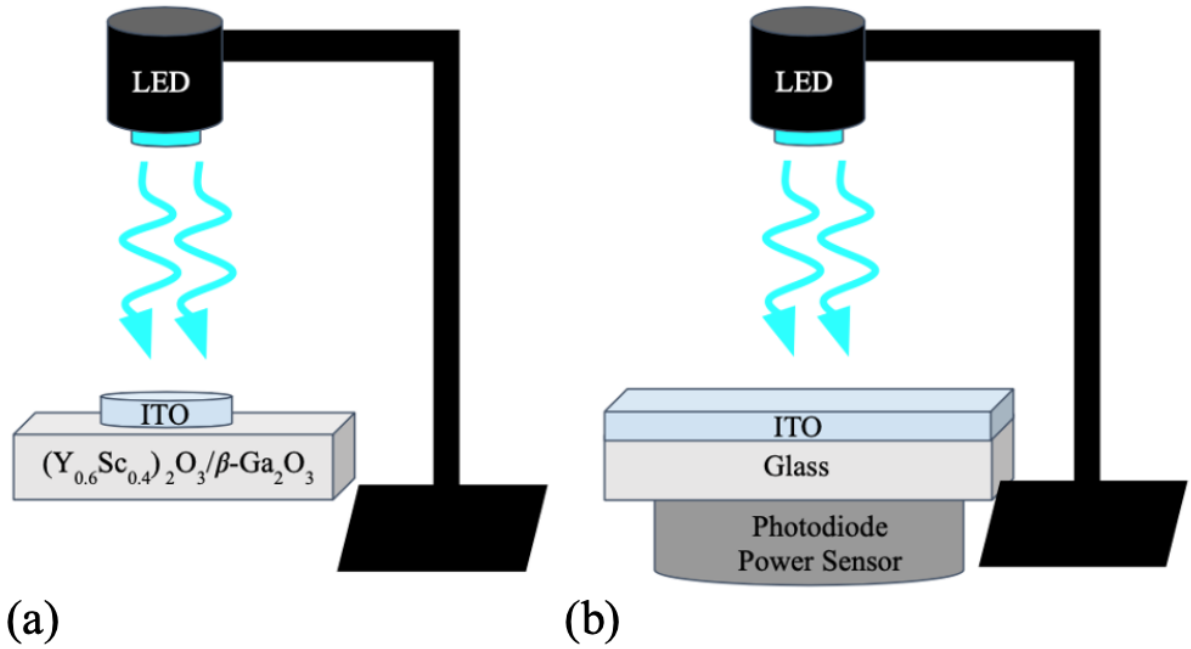


Figure 3.3: Illustrations of the photo-illumination setup showing topside illumination of the sample (a) and (b) the optical power measurement setup with a 100 nm ITO covered glass over the photodiode power sensor.

interface due to band-to-band excitation and the depletion bias causes the holes to move to the interface (Figure 3.4 (c)). The generated holes recombine with the trapped electrons at the interface, emptying the interface traps. Previously in bulk Ga_2O_3, self-trapping of holes has been observed. Here it is assumed that the photo-generated holes do not have time to be self-trapped before recombining at the interface. The change in charge at the interface causes the capacitance to increase. The illumination is turned off once the capacitance saturates, while the depletion bias remains in order for the MOSCAP to reach steady state. When the DUV illumination is removed, the capacitance rapidly drops as the remaining photo-generated holes are swept to the top contact and extracted, allowing interface trap states below the Fermi level to be filled by thermally-excited electrons (Figure 3.4 (d)). Lastly, a second *C-V* curve is taken, where interface traps are filled with electrons as the Fermi level rises through the bandgap. The concentration and energy distribution of the interface traps are then extracted from the *C-V* curves taken before and after illumination.

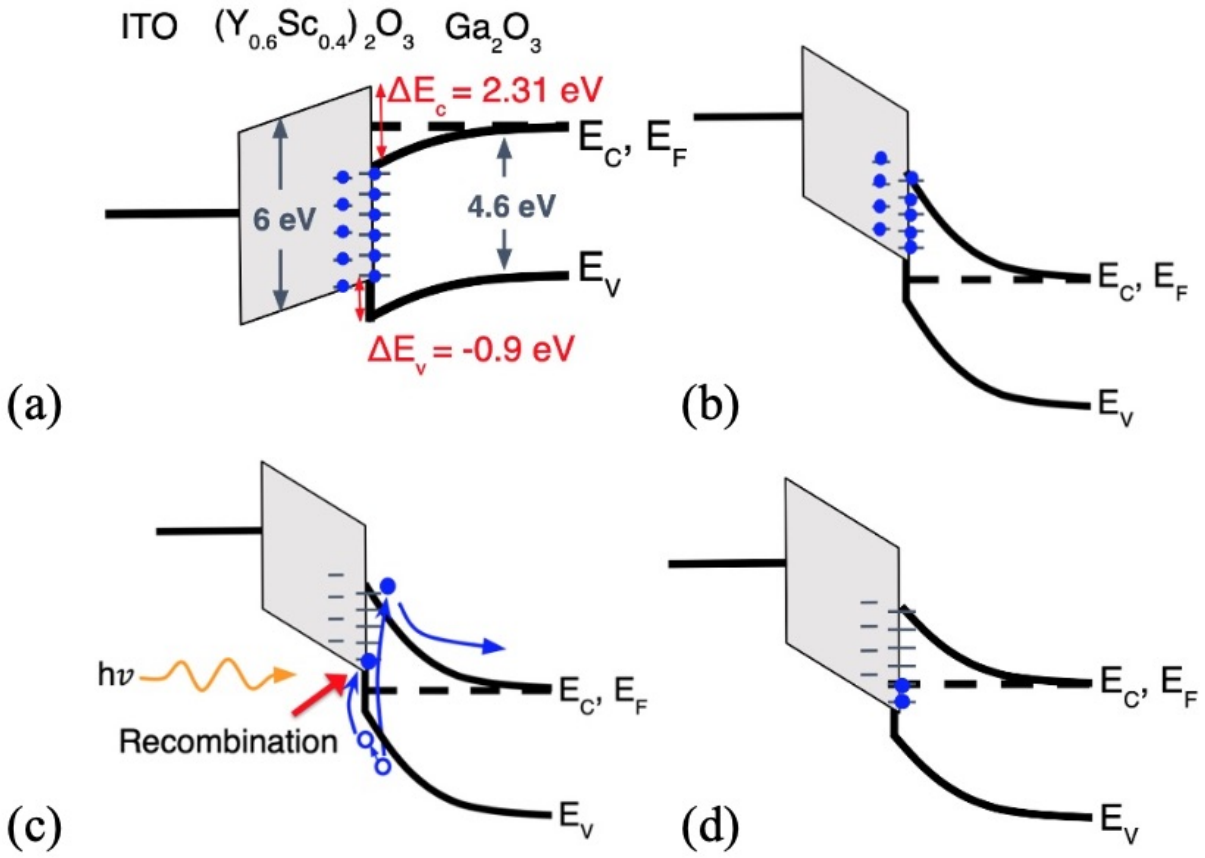


Figure 3.4: MOSCAP band diagrams: (a) in accumulation with all traps filled with electrons (estimated conduction and valence band offsets are indicated), (b) in depletion before DUV with traps filled; (c) in depletion during DUV, photo-generated holes recombine with trapped electrons; and (d) during voltage sweep after illumination, traps are filled as the Fermi level approaches the conduction band. $E_C = E_F$ within the bulk β-Ga_2O_3 due to the nearly degenerate level of Sn-doping. From [6].

3.3 Capacitance – Voltage results

3.3.1 Interface trap density results

The photo-assisted *C-V* results show a V_{fb} of 1.5 V after the MOSCAP was illuminated for 85 minutes (Figure 3.5). The voltage difference (ΔV) between the before and after DUV *C-V* curves is not constant for all capacitance values. This difference varies as the Fermi level approaches the conduction band indicating that there is an uneven distribution of interface traps within the bandgap. From the *C-V* curve before DUV illumination, the surface potential (ψ_{s}) can be calculated from

$$\psi_s = \frac{q\varepsilon_s\varepsilon_0 N_d}{2C_{sc}^2} \tag{3.2}$$

where q, ε_s, ε_0, N_{d}, and C_{sc} are the electron charge, semiconductor relative permittivity, vacuum permittivity, average doping density, and semiconductor capacitance, respectively. The D_{it} energy distribution can then be extracted by numerical differentiation [43]:

$$D_{it}(\psi_s) = \frac{C_{\mathrm{ox}}}{q}\left(\frac{d\Delta V}{d\psi_s}\right) \tag{3.3}$$

where C_{ox} is the oxide capacitance.

The resulting D_{it} energy distribution is shown in Figure 3.6 (c). A higher density of traps is located near the conduction band with a peak ($\sim 4 \times 10^{12}\ \mathrm{cm}^{-2}\mathrm{eV}^{-1}$) located 0.2 eV below the conduction band. The D_{it} drops below $\sim 2 \times 10^{11}\ \mathrm{cm}^{-2}\mathrm{eV}^{-1}$ at E_{C} - 0.9 eV, where the minimum measurable D_{it} is $\sim 1 \times 10^{10}\ \mathrm{cm}^{-2}\mathrm{eV}^{-1}$. Integrating the D_{it} distribution gives a total D_{it} charge of $<1 \times 10^{12}\ \mathrm{cm}^{-2}$. This D_{it} value is similar to those reported for SiO_2, HfO_2, and Al_2O_3 deposited by atomic layer deposition (ALD) [7, 38, 39, 44]. This technique assumes a uniform N_{d}, which will introduce a small error when calculating ψ_s [43].

The Terman method, which is a high-frequency *C-V* technique shown in Figure 3.6 (a) [41], was performed for comparison with the photo-assisted method. The ideal *C-V* curve was calculated based on the values N_d = 1.7 $\times$ 10^{18} cm^{-3} and V_{fb} = 7.3 V. The experimental N_d was extracted from

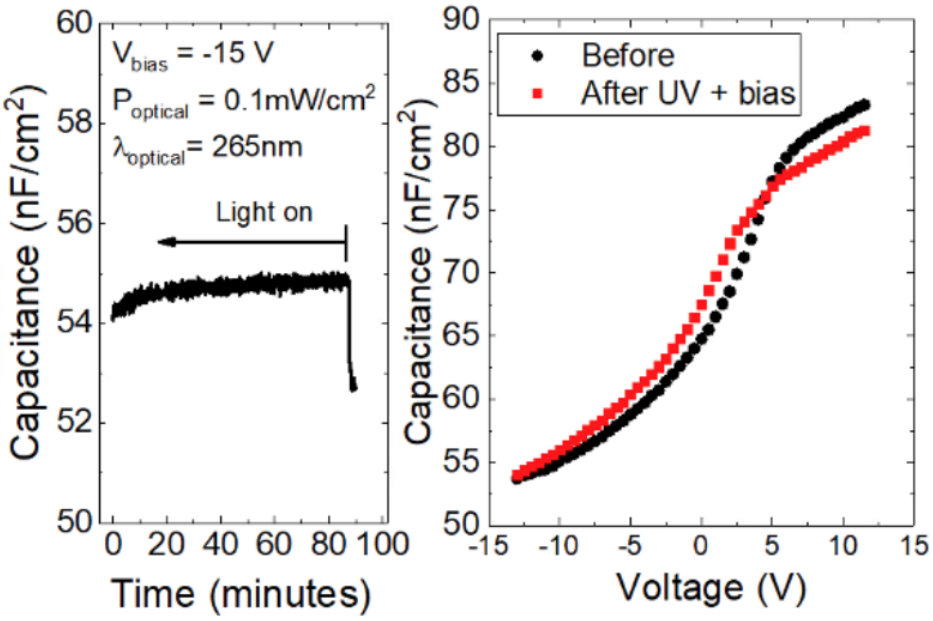


Figure 3.5: Photo-assisted *C-V* method results showing the rising capacitance value during the DUV illumination and depletion bias (left), and the *C-V* sweeps (right) before and after illumination and bias. From [6].

the slope of measured $1/C^2$ data following:

$$N_d = \frac{-2}{q\varepsilon_0\varepsilon_s \frac{d(1/C^2)}{dV}}. \tag{3.4}$$

The V_{fb} was determined by the x-intercept of the extrapolated line of $(C_{\text{ox}}/\text{C})^2$-1 [44]. D_{it} was calculated using (3.3), where ΔV is the gate voltage difference between the high frequency *C-V* curve and the ideal *C-V* curve [41]. The resulting D_{it} values are between $1 - 2 \times 10^{12}$ $\text{cm}^{-2}\text{eV}^{-1}$ in the energy range of 0.35 eV to 0.55 eV below the conduction band. The D_{it} results from the Terman method, which agree well with those obtained by photo-assisted *C-V*, are shown in Figure 3.6(c). The AC conductance method was also performed to extract D_{it} as a further means of comparison to photo-assisted *C-V* results. The standard C_{p}-G_{p} AC conductance circuit model was used [41]

$$\frac{G_p}{A\omega} = \frac{\omega G_m {C_{\text{ox}}}^2}{A(G_m^2 + \omega^2(C_{\text{ox}} - C_m)^2)}, \tag{3.5}$$

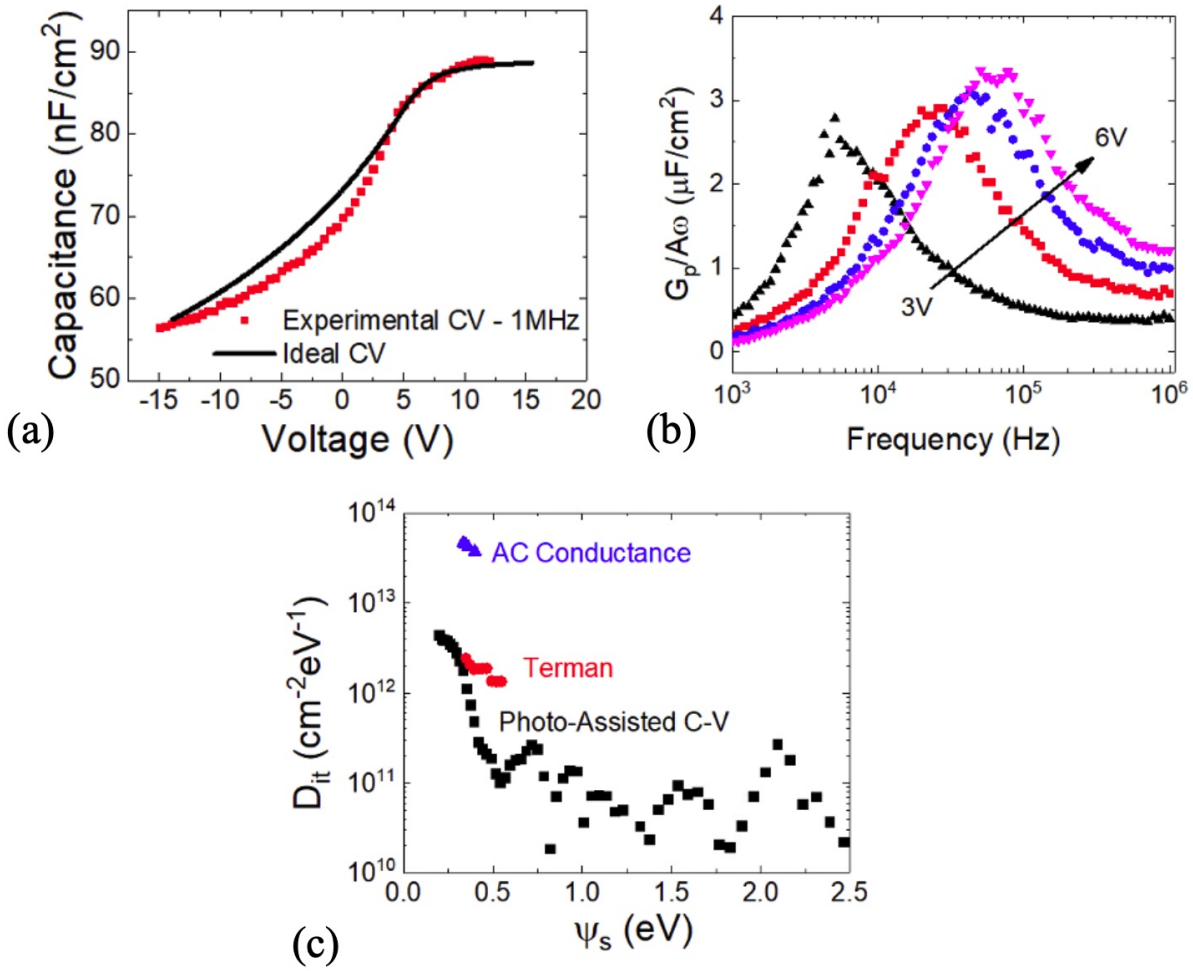


Figure 3.6: (a) Terman method *C*-*V* results. The ideal *C*-*V* curve was calculated using values of $N_d = 1.7 \times 10^{18}$ cm^{-3} and $V_{fb} = 7.3$ V that were extracted from the experimental *C*-*V* curve. The experimental *C*-*V* curve was taken from depletion to accumulation without any previous accumulation bias. (b) AC Conductance method results for voltages of 3, 4, 5 and 6 V using the standard C_p-G_p circuit model. (c) D_{it} energy distribution from the photo-assisted *C*-*V* method (black), Terman method (red), and AC conductance method (blue). Both the photo-assisted *C*-*V* method and Terman method required taking derivatives with respect to ψ_s; these derivatives were taken over seven data points. From [6].

where C_m and G_m are the measured parallel capacitance and conductance, A is the area, and ω is the frequency. D_{it} is calculated from the maximum $G_p/A\omega$ value for each voltage in Figure 3.6(b) using the relation [41]

$$D_{it} = \frac{2.5 \times max(\frac{G_p}{A\omega})}{q}. \tag{3.6}$$

The resulting D_{it} values are $\sim 4 - 5 \times 10^{13}\mathrm{cm}^{-2}\mathrm{eV}^{-1}$. These values are more than an order of magnitude larger than those obtained from the photo-assisted and Terman method results (Figure 3.6 (c)).

Weak Fermi-level pinning has been previously reported [66] as a source of unreliable D_{it} extraction from conductance measurements for MOSCAPs with a low C_{ox} value and relatively high D_{it}, i.e., when $C_{it} = q \times D_{it} > C_{ox}$. Due to the thick dielectric layer, C_{ox} is less than C_{it} in this region of the bandgap, near E_C - 0.35 eV. Other reports have successfully used the AC conductance method on β-Ga_2O_3 MOSCAPs with thin oxide layers that have larger C_{ox} values [39, 44]. In this study, reliable D_{it} extraction from conductance measurements would require MOSCAPs with thinner dielectric layers.

3.3.2 *C-V* non-idealities

A non-ideal feature of the *C-V* curves was observed for the $(Y_{0.6}Sc_{0.4})_2O_3$/β-Ga_2O_3 as well as for SiO_2/β-Ga_2O_3 (010) MOSCAPs fabricated by low pressure chemical vapor deposition (LPCVD) of silicon dioxide. The *C-V* curves in Figure 3.4 and in Figure 3.7 (a) show an increasing accumulation capacitance with increasing positive voltage. A possible explanation for the rising accumulation capacitance is the filling of border traps in the dielectrics when the MOSCAP is in accumulation (Figure 3.7(b)) [51]. The presence of border traps has been observed in several dielectrics paired with β-Ga_2O_3 including Al_2O_3, SiO_2, and Al_2O_3/HfO_2 bilayer stacks [42, 44, 54]. Border traps will be discussed further in Chapter 4.

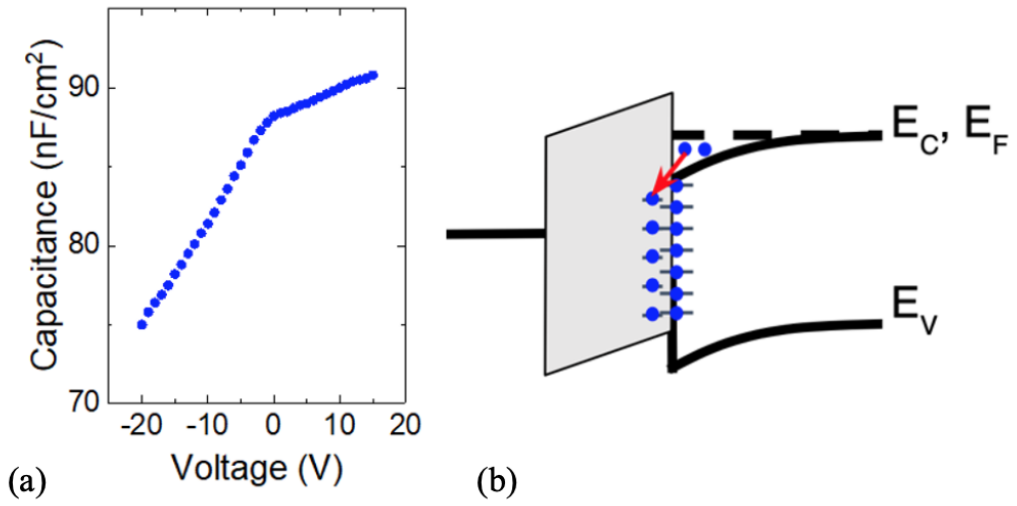


Figure 3.7: (a) *C-V* curve of β-Ga_2O_3 (010) MOSCAP with SiO_2 as the dielectric showing the increasing accumulation capacitance with increasing voltage bias. This feature was also observed in β-Ga_2O_3 (010) MOSCAPs with $(Y_{0.6}Sc_{0.4})_2O_3$ as the dielectric (Figure 3.4). The SiO_2 layer was 38 nm thick, and was deposited by LPCVD. (b) Band diagram of MOSCAP showing the filling of border traps while in accumulation. From [6].

3.4 Current – Voltage results

3.4.1 Dark and Illuminated *J-V* results

Current-voltage (*J-V*) measurements of MOSCAPs with sizes ranging from $0.79\times10^{-4}\mathrm{cm}^{-2}$ to 12.6×10^{-4} cm^{-2} showed leakage of $<$100 nA·cm^{-2} at low voltage bias (Figure 3.8(a)). The $(Y_{0.6}Sc_{0.4})_2O_3$ films were also tested to obtain the electrical breakdown field. $(Y_{0.6}Sc_{0.4})_2O_3$ films on β-Ga_2O_3 substrate showed high destructive breakdown fields of 4.3 to 6.0 MV·cm^{-1}. Examples of leakage and breakdown for both positive and negative applied voltage are shown in Figure 3.8 (b). Leakage increases significantly as the MOSCAP is biased even a few volts into accumulation (positive bias). In contrast, the leakage in depletion (negative bias) remains low at 10 nA·cm^{-2} until a voltage bias of $\sim$-25 V is reached. These trends were observed for either ITO or Ti/Au top contacts. To explain the differences in the leakage mechanisms for accumulation and depletion bias, illumination and temperature-dependent measurements were performed.

The top side of the MOSCAP was illuminated with a DUV (265 nm) LED during *J-V*

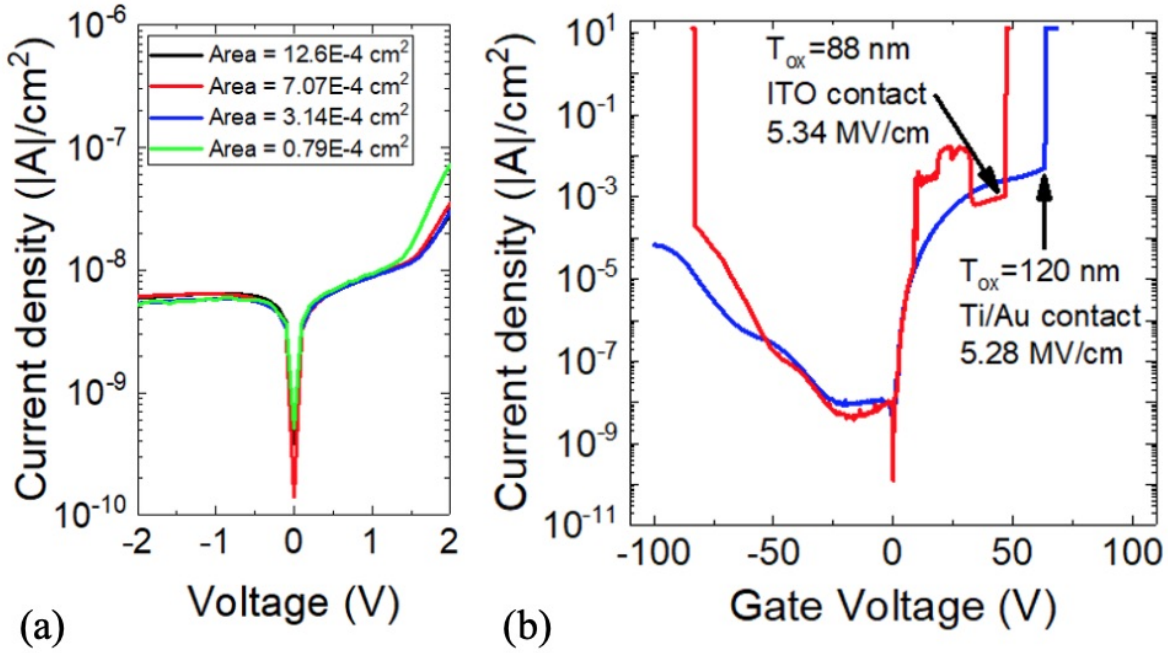


Figure 3.8: (a) *J-V* measurements of $(Y_{0.6}Sc_{0.4})_2O_3/\beta$-$Ga_2O_3$ (010) MOSCAPs of various sizes at low voltages. (b) Current density versus voltage at high fields, including breakdown. MOSCAPs with ITO top contacts as well as those with Ti/Au (10/90 nm) were measured. For all data, continuous measurements were performed with long integration time. From [6].

measurements. Figure 3.9(a) shows photo-induced increase in leakage during depletion (negative bias), presumably due to photo-generation of electron-hole pairs. Due to the negative valence band offset between $(Y_{0.6}Sc_{0.4})_2O_3$ and β-Ga_2O_3, holes generated in β-Ga_2O_3 near the interface encounter no barrier to impede their transport to the ITO contact. A hole diffusion length of 333 nm at room temperature has been reported for β-Ga_2O_3 [67], which is significantly larger than the depletion width within this voltage range. By increasing the optical power of the LED, the number of generated holes increases, increasing leakage current [68]. This phenomenon is illustrated in Figure 3.9 (b). This observation implies that when the MOSCAP is in depletion, leakage current is determined by the density of free holes in β-Ga_2O_3. As with *C-V* measurements, it is assumed here negligible self-trapping of photo-generated holes near the interface.

In addition to the current saturation observed in depletion, the *C-V* curve shown in Figure 3.10 (a) indicates the MOSCAP moves into deep depletion with larger negative bias. Instead of

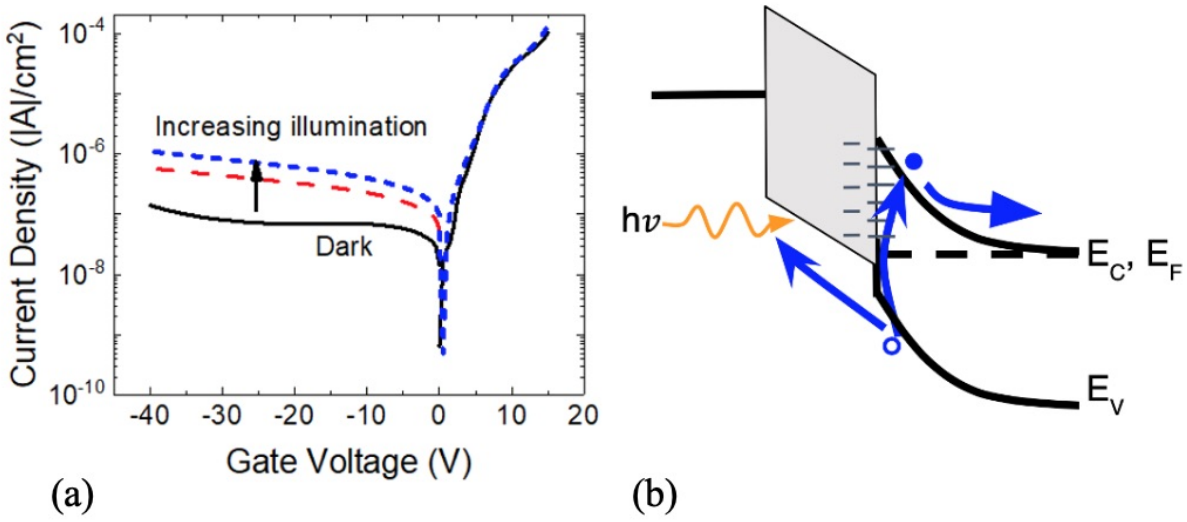


Figure 3.9: (a) *J-V* measurements of $(Y_{0.6}Sc_{0.4})_2O_3/\beta$-$Ga_2O_3$ (010) MOSCAPs in the dark and under illumination. (b) Band diagram of $(Y_{0.6}Sc_{0.4})_2O_3/\beta$-$Ga_2O_3$ (010) MOSCAPs in depletion under illumination of 0.05 and 0.1 mW/cm^2. From [6].

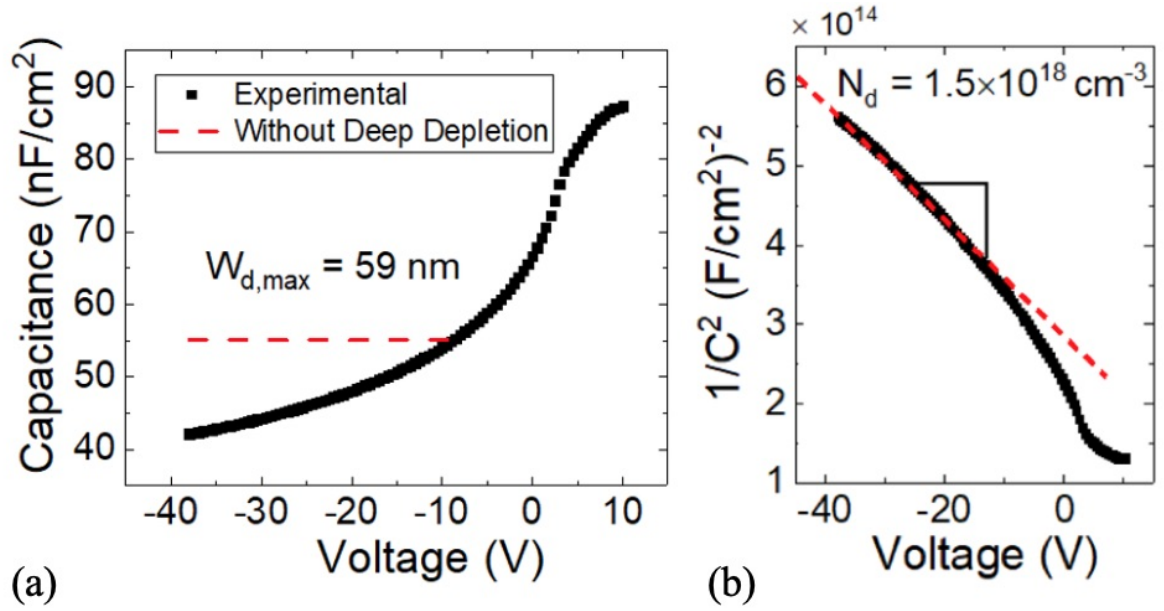


Figure 3.10: (a) *C-V* curve of $(Y_{0.6}Sc_{0.4})_2O_3/\ \beta$-$Ga_2O_3$ MOSCAP extending into deep depletion. Calculated minimum capacitance due to maximum depletion width. (b) $1/C^2$ - *V* plot showing uniform Nd throughout the deep depletion region. From [6].

the capacitance saturating due to reaching a maximum depletion width, the MOSCAP continues to deplete in order to generate more carriers to facilitate the leakage current [68]. The $1/C^2$-V data (Figure 3.10 (b)) shows a nearly linear slope within the deep depletion region indicating a uniform doping profile. The varying slope within the weak depletion region may be due to Sn incorporating into the $(Y_{0.6}Sc_{0.4})_2O_3$ from the β-Ga_2O_3.

In contrast, during accumulation (positive bias), illumination caused no significant change in the leakage current (Figure 3.9 (a)). In this regime, the leakage current is not limited by the number of free electrons in heavily-doped Ga_2O_3. Temperature dependent J-V measurements were used to determine that the large leakage observed in accumulation is governed by bulk-limited transport across the dielectric: traps in the dielectric enable electron transport to the ITO contact.

3.4.2 Temperature Dependent *J-V* results

$(Y_{0.6}Sc_{0.4})_2O_3/\beta$-$Ga_2O_3$ MOSCAPs were measured at temperatures from 200K to 300K (Figure 3.11). At positive voltages (accumulation), leakage increased at higher temperatures and higher voltage biases. The Poole-Frenkel emission model was used to fit the data [69], but the extracted value of ε_r, 24, was significantly larger than the value of 8.3 - 8.5 extracted by *C-V*. Simmons has reported [70] that insulators containing donor-like traps can be modelled using modified Poole-Frenkel emission:

$$J = q\mu N_c \Big(\frac{N_d}{N_t}\Big)^{1/2} E \times \exp\Big(\frac{\beta_{PF}E^{1/2} - (E_d + E_t)}{2kT}\Big), \tag{3.7}$$

where μ is the electron mobility, and N_c, N_d, and N_t are the conduction band density of states, donor trap density and shallow trap density, respectively. The Poole-Frenkel factor, β_{PF}, is given by

$$\beta_{PF} = \Big(\frac{q^3}{\pi\varepsilon_0\varepsilon_r}\Big)^{1/2}. \tag{3.8}$$

This conduction mechanism relies on the presence of a trap level in the dielectric at energy E_d that can promote electrons to a shallow trap level, E_t [70]. Here, the values of E_d and E_t are

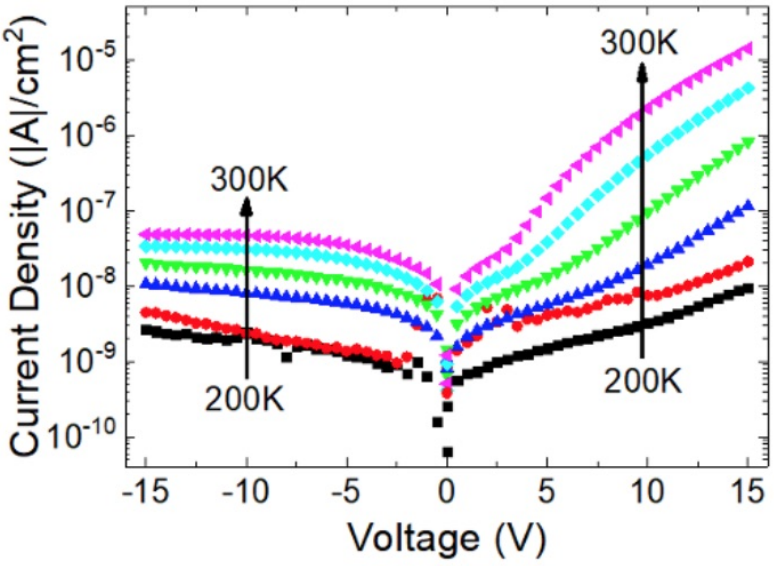


Figure 3.11: *J-V* measurements of $(Y_{0.6}Sc_{0.4})_2O_3$/ β-Ga_2O_3 (010) MOSCAPs at temperatures from 200K to 300K. From [6].

taken with respect to the conduction band edge of the dielectric. An ε_r value of 7 was extracted from the slope of ln(*J/E*) vs $E^{1/2}$ (Figure 3.12 (a)). The sum of the trap levels (E_d+E_t) was then determined to be 1.4 eV using the slope of ln(*J/E*) vs 1/k*T* (Figure 3.12 (b)). Figure 3.12 (c) shows that the positive bias experimental data fits nicely with the modified Poole-Frenkel emission at high electric fields and high temperatures. This fitting indicates there are at least two traps levels near the conduction band of the $(Y_{0.6}Sc_{0.4})_2O_3$ dielectric, which facilitate the high leakage observed when the MOSCAP is in accumulation (Figure 3.12 (d)). In the future, traps in the dielectric could be reduced by optimizing the solution process for depositing $(Y_{0.6}Sc_{0.4})_2O_3$ on β-Ga_2O_3 or by depositing this dielectric using a different method. A higher dielectric constant could also be achieved by using a different deposition method, such as ALD [71].

In contrast to the positive bias leakage, the leakage results with negative bias show a weak electric field dependence for all temperatures between 200K and 300K. The Arrhenius plot of the negative bias leakage current (Figure 3.13 (a)) shows a low thermal activation energy of $\sim$ 0.16 eV. The weak temperature dependence indicates the negative bias leakage is not due to band-to-band electron-hole pair generation; instead, the holes are thermally generated with the assistance of a deep

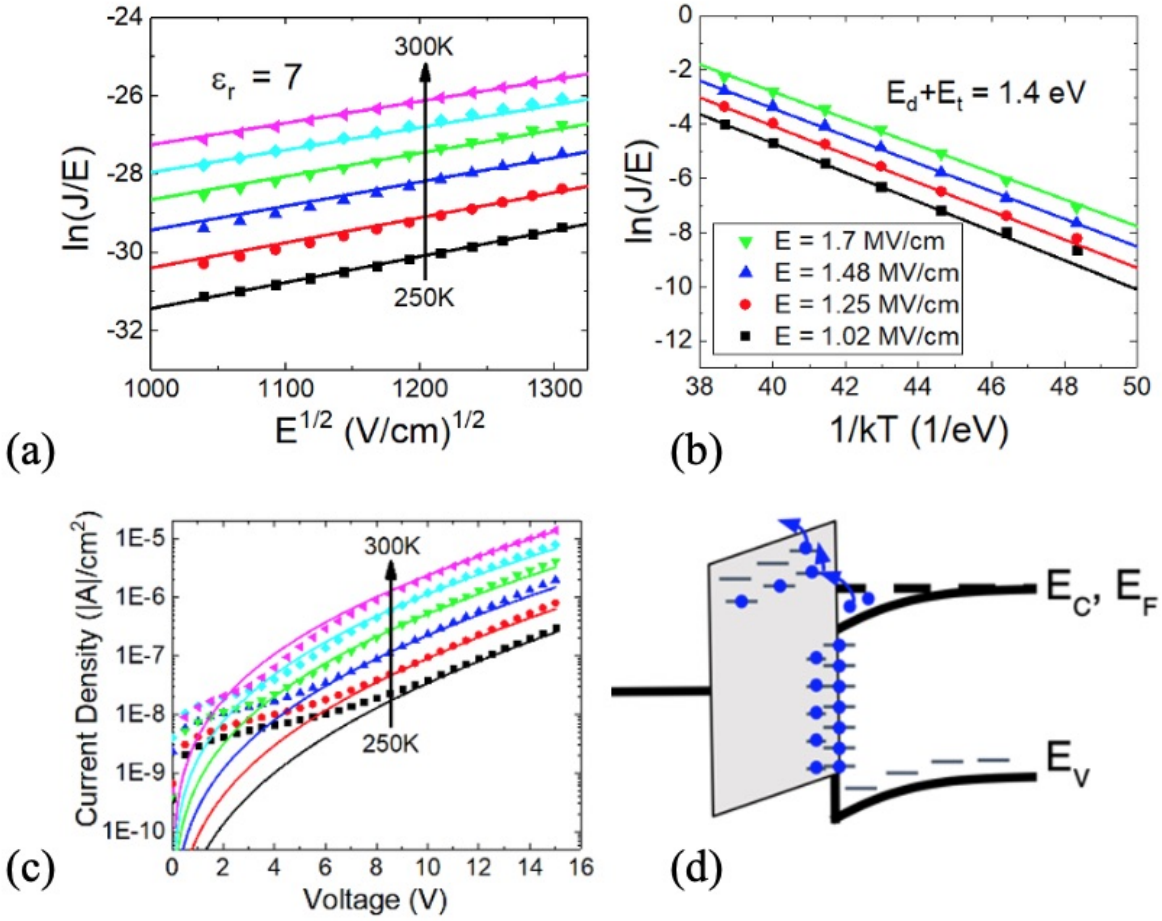


Figure 3.12: (a) Dielectric constant extracted from slope of ln(J/E) vs $E^{1/2}$ at various temperatures in accumulation; (b) Dielectric trap levels (E_d+E_t) extracted from slope of ln(J/E) vs 1/kT; (c) Modified Poole-Frenkel conduction (solid) fitted to experimental positive bias leakage data (symbols). (d) Band diagram of MOSCAP in accumulation showing the modified Poole-Frenkel leakage current mechanism. From [6].

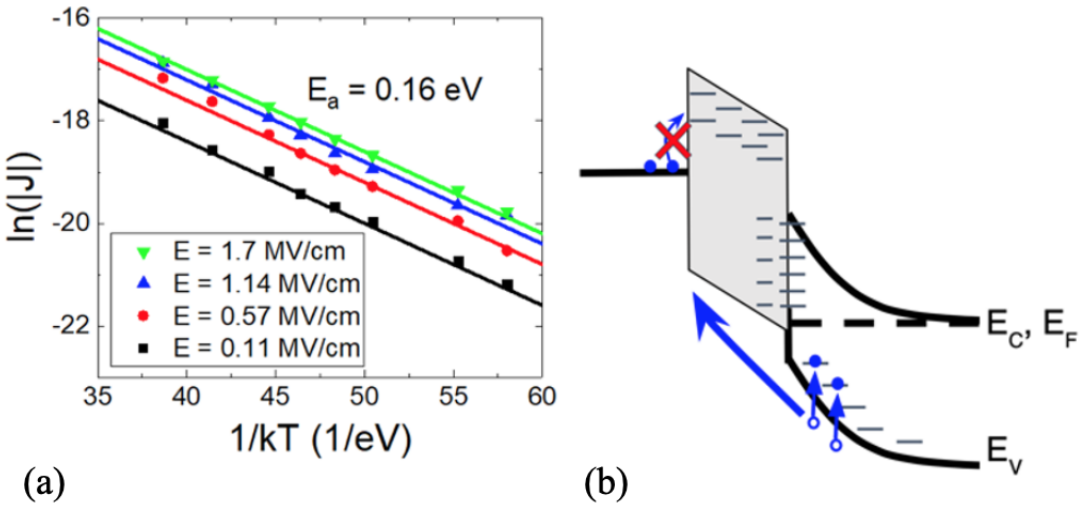


Figure 3.13: (a) Arrhenius plot of the depletion (negative bias) leakage current showing a thermal activation energy (E_a) of 0.16 eV. (b) Band diagram of MOSCAP in depletion illustrating hole generation facilitated by a deep trap level near the valence band. The traps near the conduction band of the dielectric do not contribute to the leakage current observed in depletion. From [6].

level trap near the valence band of the β-Ga_2O_3 (Figure 3.13 (b)). Deep level optical spectroscopy (DLOS) measurements have shown a defect state located 0.44 eV above the valence band in bulk unintentionally doped (UID) β-Ga_2O_3 with (010) orientation grown by the edge-defined film-fed growth (EFG) method [72]. The deep-level trap observed here may correspond to a similar defect state in our Sn-doped β-Ga_2O_3 (010) substrate, which was also grown by EFG. Furthermore, at or below room temperature, the traps near the conduction band of the dielectric do not significantly contribute to the observed reverse bias leakage, due to the large energy difference with the Fermi level of the ITO contact, estimated to be 1.3 eV.

3.5 Conclusion

Due to the large bandgap of β-Ga_2O_3 and the need for a large conduction band offset, much of the focus has been placed on SiO_2, Al_2O_3, and HfO_2 as the gate dielectric for β-Ga_2O_3 MOS structures. Scandate-based dielectrics are beneficial for their moisture insensitive properties, and ternary oxides tend to have higher crystallization temperatures than most binary oxides. Both of

Dielectric	t_{ox}**(nm)**	**Average** D_{it} **(**10^{11} **cm^{-2}eV^{-1})**	**Total** D_{it} **(**10^{12} **cm^{-2})**	ΔE_C **to** Ga_2O_3 **(eV)**	κ	**Reference**
ALD SiO_2	20	6	–	3.63	3.9	[39]
LPCVD SiO_2	45	2 - 20	2.2*	2.8 - 3.6	3.8	[38]
ALD Al_2O_3	15	2.3*	–	–	8.5	[44]
PLD γ-Al_2O_3	30	20 *	–	1.9	6.9	[57]
ALD Al_2O_3	50	0.5 - 10	0.84 *	1.5 - 2.2	7.6	[38]
ALD Al_2O_3/HfO_2	20	1 - 84	–	1.5	8.4	[54]
ALD HfO_2/Al_2O_3	20	2.2 - 80	–	1.5	9.6	[54]
ALD HfO_2	40	1.3	–	1.3	14.0	[7]
ALD Al_2O_3/SiO_2	15	0.5 -3		3.6	6.72	[47]
ALD HfAlO	31	4.45*	–	1.5	11.32	[73]
Sol-gel $(Y_{0.6}Sc_{0.4})_2O_3$	88	1.7*	< 1 *	2.31	8.3 - 8.5	This work [6]

Table 3.1: Dielectrics used in β-Ga_2O_3 MOSCAPs which report interface state density (D_{it}). Oxide thickness (t_{ox}), average and total D_{it}, conduction band offset (ΔE_C) to β-Ga_2O_3, and dielectric constant (κ) are listed. D_{it} values extracted by the photo-assisted *C-V* technique are indicated by *.

these aspects could lead to a MOS device with better environmental and temperature stability. A solution-processed ternary scandate-based dielectric, $(Y_{0.6}Sc_{0.4})_2O_3$, had previously been developed on Si, and in this chapter, its potential as a dielectric for future β-Ga_2O_3 MOS devices was analyzed.

Here, $(Y_{0.6}Sc_{0.4})_2O_3$/β-Ga_2O_3 (010) MOSCAPs have been fabricated, and several characterization methods have been performed to analyze the interface trap density (D_{it}). The photo-assisted *C-V* method was used to extract D_{it} from a larger range of the bandgap compared to traditional D_{it} methods such as Terman and AC conductance. On un-optimized MOSCAPs, a low total D_{it} charge of $< 1 \times 10^{12}$ cm^{-2} was found with a peak D_{it} of $\sim 4 \times 10^{12}$ cm^{-2}eV^{-1} near the conduction band (E_C - 0.2 eV). When compared to other β-Ga_2O_3 MOSCAPs (Table 3.1), this dielectric shows great promise for interfacial quality.

The $(Y_{0.6}Sc_{0.4})_2O_3$ MOSCAPs were further investigated for their potential in β-Ga_2O_3 devices using various current density - voltage (*J-V*) methods. Deep depletion was observed, with

leakage current governed by generation of holes from deep-level Ga_2O_3 traps. In accumulation, leakage current rises quickly with applied bias due to bulk-limited transport of majority carrier electrons through traps near the conduction band of $(Y_{0.6}Sc_{0.4})_2O_3$, known as modified Poole-Frenkel emission. For both bias polarities, high breakdown fields of 4.3 - 6.0 MV·cm^{-1} were observed.

These results indicate a high-quality interface between the solution-processed $(Y_{0.6}Sc_{0.4})_2O_3$ film and the β-Ga_2O_3 substrate. While the dielectric films used here were rather thick (88 nm), in the future the dielectric thickness can be reduced by using an ink with a lower molarity. Furthermore, the dielectric and interface may be improved by ALD deposition or post-deposition treatments. Based on the low D_{it} value and the predicted large conduction band offset of 2.31 eV, $(Y_{0.6}Sc_{0.4})_2O_3$ appears to be an excellent candidate for the gate dielectric of β-Ga_2O_3 planar MOSFETs. The results of this chapter, also, helps establish *C*-*V* and *J*-*V* techniques that are useful for analyzing compatibility of other dielectrics with WBG semiconductors.

CHAPTER 4

Charge Trapping and Recovery in ALD HfO_2/β-Ga_2O_3 (010) MOS Capacitors

4.1 Introduction

In Chapter 3, I used multiple capacitance - voltage (*C*-*V*) and current density - voltage (*J*-*V*) techniques in order to analyze the capability of a new dielectric with β-Ga_2O_3. I was able to show the solution-processed ternary scandate-based dielectric, $(Y_{0.6}Sc_{0.4})_2O_3$, had a low interface trap density (D_{it}) with highly Sn-doped β-Ga_2O_3 (010) substrates. While this dielectric creates a clean interface with planar β-Ga_2O_3, solution-process is not an ideal deposition technique for uniform dielectric layers over non-planar features.

In order to achieve an enhancement-mode vertical power MOSFET with β-Ga_2O_3, a finFET structure is necessary. Due its nonplanar structure, a conformal dielectric layer would be hard to achieve with many deposition techniques, especially solution-processing. Atomic layer deposition (ALD) is the superior dielectric deposition method for these non-planar structures. ALD is a vapor phase technique that is capable of producing thin, conformal, high-quality layers of many materials, especially high-κ dielectrics. Alternating pulses of gaseous chemical precursors react to the surface leaving one monolayer at a time; this process allows for angstrom level thickness control. This process was adopted by Intel in 2007 for depositing their high-κ gate oxide stacks [74]. Due to the many benefits of ALD, including fewer pinholes, conformality, thickness control, and tunable film composition [74], this dielectric deposition technique has been the most frequently used for

β-Ga_2O_3 MOSFETs [13].

To date, β-Ga_2O_3 MOSFETs have only been reported with Al_2O_3, SiO_2, and HfO_2 gate dielectrics [3]. As previously mentioned, dielectrics in power MOSFETs must meet many criteria. These include a high dielectric constant (κ), large conduction band offset (ΔE_C) to the semiconductor, large breakdown field, and low leakage current. Most of the focus has been on Al_2O_3 and SiO_2. While SiO_2 has a very large ΔE_C of $\sim$3.6 eV [75], the dielectric constant is low. ALD Al_2O_3, which has been used in many β-Ga_2O_3 MOSFETs, has both a large ΔE_C and κ of 1.5 eV and 8.9, respectively [40]. On the downside, post-deposition annealing studies have shown the Al_2O_3/β-Ga_2O_3 interface is not stable at high temperatures [11].

HfO_2 has shown great potential as a gate dielectric for β-Ga_2O_3 devices due to its higher dielectric constant ($>$14) compared to SiO_2 and Al_2O_3. Example *C-V* characteristics of HfO_2/ $(\bar{2}01)$ β-Ga_2O_3 MOSCAPs are shown in Figure 4.1 (a) [7] and (b) [8]. This dielectric, deposited by atomic layer deposition (ALD), has been reported to have a low D_{it} of 1.3×10^{11} $\mathrm{cm^{-2}eV^{-1}}$ with $(\bar{2}01)$ β-Ga_2O_3 as shown by Figure 4.1 (c), which was extracted using the Terman method [7]. Figure 4.1 (d) shows the band alignment of HfO_2 to $(\bar{2}01)$ β-Ga_2O_3 determined with X-ray Photoelectron Spectroscopy (XPS), which includes a ΔE_C of 1.3 eV [9]. Due to the necessity of a conformal, high-quality, ALD dielectric film for vertical β-Ga_2O_3 MOSFETs, I continued my investigation of dielectric interfaces to β-Ga_2O_3 with ALD HfO_2.

The reliability of the MOS structure is also crucial for the performance of high-power devices. Charge trapping in the gate insulator can lead to threshold voltage shifts and premature dielectric breakdown of the transistor. A few studies have reported the results of constant-voltage stress on β-Ga_2O_3 metal-oxide-semiconductor capacitors (MOSCAPs) including on Al_2O_3 [76] and HfAlO [48], but no studies have been reported on the reliability of or the possibility of recovery from stress-induced charge trapping on HfO_2 with β-Ga_2O_3. In this chapter, positive bias stress testing was used to investigate the charge trapping and photo-assisted recovery behavior of ALD HfO_2 in β-Ga_2O_3 MOSCAPs. The investigation of the impact of a staggered band alignment (negative valence band offset) with the wide bandgap semiconductor is continued in this chapter.

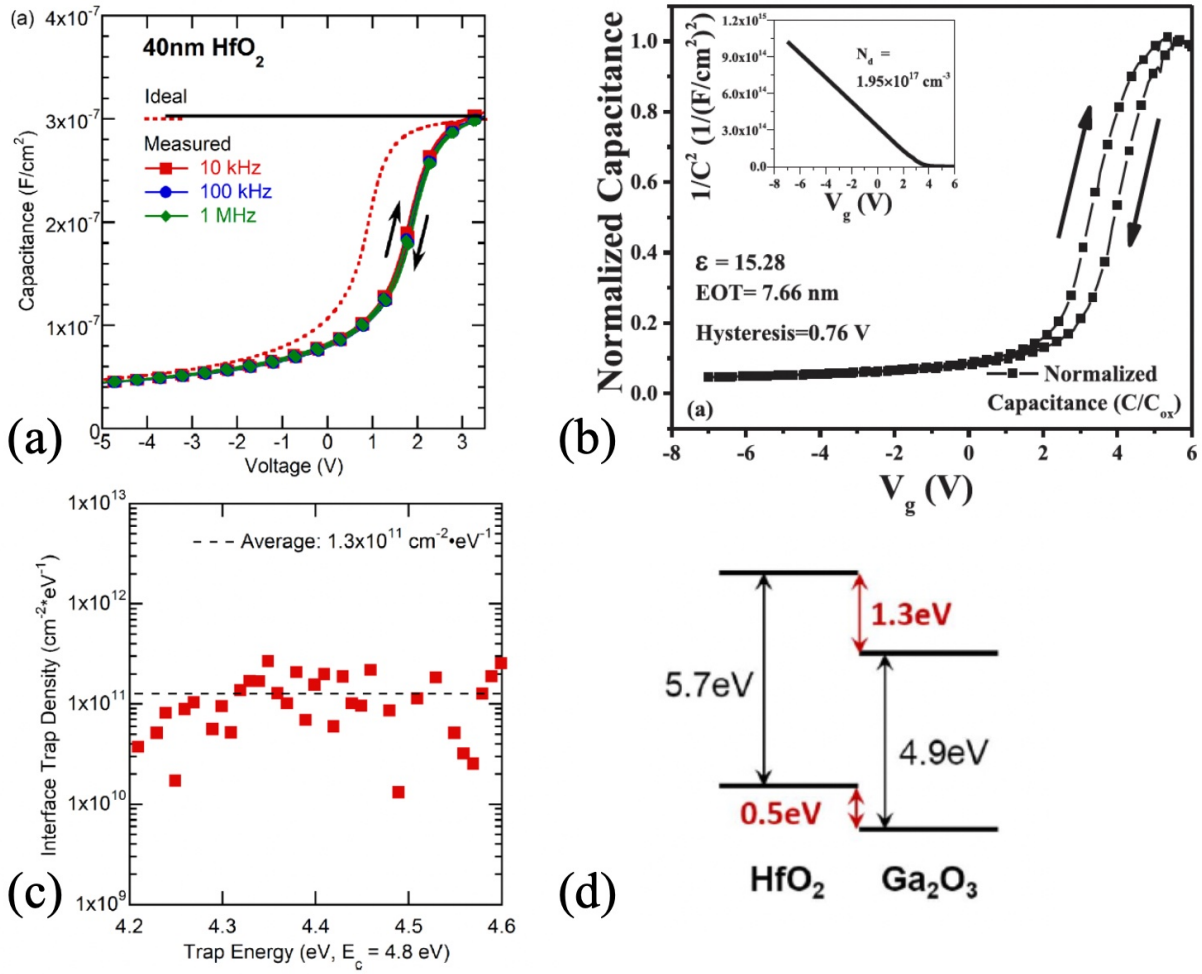


Figure 4.1: *C-V* characteristics of HfO_2/ $(\bar{2}01)\beta$-Ga_2O_3 MOSCAPs from (a) [7] (b) [8]. (c) D_{it} extracted from HfO_2/ $(\bar{2}01)\beta$-Ga_2O_3 MOSCAPs using the Terman method [7]. (d) Band alignment of HfO_2/β-Ga_2O_3 MOS structure from [9]. Used with permission of AIP Publishing and IOP Publishing; permission conveyed through Copyright Clearance Center, Inc.

4.2 Experimental Methods

HfO_2/β-Ga_2O_3 MOSCAPs were formed on Sn-doped β-Ga_2O_3 (010) substrates from Tamura Corporation. Diced substrates were cleaned with solvents, then treated with a 10-min piranha etch and 1-min buffered hydrofluoric acid dip. Next, 43 nm of HfO_2 was deposited using a Veeco Fiji ALD at 200°C with tetrakis(dimethylamido)hafnium (TDMAH) and H_2O. The recipe includes pulse times of 0.06 s and 0.25 s for H_2O and TDMAH, respectively, with 12 s purge times. The Ar carrier and plasma flow rates are 60 and 400 sccm, respectively. Post deposition annealing was performed on the HfO_2 film at 500°C in forming gas for five minutes. Backside ohmic contacts were formed with a 5-min ion mill etch before depositing Ti/Au (20 nm /230 nm) using electron beam evaporation. The samples were annealed at 470°C in N_2 for one minute to improve the ohmic contact, following [27]. Next, 100 nm of indium tin oxide (ITO) was sputtered and patterned for the top contact, and a 5-min forming gas anneal was performed at 450°C to improve the conductivity of the ITO contact [64]. ITO was used as a top contact to facilitate photo-illumination experiments, following [6].

ALD HfO_2/Si MOSCAPs were fabricated simultaneously to serve as an experimental control. Silicon (100) samples, n-type with resistivity of 1 – 10 Ω-cm, were cleaned with solvents before ALD deposition. HfO_2 was deposited on Si and β-Ga_2O_3 during the same ALD run; the resulting HfO_2 thickness on Si was 42 nm. The HfO_2 film thickness was measured with a J A Woollam M-2000 Ellipsometer. The slight difference in HfO_2 thickness on the two substrates (43 nm on Ga_2O_3 and 42 nm on Si) is most likely due to the difference in sample size. The Si sample experienced the same annealing steps and top contact ITO deposition as the β-Ga_2O_3 sample. The ohmic contact to Si was formed by soldering Sn to the Si substrate.

All measurements were performed in the dark at room temperature, unless specified otherwise. Capacitance-voltage (*C*-*V*) measurements were taken at a frequency of 1 MHz, a sweep rate of 1 V$\cdot$ s^{-1}, and an AC voltage amplitude of 50 mV with an HP4284A LCR meter. *C*-*V* sweeps were taken in the direction from depletion (-*V*) to accumulation (+*V*). Doping concentrations, N_D, of $\sim 3 \times 10^{18}$ $\mathrm{cm}^{-3}$and $\sim 2 \times 10^{15}$ cm^{-3} were extracted from the slope of the $1/C^2$ data for the

β-Ga_2O_3 and Si substrates, respectively. For stress measurements, a positive bias stress was applied to the MOSCAP. Periodically, the bias stress was stopped to take a *C-V* sweep. Illumination studies were performed with a DUV LED with a wavelength of 265 nm and optical power density of ~ 0.1 mW·cm^{-2}, using the setup described in [6].

4.3 Results and Discussion

4.3.1 Positive bias stress results

Figure 4.2(a) shows typical positive bias stress results for an ALD HfO_2/β-Ga_2O_3 MOSCAP. The MOSCAP was held at +12 V between *C-V* sweeps, which corresponds to an electric field bias (E_{stress}) of $\sim$1.41 MV·cm^{-1}, where Estress corresponds to difference between the applied voltage and the flatband voltage (V_{fb}), divided by the dielectric layer thickness. After an initial "fresh" *C-V* sweep is measured, several subsequent *C-V* sweeps were taken before starting stress measurements in order to fill border traps which cause a static V_{fb} shift [54]. The last *C-V* curve measured before stress measurements is referred to as the "stable" *C-V* curve. The initial application of voltage stress was for 100 s. A subsequent *C-V* sweep showed a positive V_{fb} shift of $\sim$0.3 V. This stress/measurement process was repeated several more times with increasing voltage stress times. The cumulative stress duration was 4300 s. As shown in figure 4.2(a), the *C-V* curves continue to shift more positively with longer stress times. This is also observed in the right-ward shifts of the $(C_{ox}/C)^2$-1 curves in figure 4.2(b), where C_{ox} is the oxide capacitance per unit area and the x intercept indicates V_{fb}. Other β-Ga_2O_3 MOSCAPs were tested in the same manner with various stress bias values. The change in V_{fb} from the stable, pre-stress value is defined as ΔV_{fb}. Figure 4.2 shows ΔV_{fb} for various stress biases. From this figure, it is clear that high E_{stress} and/or long t_{stress} lead to significant charge trapping in these MOSCAPs.

The White and Cricchi logarithmic model was used to fit the ΔV_{fb} data for higher stress fields, as shown in figure 4.3. This model assumes charge trapping occurs by direct tunneling of surface state charges to traps within the dielectric at the same energy level [77]. The resulting

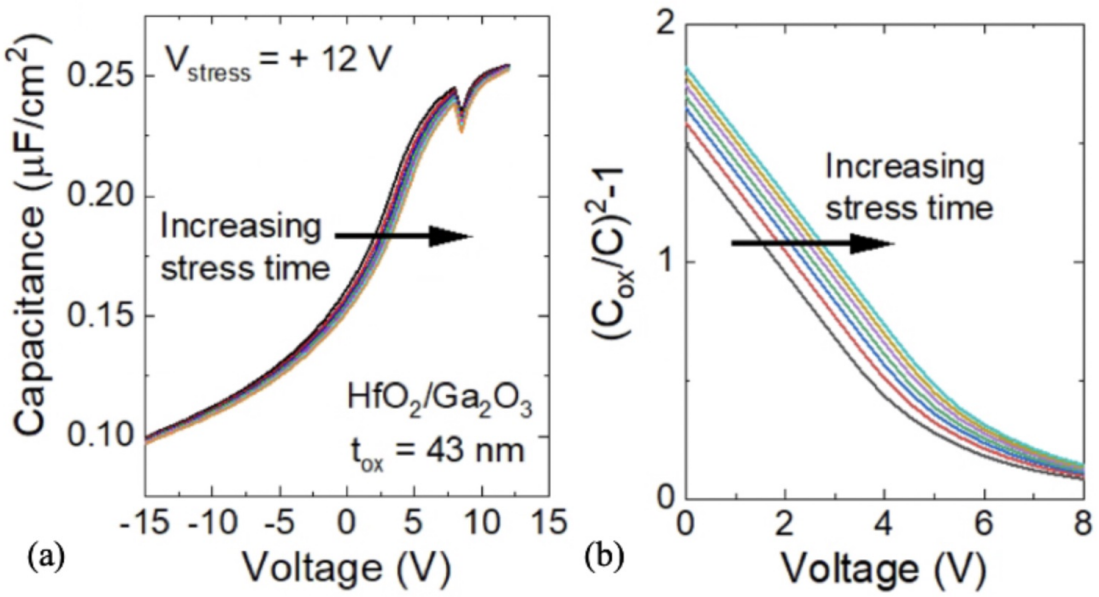


Figure 4.2: (a) High frequency *C-V* sweeps taken following positive constant voltage stress of HfO_2/β-Ga_2O_3 MOSCAPs. The dip in the *C-V* curves around 8 V is a measurement artifact due to auto-ranging of the LCR tool. (b) $(C_{ox}/C)^2$-1 versus voltage plots showing a positive shift in V_{fb} with increasing stress time. In both plots, the stress time varied from 100 s to 2000 s. The left-most traces indicate the stable *C-V* curve before bias stress was begun. From [10].

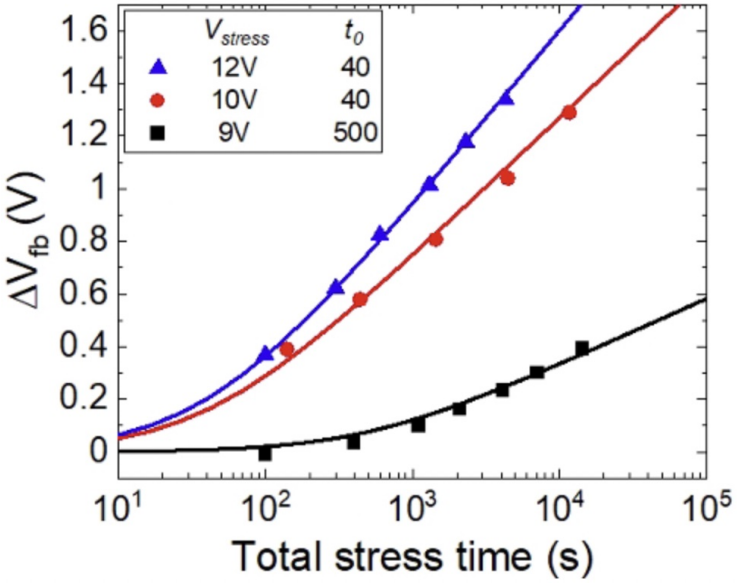


Figure 4.3: ΔV_{fb} versus cumulative stress time of HfO_2/β-Ga_2O_3 MOSCAPs under various V_{stress}. Symbols show experimental data and solid lines show fits to the White and Cricchi logarithmic model using the fitting parameter shown in the legend. The +9 V V_{stress} fit has a comparatively large time constant (t_0), which could indicate e-fields above a certain threshold are necessary to access traps and enable tunneling. From [10].

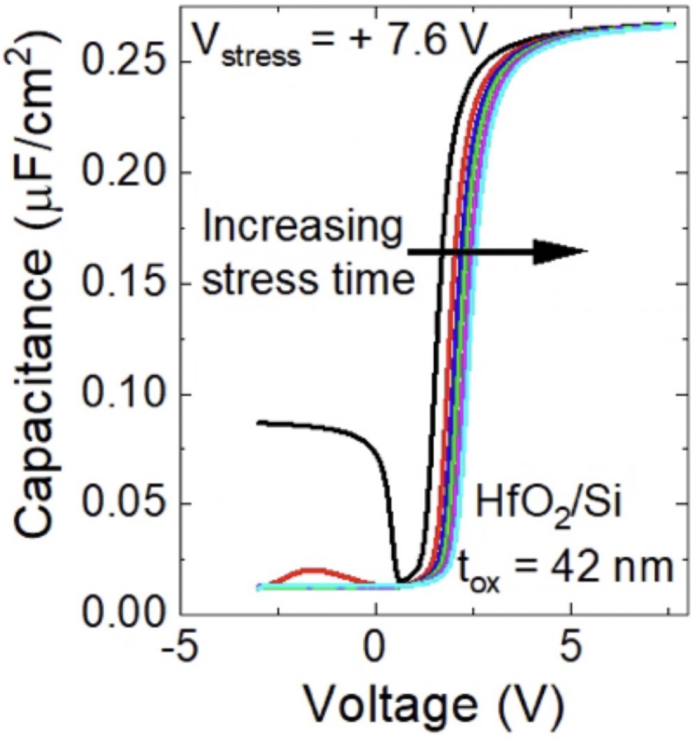


Figure 4.4: High frequency *C-V* results of positive bias stress testing of HfO_2/Si MOSCAPs with V_{stress} = +7.6 V (E_{stress} = 1.44 MV·cm^{-1}). Stress times varied from 100 s to 3000 s. The left-most trace indicates the stable *C-V* curve before bias stress was begun.

logarithmic time dependence of ΔV_{fb} is proportional to $ln(1 + t_{stress}/t_0)$, where t_0 is the time constant of the decay and t_{stress} is the cumulative stress time [78]. For V_{stress} of 10 V and 12 V, which correspond to E_{stress} of 1.23 MV·cm^{-1} and 1.41 MV·cm^{-1} respectively, a t_0 of 40 s provides a good fit to the data. When V_{stress} is 9 V, which equates to E_{stress} of 0.98 MV·cm^{-1}, the fit requires a much larger time constant, t_0, of 500 s. This may indicate the existence of a threshold e-field that is required for the electrons to access the traps and enable tunneling into the dielectric. These stress fields are approximately 2-3 times larger than the maximum electric fields applied to the gate in vertical β-Ga_2O_3 MOSFETs during normal operation [23].

In order to determine if the quantity of charge trapping is characteristic of the dielectric or is due to its relationship with the wide bandgap semiconductor, HfO_2/Si MOSCAPs were also stressed using the same method as the β-Ga_2O_3 devices. For the Si MOSCAPs, E_{stress} of $\sim$1.44 MV·cm^{-1} and $\sim$1.31 MV·cm^{-1} was applied, which corresponds to +7.6 V and +7 V stress bias, respectively.

Figure 4.4 shows the *C-V* curves due to +7.6 V stress. When compared to the β-Ga_2O_3 results for similar E_{stress}, the Si MOSCAPs show only a slight decrease in ΔV_{fb} (Figure 4.5). For a more apt comparison, the change in oxide charge density, ΔQ_{ox}, is calculated via

$$\Delta Q_{ox} = \frac{\Delta V_{fb} \times C_{ox}}{q}, \tag{4.1}$$

where q is the elementary charge. Figure 4.5 shows ΔQ_{ox} for both MOSCAPs with similar E_{stress}. The similarity in the β-Ga_2O_3 and the Si MOSCAP results indicates that the two structures experience a similar trapping mechanism during positive bias stress with relatively high E_{stress} of $\sim$1.4 MV·cm^{-1}. For lower E_{stress} (1.31 MV·cm^{-1} for Si and 1.23 MV·cm^{-1} for β-Ga_2O_3), the Si MOSCAP exhibits significantly less charge trapping. Thus, HfO_2/Si MOSCAPs require a higher electric field, compared to those on β-Ga_2O_3, to see the same level of charge trapping. This could be due to differences in the conduction band offsets between HfO_2 and the two semiconductors.

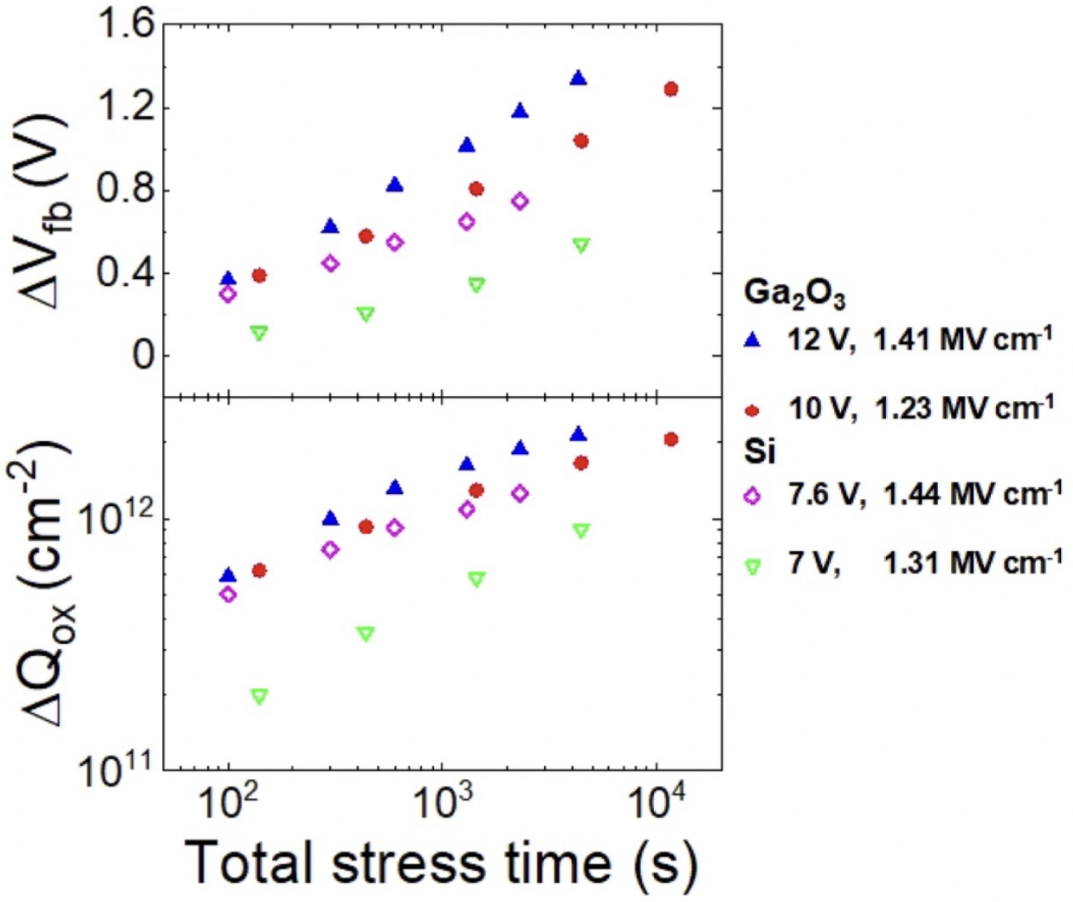


Figure 4.5: ΔV_{fb} and ΔQ_{ox} versus cumulative stress time of HfO_2/β-Ga_2O_3 and HfO_2/Si MOSCAPs under positive bias stress. The legend to the right gives the respective, V_{stress} , E_{stress} for each data set. The β-Ga_2O_3 data is the same as in Figure 4.3. From [10].

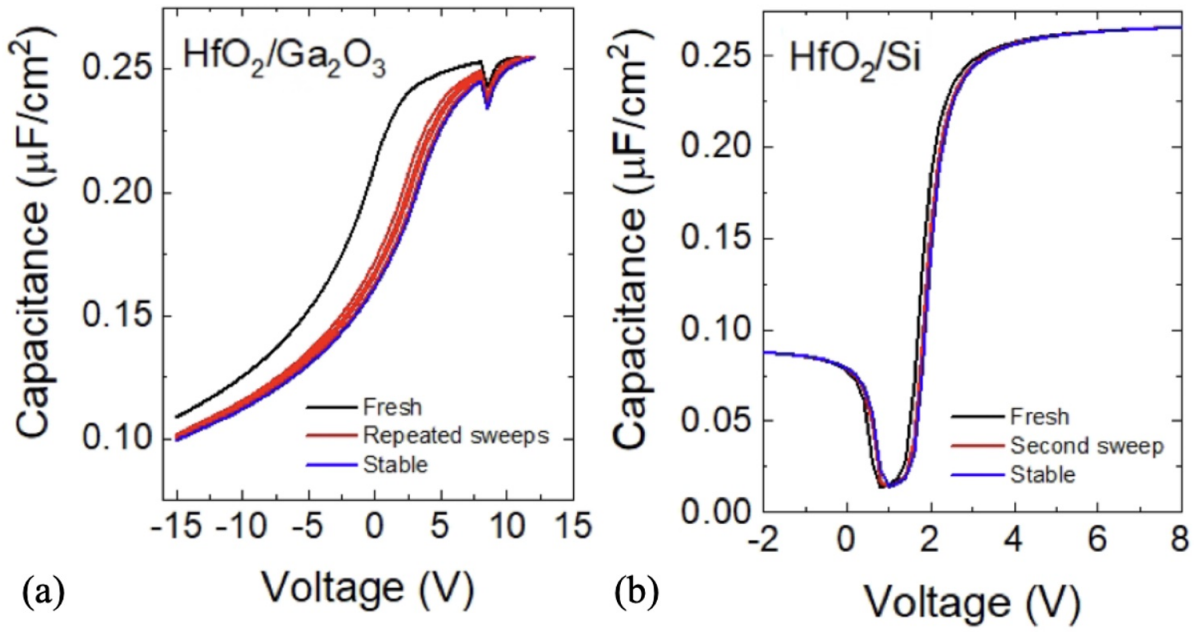


Figure 4.6: Initial *C-V* sweeps of (a) HfO_2/β-Ga_2O_3 and (b) HfO_2/Si MOSCAPs. (a) β-Ga_2O_3 MOSCAPs show significant positive ΔV_{fb} upon repeated *C-V* sweeps. (b) Si MOSCAPs only experience $\sim$0.1 ΔV_{fb} between "fresh" and "stable" *C-V* curves. From [10].

4.3.2 "Fresh" to "Stable" *C-V* Shifting

The most significant difference observed between the β-Ga_2O_3 and Si MOSCAPs is the shifting of the *C-V* curves from the "fresh" curve to the "stable" curve that occurs upon repeated *C-V* sweeps from depletion to accumulation before constant voltage stress is applied. As shown in Figure 4.6(a), there is a significant positive voltage shift in the β-Ga_2O_3 *C-V* curve from the first or "fresh" curve to the second curve, and the curves continue to shift to more positive voltages with repeated sweeps until a "stable" curve is obtained. For β-Ga_2O_3, the ΔV_{fb} between the "fresh" and "stable" *C-V* curves is $\sim$3.75 V, which equates to a ΔQ_{ox} of $\sim 6 \times 10^{12}$ cm^{-2}. In contrast, the Si MOSCAP shows a small positive shift of $\sim$ 0.1 V from the first to second sweep and negligible shifting with subsequent sweeps (Figure 4.6(b)).

The similarities in the stress results and differences in the initial *C-V* curve shifts between the MOSCAPs can best be explained by filling of border traps in the dielectric. Border traps – that is, charge traps that occur in the dielectric near the semiconductor interface – can significantly impact

the performance and reliability of MOS devices [46]. As a MOSCAP is biased into accumulation, electrons can easily be trapped in states at and near the dielectric interface. These traps have been used to explain *C-V* curve shifts observed in β-Ga_2O_3 MOSCAPs with bilayer stacks of Al_2O_3/HfO_2 and HfO_2/Al_2O_3 [54].

There are several possible physical explanations for the lower amount of charge trapping observed in the Si MOSCAPs during the initial *C-V* sweeps. One possibility is that electrons trapped in the Si MOSCAPs are more readily able to recombine with holes, due to the higher concentration and mobility of holes in Si compared to Ga_2O_3. Holes within β-Ga_2O_3 have been frequently described as self-trapped and mostly immobile [13]. Thus, holes in β-Ga_2O_3 may be unlikely to recombine with trapped electrons at and near the interface, whereas such recombination can readily occur in Si MOSCAPs. However during positive bias stress, electrons can move to deeper traps within the dielectric in both β-Ga_2O_3 and Si MOSCAPs. The recombination times of these trapped electrons would be very long even when holes are readily available in the substrate, causing similar stress-induced ΔV_{fb} in the two semiconductors. Another possibility is that the thin native oxide inevitably present on Si substrates could lower the concentration of border traps or provide a barrier to the injection of electrons into dielectric traps.

A possible physical explanation for the high quantity of border traps in the HfO_2 film on both β-Ga_2O_3 and Si could be structural morphology. It is known that thicker layers of ALD HfO_2 deposited on Si tend to be polycrystalline [79] and ALD HfO_2 on Ga_2O_3 can crystallize at a deposition temperature of 350°C, well below the anneal temperature of 500°C used in this work [80]. To determine the morphology of our HfO_2 layer, we performed x-ray diffraction on the HfO_2/Si piece and confirmed the presence of nanocrystalline ordering in the HfO_2 film, shown in Figure 4.7. A polycrystalline dielectric may have more defects, due to the presence of grain boundaries, compared to amorphous dielectrics such as SiO_2 [79]. These defects can facilitate the trapping of electrons during stress measurements, leading to the large positive ΔV_{fb}.

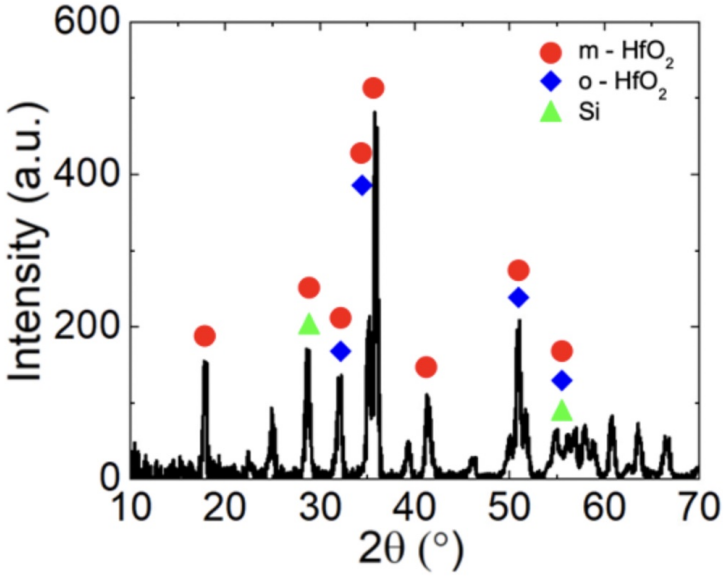


Figure 4.7: XRD results of ALD HfO_2 on Si showing crystallization peaks. Symbols indicate peaks from monoclinic – HfO_2 (ICSD - 27313), orthorhombic – HfO_2 (ICSD - 87457), and Si (ICSD – 29287). From [10].

4.3.3 Recovery of Stress-Induced Charge Trapping with DUV Illumination

In other MOSCAPs, photo-illumination with photon energy greater than the bandgap can generate electron-hole pairs that facilitate recovery of stress-induced flat band voltage shifts. For example, GaN vertical finFETs saw expedited recovery from positive bias stress when UV-light was applied along with 0 V bias [81]. Here, I investigated the recovery of stress-induced trapped charge in HfO_2 MOSCAPs using DUV illumination. First, a bias stress of +11 V and +8 V was applied to the β-Ga_2O_3 and Si MOSCAPs, respectively. The MOSCAPs were biased at this positive voltage for 300 s and then biased at 0 V for 300 s, in the dark. *C-V* sweeps were taken before and after each step. Both MOSCAPs experienced a right-ward shift in their *C-V* curves from the positive bias stress. No further changes were observed in V_{fb} after the 0 V bias in the dark, indicating that 0 V bias alone is insufficient to remove trapped electrons.

Next, a second 300 s positive bias stress was performed on the MOSCAPs. The resulting *C-V* curves are shown in figures 4.8 (a) and (b) as the "After Stress" curve. A second 0 V, 300 s recovery bias was then performed, this time with the addition of DUV illumination, followed by

C-V measurement of the "After 0 V + DUV" curve. The Si MOSCAP *C-V* curve shifted slightly to the left after the recovery bias with DUV, but the MOSCAP did not return to its "stable" V_{fb} value (Figure 4.8 (b)). In contrast, the β-Ga_2O_3 MOSCAP saw a significant V_{fb} shift to the left after the illuminated recovery bias, so that the "After 0V + DUV" curve is very similar to the "fresh" *C-V* curve (Figure 4.8 (a)). Finally, on the β-Ga_2O_3 MOSCAP, an additional *C-V* sweep was taken immediately following the "After 0 V + DUV" curve. This last sweep closely matches the "Stable" *C-V* trace (Figure 4.8 (a)). In sum, this recovery experiment shows that the HfO_2/β-Ga_2O_3 MOSCAP can fully recover quickly from positive bias stress with the use of DUV illumination.

The nearly complete recovery of β-Ga_2O_3 MOSCAPs with 300 s 0 V bias + DUV illumination, compared to Si MOSCAPs, is possibly due to differences in energy band alignment. HfO_2 exhibits a type-II band alignment with β-Ga_2O_3 (Figure 4.9(a)) [13]. Due to the negative valence band offset, ΔE_V, of 0.5 eV [7], there is no barrier for the transport of photo-generated holes from

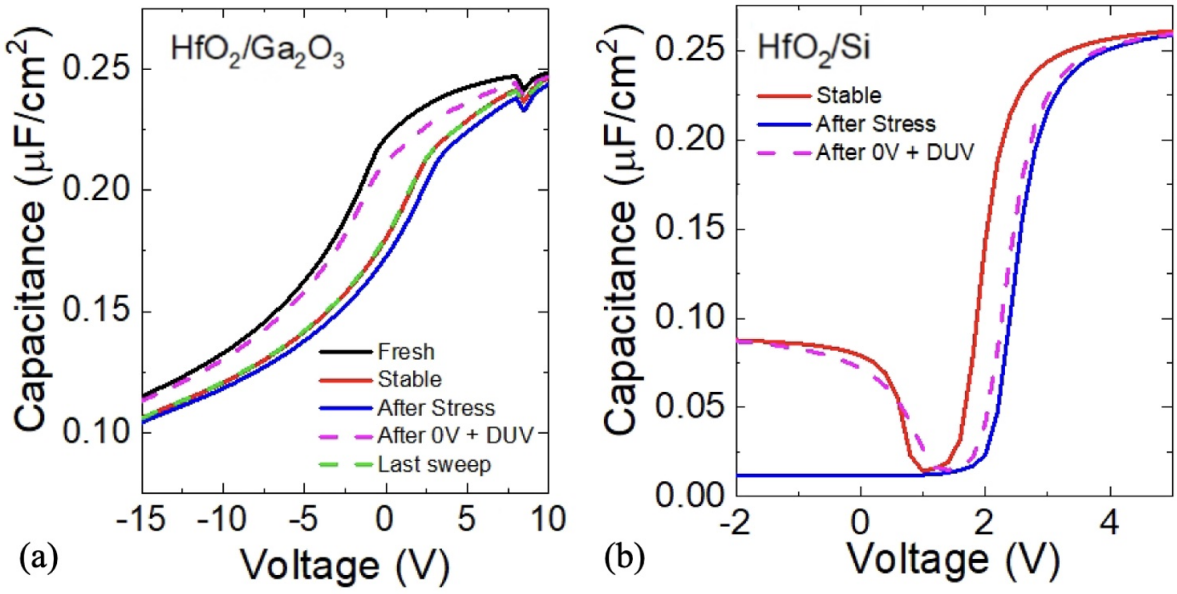


Figure 4.8: Recovery *C-V* results of (a) HfO_2/β-Ga_2O_3 and (b) HfO_2/Si MOSCAPs. Both MOSCAPs were biased positively at 11 V and 8 V, respectively, for two periods of 300 s each. During recovery, the MOSCAPs were biased at 0 V for 300 s. In the dark, no recovery or shifting of the *C-V* curves, was observed. After recovery with 300 s DUV illumination and 0 V, the β-Ga_2O_3 MOSCAP experienced much more significant recovery ($-\Delta V_{fb}$) compared to the Si MOSCAP. From [10].

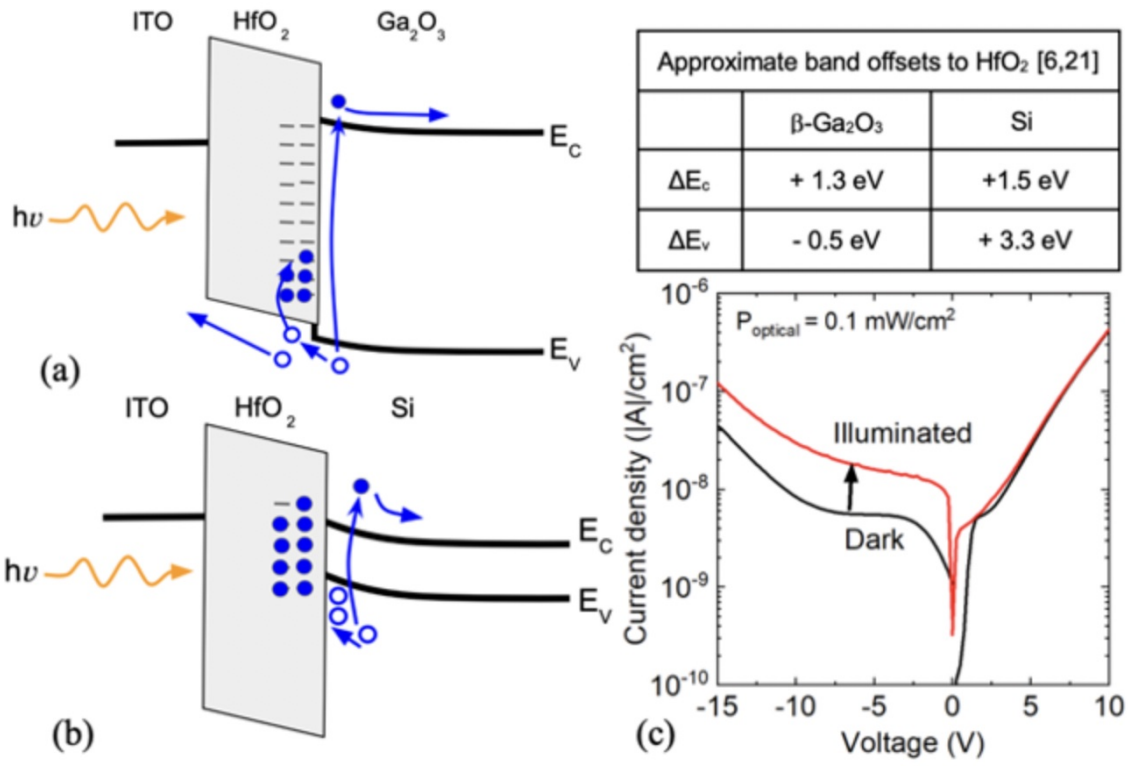


Figure 4.9: Band diagrams of (a) HfO_2/β-Ga_2O_3, and (b) HfO_2/Si under depletion bias and illumination. The type-II band alignment of β-Ga_2O_3 with HfO_2 allows the movement of photo generated holes, which can lead to photo-current and recombination with trapped electrons. (c) Table of approximate band offsets for both β-Ga_2O_3 and Si to HfO_2 and plot showing photo current of HfO_2/β-Ga_2O_3 MOSCAPs during DUV illumination at 265 nm. From [10].

the substrate to the dielectric and ITO contact. These photo-generated holes can recombine with the electrons that were trapped in border states during positive bias stress, as shown in Figure 4.9(a). In contrast, HfO_2 forms a type-I band alignment to silicon [82]. The positive valence band offset impedes the movement of photo-generated holes into the dielectric, causing the recovery process to be much slower (Figure 4.9(b)). Others have recently attributed the DUV-assisted recovery of Al_2O_3/β-Ga_2O_3 finFETs to the photo-excitation of trapped electrons at the oxide-semiconductor interface [83]. While the photo-excitation of trapped electrons could contribute to recovery in our MOSCAPs, the lack of evidence for this process in our Si MOSCAPs lead us to surmise that photo-generated holes at the type-II band interface dominate the recovery process in our HfO_2/Ga_2O_3

MOSCAPs. In addition to providing a pathway to V_{fb} recovery, the type-II band alignment of HfO_2/β-Ga_2O_3 leads to significant photo-current when the MOSCAP is illuminated with DUV while biased in depletion (Figure 4.9(c)). The HfO_2/β-Ga_2O_3 MOSCAP displays non-symmetric *J-V* behavior. At positive bias, the leakage current is attributed to accumulated electrons moving through the dielectric via trap states. At negative bias, leakage current is limited due to the small concentration of mobile holes. Illumination or a large negative bias generates excess holes, causing a significant increase in leakage. Similar *J-V* behavior and reverse bias photo-current have been observed in other dielectrics with type-II band alignment to β-Ga_2O_3 [6].

Based on these results, ALD HfO_2, in its present state, does not form a reliable dielectric for β-Ga_2O_3 power MOSFETs. The charge trapping that occurs upon initial bias sweeps and during positive bias stress could lead to threshold voltage shifts and early breakdown of the MOSFETs. To obtain a dielectric film that is more robust against positive bias stress, it may be desirable to use a thinner, amorphous HfO_2 film, or to optimize the ALD recipe and substrate preparation steps to reduce defects in the HfO_2 film near its interface with β-Ga_2O_3 [84]. Another possible solution would be to deposit a thin layer of SiO_2, or another dielectric with a large positive valence band offset, before HfO_2 deposition, to act as a barrier to charge trapping. Such a SiO_2/HfO_2 dielectric stack would benefit from the larger band offsets of the SiO_2 as well as from the high-κ of the HfO_2.

4.4 Conclusion

In this chapter, I fabricated and tested HfO_2/β-Ga_2O_3 (010) MOSCAPs to evaluate their reliability under positive bias stress. The HfO_2 MOSCAPs showed positive shifts in V_{fb} due to electron trapping during stress under various electric fields, which can be fitted to the White and Cricchi logarithmic time-dependent model. HfO_2/Si MOSCAPs were also tested for their reliability in order to determine the significance of the WBG semiconductor on charge trapping. The comparison indicated MOS structures with WBG semiconductors are more susceptible to charge trapping at lower electric fields.

In addition to during positive bias stress, the β-Ga_2O_3 MOSCAPs experienced significant charge trapping, or + ΔV_{fb}, during repeated *C-V* sweeps from "fresh" to "stable" measurements. Si MOSCAPs showed negligible shifting with repeated sweeps. This difference is attributed to the filling of interface and border traps, which cannot be emptied solely with a depletion bias in the β-Ga_2O_3 case due to the lack of mobile holes. In contrast, the Si MOSCAPs can fill and empty these traps relatively quickly during the *C-V* sweeps with the help of inversion.

Another difference observed between the β-Ga_2O_3 and Si MOSCAPs is the fast recovery under DUV illumination seen in β-Ga_2O_3. HfO_2/β-Ga_2O_3 MOSCAPs were able to fully recovery from the stress-induced charge trapping after 5 min of 0V bias + DUV due to the electron-hole pair generation and the type-II band alignment. HfO_2/Si MOSCAPs experienced only partial recovery under the same conditions; the positive ΔE_V impeded the photo-generated holes from recombining with the trapped electrons in the dielectric. The type-II band alignment in the HfO_2/β-Ga_2O_3 MOSCAPs also likely contributed to the photo-current observed in depletion.

Based on these results, the film quality of the HfO_2 needs to be improved to achieve a more reliable high-κ dielectric film for future high-voltage, high-power β-Ga_2O_3 MOS-based devices. This chapter, also, highlights the importance of investigating the reliability of MOS structures on WBG semiconductors as charge trapping and emission behavior varies due to band alignment and hole-generation differences. These results also show the possibility of recovery from stress with DUV illumination, which could be very beneficial for future β-Ga_2O_3 power MOSFETs. These techniques of investigating reliability and recovery can be implemented in future interface studies of non-planar β-Ga_2O_3 MOS structures.

CHAPTER 5

Effects of High Temperature Annealing on the ALD HfO_2/β-Ga_2O_3 (010) interface

5.1 Introduction

In previous chapters, I have investigated the interface quality and stress reliability of dielectrics with the WBG semiconductor, β-Ga_2O_3, with most of our focus being on ALD HfO_2/ β-Ga_2O_3 MOS structures. Many researchers have instead focused on using ALD Al_2O_3 as the gate dielectric in their β-Ga_2O_3 MOS devices. Al_2O_3 does have many benefits, making this dielectric useful for β-Ga_2O_3 devices, including its high dielectric constant, and a large bandgap which provides a large conduction band offset and a positive valence band offset to β-Ga_2O_3. On the other hand, there have been many studies that indicate a stability issue with the Al_2O_3/β-Ga_2O_3 interface, especially under high temperatures [11, 38, 44], which makes Al_2O_3 possibly an inadequate option for β-Ga_2O_3 power MOSFETs.

5.1.1 Why MOS stability under high temperatures is necessary

The MOS gate structure is critical for all MOSFETs as it controls the switch behavior. Any changes occurring in this structure, especially at the interface of the dielectric and semiconductor, can affect the performance and stability of the device. Electrical stress can be one of the causes of a changing MOS structure as I have shown in the HfO_2/β-Ga_2O_3 MOSCAPs in the last chapter.

Charge trapping due to electrical stress resulted in flatband voltage shifts which equates to a shifting threshold voltage in a device [10]. Another cause of MOS instability can be thermal stress. Thermal stress can have a similar impact on the electrical behavior of the MOS structure causing changes in oxide and interface traps, as well as, fostering leakage paths through dielectric crystallization, which can lead to threshold voltage instability and premature breakdown. Thermal stress can occur during the lifetime of the device due to increased operating temperatures (<250°C) which high power devices must be able to withstand [85]; the MOS stability at these temperatures will not be investigated in this chapter. Thermal stress could also occur during the fabrication process of these MOS devices as there are many processes that require temperatures higher than 250°C (e.g. post-metalization annealing, epilayer regrowth, and ion-implant activation/annealing). Device researcher must be aware of how these high temperature processes impact the MOS behavior.

5.1.2 Evidence of Al and Ga interdiffusion at high temperatures

The unstable Al_2O_3/β-Ga_2O_3 interface is apparent through several post-deposition annealing (PDA) reports. Jayawardena, et al., analyzed the interface trap density (D_{it}) of ALD Al_2O_3 on ($\bar{2}01$) β-Ga_2O_3 with a 2-min 500ºC anneal and without any annealing processes. In both N_2 and forming gas (FG) annealing environments, D_{it}, extracted by the high-low capacitance - voltage (*C-V*) method and the photo-assisted *C-V* method, increased [38]. In another study, Zhou, et al., saw a reduction in D_{it} with a 2-min 500ºC anneal in both N_2 and O_2 annealing environments, but increasing the annealing temperature to 600, 700 and 800ºC degraded the interface after only one minute of annealing [44]. Similarly, Hirose et al., showed that D_{it} increased by a factor of $\sim$5 - 6 following a 5-min, N_2 anneal at 600ºC to 700ºC [11]. The increase in D_{it} is attributed to structural changes occurring at the interface, likely the inter-diffusion of the Al and Ga atoms creating a mixed phase of β-$Al_xGa_{(2-x)}O_3$, where $0 \leq x \leq 2$ [38]. Increasing interfacial defects from a relatively short annealing process causes concern of a degrading interface under device operation limiting the lifetime of the device.

The inter-diffusion of Al and Ga atoms in these oxide stacks has been shown using secondary

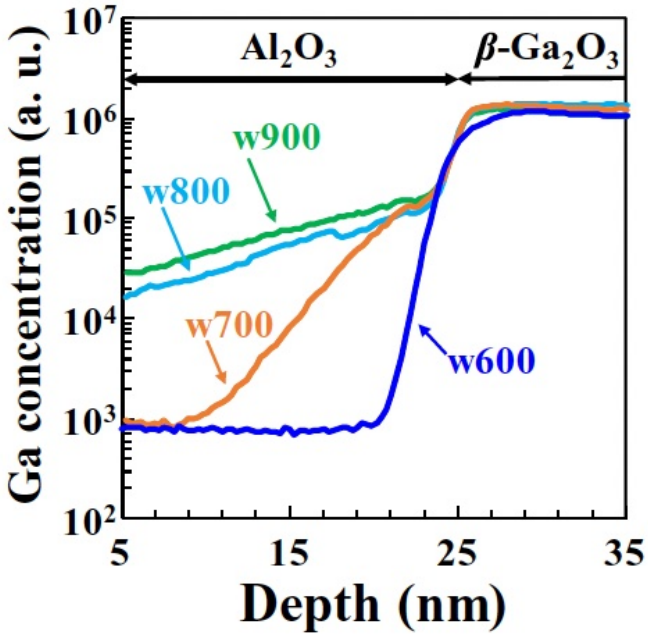


Figure 5.1: Ga depth profile in Al_2O_3 films after PDA of 600-900°C. Reprinted from Microelectronic Engineering, Vol 216, Hirose, *et al.*, "Influence of post-deposition annealing on characteristics of Pt/Al_2O_3/β-Ga_2O_3 MOS capacitors", 111040, Copyright (2019), with permission from Elsevier [11].

ion mass spectrometry (SIMS) depth profile. SIMS was performed on annealed and "as-deposited" pulsed-laser deposited (PLD) β-Ga_2O_3 films on sapphire (Al_2O_3) substrates. Anneals were performed for 24 hours at various temperatures, and SIMS results from the 800ºC annealed sample showed significant Al atom intensities at the surface of the sample, $\sim$1.5 μm from the interface [49]. In addition to showing electrical *C-V* data on annealed samples, Hirose, et al. examined the Ga-diffusion through SIMS depth profile on ALD Al_2O_3/β-Ga_2O_3 stacks [11]. After 700ºC for PDA, the SIMS depth profile (Figure 5.1) showed significant Ga atom intensities in the Al_2O_3 layer up to $\sim$10 nm from the interface; this Ga concentration increased with increasing PDA temperature [11]. Cross-sectional transmission electron microscope (TEM) images showed crystallization of the Al_2O_3 films starting at 700ºC. It is believed that the Ga atom diffusion process into the Al_2O_3 film is caused by the solid-solution reaction and not the decomposition of β-Ga_2O_3, which requires a temperature of 1150ºC [11]. In the previous study, a right shift in the x-ray diffraction indicated Al atoms from the sapphire substrate substituted on Ga sites in the PLD Ga_2O_3 layer [49].

Oxide	Standard molar Gibbs energy of formation at 298.15 K (kJ/mol)	Crystal ionic radii (pm) (6-coordinate)
Ga_2O_3	-998.3	76
Al_2O_3	-1,582.30	67.5
HfO_2	-1,027.2	85
SiO_2	-856.3	54

Table 5.1: Gibbs energy of formation and the crystal ionic radii of various oxides including Ga_2O_3 and frequently used dielectrics.

5.1.3 HfO_2 material properties and potential benefits to thermal stability with β-Ga_2O_3

The previously mentioned studies show clear evidence that the interface of ALD Al_2O_3/ β-Ga_2O_3 is not stable at elevated temperatures. Based on the Gibbs energy of formation (shown in Table 5.1), Al_2O_3 forms much more easily compared to Ga_2O_3 [86]. Al atoms could be taking O atoms from the Ga_2O_3 substrate leaving Ga atoms free to move into the Al_2O_3; this would create the mixed phase of β-$Al_xGa_{(2-x)}O_3$, where $0 \leq x \leq 2$. HfO_2 could provide a better barrier to impede interdiffusion with Ga_2O_3 and should be investigated for the impact of high temperature processing on the MOS structure similar to the studies on Al_2O_3. The reasoning behind the interest in HfO_2 includes the thermodynamic properties of this dielectric. HfO_2 has a more similar Gibbs energy of formation as Ga_2O_3 [86], which might lead to less competition over the O atoms and hence, less diffusion. Another possible benefit of HfO_2 is the ionic radius of Hf is larger than Ga (Table 5.1); Al's ionic radius is less than Ga possibly assisting the diffusion of Al atoms into the Ga_2O_3 substrate [87]. On the other hand, HfO_2 is known to crystallize at relatively low temperatures ($<$500°C) [88, 89], which may negatively affect the insulator properties.

In this chapter, I investigate the impact of high temperature annealing processes on the ALD HfO_2/β-Ga_2O_3 interface using various material analyses and electrical techniques. SIMS depth profile was performed on several HfO_2/β-Ga_2O_3 samples with various annealing conditions to determine at which temperature Ga-diffusion into the HfO_2 layer occurs. Note: only Ga diffusion into the dielectric layer is considered within this study. Hf atoms may be diffusing into the β-Ga_2O_3

substrate, but due to the nature of re-sputtering within the ion mill, it is difficult to conclude any differences among the decreasing Hf-signals in the SIMS analysis. Grazing incidence X-ray diffraction (GIXRD) was used to determine the crystal morphology of the HfO_2 layer deposited on β-Ga_2O_3, and how it changes with high temperature annealing. The changes in material properties of the dielectric and its interface to the semiconductor is then compared to the electrical properties, including leakage current and interface traps densities (D_{it}), of the MOS structure through MOSCAP analysis. This analysis will be necessary for device researchers to consider when choosing a dielectric and while developing the fabrication process for future stable β-Ga_2O_3 power MOSFETs.

5.2 Experimental Methods

Sn-doped β-Ga_2O_3 (010) substrates from Tamura Corporation were used in this study. Diced substrates were cleaned with solvents, then treated with UV/O_3 for 20 minutes. Approximately 22 nm of HfO_2 was then deposited on the samples using a Veeco Fiji ALD at 200ºC with tetrakis(dimethylamido)hafnium (TDMAH) and H_2O using the recipe parameters previously reported [10]. Samples were annealed in a N_2 environment at various temperatures using a Jetfirst 150 Rapid Thermal Process. Two samples were not annealed in order to characterize the "as-deposited" properties. HfO_2 thickness was measured with a JA Woollam M-2000 Ellipsometer.

To characterize the atomic diffusion and crystal structure, I performed SIMS depth profile using a Nanoquest II Ion Mill and GIXRD using a Rigaku Smartlab XRD. SIMS was performed by ion mill etching for 6-8 minutes using a beam voltage of 300 V and beam current of 320 mA. The Ga atom intensities were recorded throughout the etch. Selected samples were processed to make MOSCAPs for electrical analysis. Following the ALD HfO_2 and post deposition annealing as earlier described, the backside ohmic contact was formed with a 5-min ion mill etch prior to electron beam evaporation of Ti/Au (20 nm/ 230 nm). A 100-nm layer of indium tin oxide (ITO) was sputtered and patterned to form top contacts. A transparent conductor was chosen for the top

contact to facilitate photo-illumination experiments following [6]. The MOSCAP samples were next annealed for one minute in N_2 at 470ºC to improve the ohmic contact [27] and then annealed for five minutes in forming gas at 450ºC to improve the conductivity of the ITO contact [64]. These MOSCAP samples are referred to as "As-prepared." GIXRD was performed on unpatterned ALD HfO_2/β-Ga_2O_3 (010) samples with similar annealing conditions to those used for the MOSCAPs.

All electrical measurements were taken in the dark at room temperature. Capacitance – voltage (C-V) measurements were taken with an HP4284A LCR meter using a sweep rate of 1 V s^{-1} and an AC voltage amplitude of 50 mV, using the parallel capacitance – parallel resistance circuit model. C-V sweeps were taken with voltage swept from depletion (-V) to accumulation (+V) at a frequency of 1 MHz, unless otherwise stated. Continuous current – voltage (J-V) measurements were taken with an HP4156A semiconductor parameter analyzer using long integration time.

5.3 Results and Discussion

5.3.1 Ga-diffusion into Al_2O_3 preliminary experiment

In order to verify our ability to observe Ga-diffusion into the dielectric layer using the Nanoquest II Ion Mill/SIMS tool at the Laurie Nanofabrication Facility (LNF), I performed an initial test on an ALD Al_2O_3/β-Ga_2O_3 stack, following Hirose's procedure [11]. For this test, approximately 20 nm of Al_2O_3 was deposited at 150°C using trimethylaluminum (TMA) and H_2O as the precursors onto Sn-doped β-Ga_2O_3 (010) samples. One sample was left "As-deposited" to use as a control; the other sample was annealed at 900°C for 10 minutes in N_2 environment, which based on Hirose's results [11] would cause significant Ga-diffusion into the Al_2O_3 layer.

The results of the Al_2O_3 SIMS experiment are shown in Figure 5.2. For each data set, including the data included in Figure 5.2(a), the intensity is normalized to the maximum Ga count. The SIMS data is acquired as a function of sputtering time. To convert sputtering time to depth, the

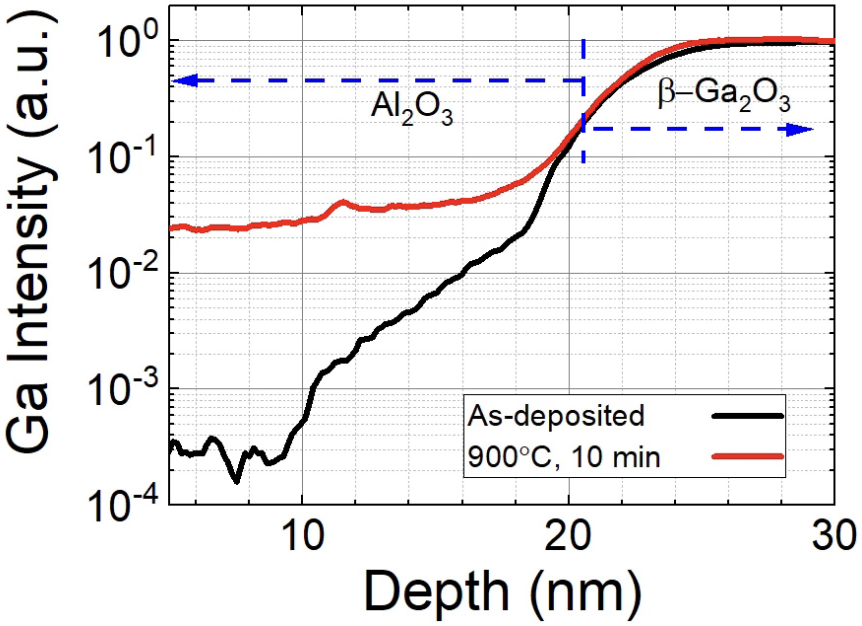


Figure 5.2: Ga depth profiles in Al_2O_3 as deposited (black) and after 10-min anneal in N_2 at 900ºC (red).

following equation was used:

$$Depth = \frac{Sputtering\ time}{Time\ at\ normalized\ Ga\ intensity\ of\ 0.2} \times t_{dielectric}, \tag{5.1}$$

where $t_{\text{dielectric}}$ is the thickness of the Al_2O_3 (or HfO_2 layer in the case of 5.2(a)) measured by ellipsometry. In addition, the curves have been shifted horizontally to align the points at which the Ga normalized intensity is 0.2, to allow for better comparison between samples. This point is chosen to indicate the approximate location of the interface, as labelled in Figure 5.2 and 5.3(a). Due to differences in sputter etch rates between Al_2O_3, HfO_2 and β-Ga_2O_3, the depth values within the substrate (i.e., depths $>$ 21 nm for Figure 5.2 and 24 nm for Figure 5.3(a)) may not be fully accurate.

The Ga depth profile of the As-deposited Al_2O_3/β-Ga_2O_3 sample showed a significant Ga intensity within the Al_2O_3 layer almost 10 nm away from the interface. This result may indicate that some out-diffusion of Ga into the dielectric does not require elevated annealing temperatures, though

more experiments would be required to confirm that theory. The motivation of this experiment was to confirm the ability to observe Ga-diffusion out of the substrate into the dielectric layer with the LNF's SIMS, and that was verified with the sample annealed at 900°C. While the As-deposited sample showed a Ga intensity at the noise level (<0.002) during the top 10 nm of the etch, the 900°C sample showed a Ga intensity above 0.02 throughout the Al_2O_3 layer indicating significant diffusion of Ga atoms has occurred during the 900°C anneal.

5.3.2 Impact of Ga-diffusion on HfO_2 material properties

Figure 5.3(a) shows the Ga intensity depth profile obtained from SIMS for the HfO_2 samples. The as-deposited trace in Figure 5.3(a) shows a sharp increase in the Ga intensity over <5 nm as the etch moves across the HfO_2/β-Ga_2O_3 interface; this slope from the Ga signal is due the depth resolution limit of the measurement and not necessarily indicating a diffused interface. The Ga profile does not change significantly for anneals up to 850ºC for 10 min. This indicates that minimal Ga diffusion into the dielectric layer occurs during these thermal treatments. In contrast, following a 900ºC anneal, the Ga depth profiles indicate significant diffusion of Ga into the HfO_2 layer. The distance in the HfO_2 across which the normalized Ga intensity falls from 0.2 to 0.002 is used as a metric to compare Ga out-diffusion between samples. For the as-deposited sample, this distance is $\sim$ 4.8 nm. After a 5-min anneal at 900ºC, that distance increases to $\sim$ 8.0 nm, and after a 10-min anneal at 900ºC, it further increases to $\sim$ 15.5 nm. Clearly, 900ºC anneals result in significant blurring of the HfO_2/β-Ga_2O_3 interface.

In Figure 5.3(b), the 900ºC Ga depth profiles within the HfO_2 layer were fit using the standard solution to the diffusion equation assuming a constant source [90],

$$Ga\ intensity(x) \sim \left[erfc\frac{x}{2\sqrt{Dt}}\right], \tag{5.2}$$

where *D* is the diffusion coefficient of Ga atoms in HfO_2, *t* is the time of the anneal, *x* is the depth into the dielectric, and erfc is the complementary error function. For an anneal temperature of

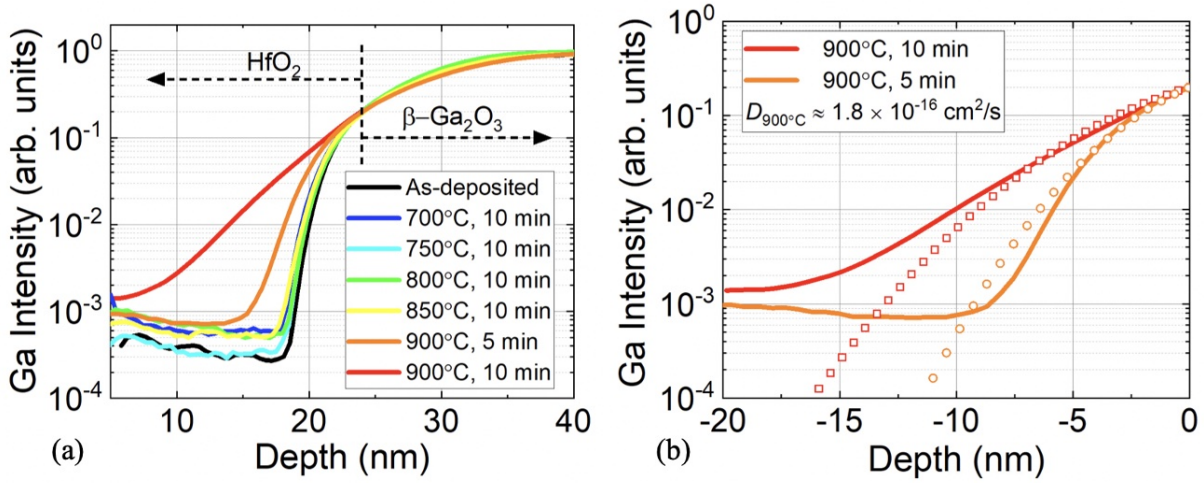


Figure 5.3: (a) SIMS Ga atom depth profiles within ALD HfO_2/β-Ga_2O_3 stacks. For each profile, the Ga intensity was normalized to the maximum Ga atom count. The interface was defined to be at a normalized Ga intensity of 0.2. (b) SIMS Ga atom profiles for 5-min and 10-min 900ºC anneals, fit using the Eq. (2), the diffusion equation solution assuming a constant source. Ga intensity below 10^{-3} is experimental noise due to the limit of the SIMS measurement. From [12].

900ºC, D is found to be $\sim 1.8 \times 10^{-16}$ cm^2/s. For comparison, this is approximately an order of magnitude less than the diffusion coefficient of boron within HfO_2 at the same temperature [91], as expected given Ga's larger atom radius. These results indicate that 900ºC anneals significantly change the composition of the HfO_2 dielectric interfacial layer. Since such anneals are frequently used for post-ion implant activation [92], the large interfacial region resulting from Ga out-diffusion will restrict the minimum HfO_2 thickness allowed for future MOS devices.

The impact of the interdiffusion at 900ºC on the crystal morphology of HfO_2 was then investigated using GIXRD. It is well known that HfO_2 tends to crystallize at relatively low temperatures of $<$ 500ºC [88, 89], and polycrystalline HfO_2 was intentional deposited on β-Ga_2O_3 using ALD at the elevated temperature of 350 ºC [80]. In contrast, reports have shown the crystallization of Al_2O_3 occurs at higher temperatures >600 ºC [11, 93, 94]. The GIXRD data for the as-deposited HfO_2 sample, shown in Figure 5.4, displays a broad peak, indicating the ALD HfO_2 film is amorphous when deposited on β-Ga_2O_3. Following the low-temperature anneal processes ($<$ 500ºC) used for the MOSCAP fabrication (i.e., the as-prepared sample), the HfO_2 film exhibits nanocrystalline ordering. The 700ºC- and 900ºC-annealed samples display very similar XRD patterns, which match

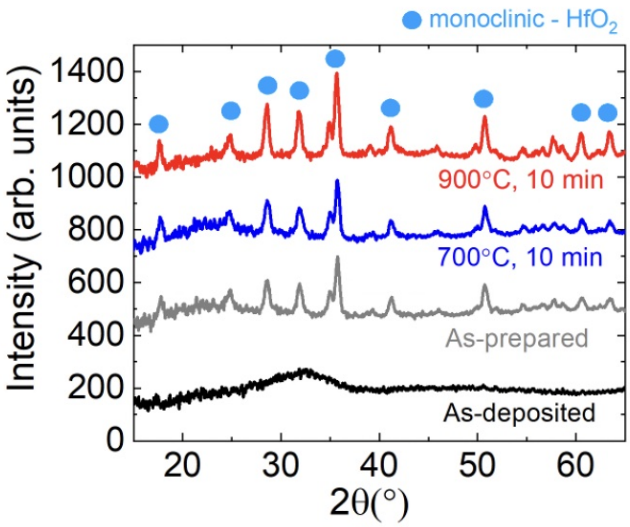


Figure 5.4: GIXRD of HfO_2 films deposited on β-Ga_2O_3, annealed at various temperatures. The as-prepared sample was subjected to a 470ºC, 1-min anneal in N*2* to improve the Ti/Au ohmic contact and a 450ºC, 5-min anneal in forming gas to reduce the ITO electrode resistance. Symbols indicate peaks from monoclinic HfO_2 (ICSD 27313). From [12].

well with the expected peaks from monoclinic HfO_2 films (ICSD 27313). The average crystallite diameter ranges from 13 nm to 18 nm based on the Scherrer equation [88]. It is interesting that while the sample annealed at 900ºC showed significant Ga out-diffusion, the HfO_2 layer does not exhibit a phase change or significant increase in crystallite diameter. Nonetheless, the grains boundaries in crystallized films may act as current leakage paths, which would result in poor insulator behavior [95].

5.3.3 Electrical impact on MOS structure

To assess electrical leakage, *J-V* measurements (Figure 5.5(a)) were taken for the HfO_2/β-Ga_2O_3 MOSCAPs. The as-prepared MOSCAPs showed low leakage ($<$ 20 nA/cm2) for both forward (+V) and reverse bias (-V) despite showing nanocrystalline ordering in GIXRD. The 700ºC-annealed MOSCAPs also exhibited low leakage in reverse bias, but have significantly higher leakage ($\sim$10 μA/cm^2) in forward bias compared to the as-prepared MOSCAPs. As described in reference [10], the reverse bias leakage may be limited due to a small concentration of mobile

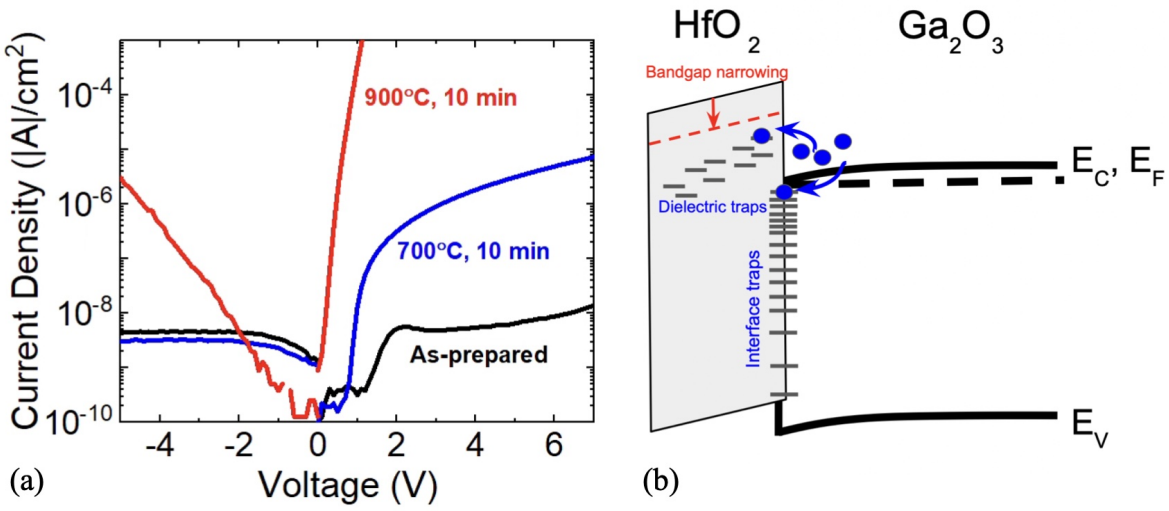


Figure 5.5: (a) Continuous *J-V* measurements of the MOSCAP samples. (b) Band diagram of HfO_2/ β-Ga_2O_3 in accumulation showing electrons moving into dielectric and interface traps. Also illustrated is the possibility of bandgap narrowing of HfO_2 due to Ga incorporation upon 900 ºC anneal. From [12].

holes within the substrate, which is not impacted by the annealing process. The higher leakage in the 700ºC-annealed MOSCAPs in forward bias could be attributable to changes in the grain boundaries or crystal structure not observable in GIXRD and/or changes in dielectric traps which would facilitate electron transport, as shown in the band diagram in Figure 5.5(b).

The dielectric in the 900ºC-annealed MOSCAPs exhibits extremely high leakage in both forward and reverse bias. Under forward bias, leakage quickly rises to 1 mA/cm^2 showing repeatable non-destructive breakdown. This significant increase in leakage could be caused by narrowing of the HfO_2 bandgap [88, 96] and subsequent lowering of the conduction band offset, potentially causing dielectric traps levels to become more accessible to electron transport (Figure 5.5(b)). A reduction in HfO_2 bandgap is likely the result of the Ga-incorporation into the HfO_2 layer creating a mixed HfO_2-Ga_2O_3 interfacial layer [96]. Bandgap narrowing of the HfO_2 could also be contributing to the higher forward bias leakage in the 700 ºC-annealed MOSCAP, but the lack of evidence of Ga-diffusion in the SIMS results does not strongly support that conclusion. Overall, these results indicate that HfO_2 dielectric films on β-Ga_2O_3 that have been subjected high-temperature anneals

can no longer provide adequate electrical insulation.

To quantitatively determine how dielectric traps vary with anneal conditions, *C-V* measurements at various frequencies were taken on the MOSCAPs. The results are shown in figures 5.5(a) and (b). The *C-V* behavior of the as-prepared and the 700ºC-annealed samples are similar, with frequency dispersion observed in the accumulation region. Such dispersion is typically associated with interface traps and dielectric border traps [97, 98]; optimization of the surface preparation and ALD HfO_2 deposition process will be necessary to minimize such defects in future β-Ga_2O_3 devices. The 700ºC-annealed sample has a larger flatband voltage (V_{fb}) of 4.5 V, determined by the *x*-intercept of the extrapolated line from the $(C_{ox}/C)^2$-1 versus *V* data, presumably resulting from a higher quantity of dielectric traps (D_{ox}) of 10 $\times 10^{12}$ cm^{-2} compared to the as-prepared MOSCAPs (V_{fb} = 3.5 V and $D_{ox} = 8.5 \times 10^{12}$ cm^{-2}). Figures 5.6 (c) and (d) show the *C-V* results from the 900ºC-annealed (10 min) MOSCAP sample which has non-negligible Ga out-diffusion. Significant frequency dispersion was observed in this sample, as highlighted by the log-scale *C* values in Figure 5.6 (c). In addition, at a frequency of 1 MHz (Figure 5.6 (d)) the MOSCAP showed very low *C* values and was not able to fully accumulate before breaking down. This further supports the conclusion drawn from the leakage data, that the electrical insulation quality is degraded by Ga out diffusion occurring at the HfO_2/β-Ga_2O_3 interface when it is annealed at 900ºC.

To extract the distribution of interface traps (D_{it}) throughout the bandgap of β-Ga_2O_3 as shown in Figure 5.7 (b), the photo-assisted *C-V* technique was used. This method has been used to characterized various dielectric - β-Ga_2O_3 interfaces [6, 45, 73, 97] and allows for a more thorough extraction of D_{it} due to the use of deep ultra violet (DUV) illumination. The before (solid) and after DUV (dashed) *C-V* sweeps for each case are shown in Figure 5.7 (a). Between the two *C-V* sweeps, the MOSCAPs were held in depletion at -15 V and illuminated with a 256 nm LED for 10 minutes. The D_{it} energy distribution (Figure 5.7 (b)) was then extracted using the following equation:

$$D_{it}(\psi_s) = \frac{C_{ox}}{q}\left(\frac{d\Delta V}{d\psi_s}\right), \tag{5.3}$$

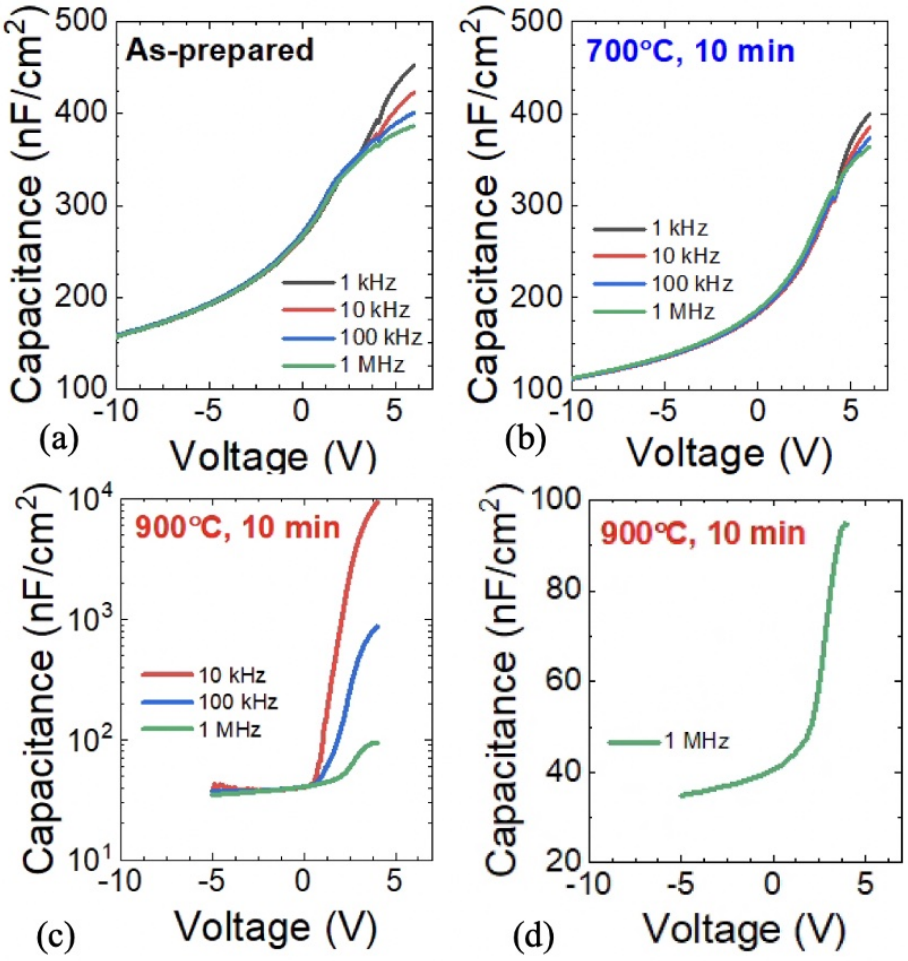


Figure 5.6: *C-V* sweeps at various frequencies for (a) as-prepared and (b) 700ºC, 10-min annealed HfO_2/β-Ga_2O_3 MOSCAPs. (c) Log scale *C-V* data at various frequencies for a 900ºC, 10-min annealed HfO_2/β-Ga_2O_3 MOSCAP, and (d) high frequency (1 MHz) *C-V* sweep plotted on a linear scale to highlight the low capacitance value in accumulation, when compared to Figure 5.6(a) and (b). From [12].

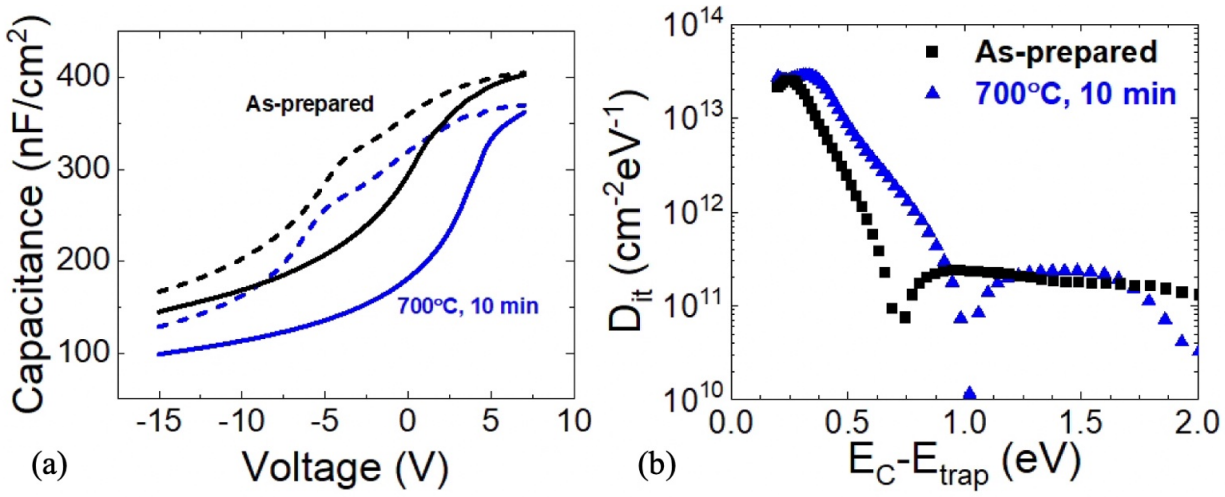


Figure 5.7: Photo-assisted *C-V* method results (a) showing the shift in *C-V* curves due to the filling of traps from the DUV illumination and depletion bias. The MOSCAPs were held in depletion (-15 V) for 10 minutes while the DUV LED was illuminated. Solid curves – before DUV, Dash curves – After DUV & -15V bias. (b) The resulting D_{it} distribution from 0.2 eV to 2 eV below E_C. From [12].

where C_{ox} is the oxide capacitance, q is the electron charge, ΔV is the voltage difference between the before and after DUV *C-V* curves, and ψ_s is the surface potential, which is related to the energy level of the interface trap. C_{ox} was determined by the x-intercept of the $|dC/dV|^{1/3}$ versus *C*, following Islam and Haque's quantum-mechanical model [99]. The relative permittivity (ε_{HfO_2}) of the dielectric ($\sim$10.9) is lower than the value expected for HfO_2 ($>$14), which, along with the frequency dispersion observed in accumulation, indicates the presence of defects inhibiting full accumulation of the MOSCAPs. This may be due to the absence of acid treatments (e.g., piranha clean and buffer oxide etch [100]) before ALD deposition.

The as-prepared and 700ºC-annealed MOSCAPs show a similar D_{it} energy distribution (Figure 5.7(b)) with peak D_{it} values of 2-3 $\times 10^{13}$ $\mathrm{cm^{-2}eV^{-1}}$ near the conduction band (E_C) and a mid-gap D_{it} value of 2 $\times 10^{11}$ $\mathrm{cm^{-2}eV^{-1}}$ at 1-2 eV below E_C. The key difference between these MOSCAPs is that in the 700ºC-annealed MOSCAP the high D_{it} near E_C extends across a wider energy range compared to the as-prepared MOSCAP. For the as-prepared sample, D_{it} drops below 10^{12} $\mathrm{cm^{-2}eV^{-1}}$ around E_C-0.56 eV, whereas for the 700ºC-annealed sample D_{it} reaches this same value at E_C-0.8 eV. These results indicate that the high-temperature anneal creates additional

interface traps in the sub-bandgap energy region (0.3 eV to 0.9 eV below E_C). Integrating D_{it} from 0.2 eV to 2 eV below E_C gives a total D_{it} of 5.4 $\times 10^{12}$ cm^{-2} for the as-prepared sample and 9.9 $\times 10^{12} \mathrm{cm}^{-2}$ for the 700ºC-annealed sample. Thus, the 700ºC-annealed sample has a significantly higher total density of interface states. This trend agrees with the observation of an increased flat band voltage shift, ΔV_{fb}, following DUV illumination. The 700ºC-annealed MOSCAP has a larger ΔV_{fb} compared to the as-prepared sample (Figure 5.7 (a)). Average D_{it} values of $< 10^{12}$ $\mathrm{cm}^{-2}\mathrm{eV}^{-1}$ have been measured on HfO_2/($\bar{2}01$) β-Ga_2O_3 MOSCAPs using traditional D_{it} techniques, including Terman [7] and High-Low Frequency method [80].

The results of these temperature stability investigations on the ALD HfO_2/β-Ga_2O_3 interface are summarized in Figure 5.8. For the minimal thermal treatment used here (i.e., the required 470ºC 1-min ohmic contact anneal), the ALD HfO_2 begins to crystallize, but still forms a robust insulator to the wide bandgap semiconductor. Between 500ºC and 700ºC the HfO_2 film and its interface to β-Ga_2O_3 begins to degrade resulting in an increase in D_{it} and leakage current. However, the film still provides electrical insulation for the wide bandgap semiconductor. Upon annealing at 900ºC the ALD HfO_2/β-Ga_2O_3 interface breaks down due to the diffusion of Ga atoms into the HfO_2 layer, as observed by SIMS depth profile analysis, causing the dielectric properties to fully degrade and leakage current to drastically increase. Such high temperature anneals, between 900 ºC and 1000 ºC, are often used for post-ion implant anneals [92]. While temperatures down to 800 ºC can be used for this purpose, in order to minimize dielectric degradation, this results in lower donor activation efficiency [101].

While the ALD HfO_2/β-Ga_2O_3 interface appears to be more stable under high temperature anneals compared to ALD Al_2O_3/β-Ga_2O_3, which has been demonstrated to out-diffuse Ga into Al_2O_3 at 700ºC [11], nonetheless, these high temperature effects must be considered when designing and fabricating β-Ga_2O_3 MOS structures with thin HfO_2 layers. Further optimization of the ALD dielectric, such as formation of bilayer stacks or ternary alloys with SiO_2 [102, 103], may improve the thermal stability of the HfO_2/β-Ga_2O_3 interface by reducing the out-diffusivity of Ga. Additional material analyses, including high-resolution transmission electron microscopy and atomic probe

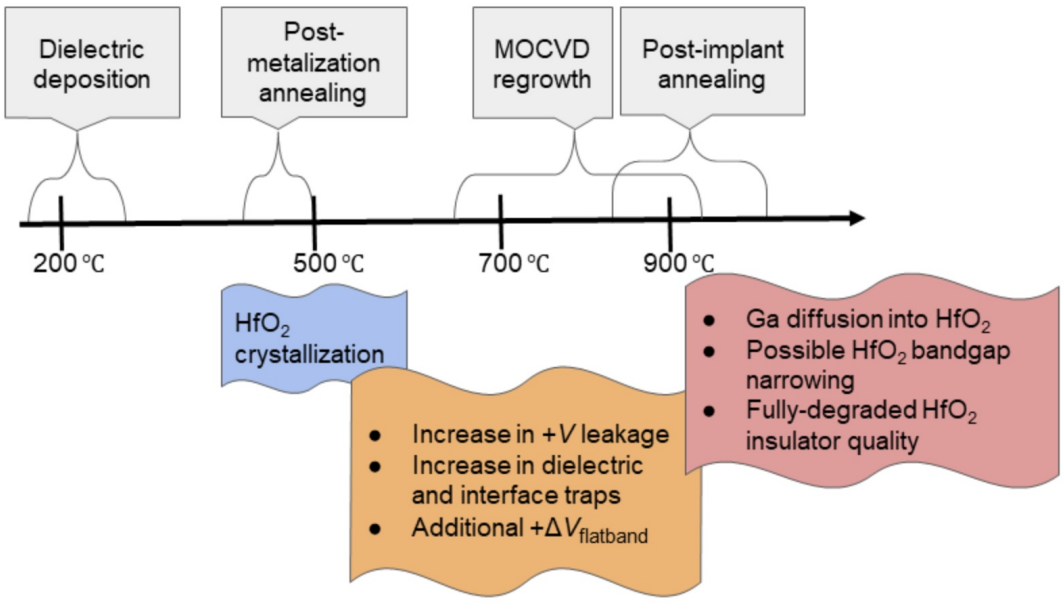


Figure 5.8: Diagram summarizing the impacts of high temperature annealing on the ALD HfO_2 dielectric and its interface to β-Ga_2O_3, using examples of fabrication processes frequently used in this temperature range. From [12].

tomography, would be beneficial for an in-depth understanding of the interactions occurring at these material interfaces. Thermal studies of such dielectrics should be performed to assess their stability in practical gallium oxide device fabrication process flows.

5.4 Conclusion

A thermally stable dielectric-semiconductor interface is necessary for the development of high-performing, reliable power MOSFETs. With many device fabrication processes requiring various high temperatures it is important for device researches to be aware of the impact these thermal stresses can have on the MOS structure. The stability issue of the Al_2O_3/β-Ga_2O_3 interface at elevated temperatures has been well-documented [11, 38, 44, 49] indicating that Al_2O_3 may be an inadequate choice of gate dielectric for future β-Ga_2O_3 MOSFETs. The goal of this chapter was to determine how high temperature annealing processes impacted the HfO_2/β-Ga_2O_3 interface, including both the material and electrical properties.

Ga-atoms have been observed to out-diffuse from the Ga_2O_3 substrate into the Al_2O_3 layer after annealing at 700°C [11]. Once I verified the ability to observe Ga-diffusion in Al_2O_3 due to high temperature annealing with secondary ion mass spectrometry (SIMS) depth profile, I performed a similar experiment on ALD HfO_2/β-Ga_2O_3 samples. These dielectric-semiconductor stacks were annealed in N_2 environment at various temperatures, and the Ga-intensity depth profile from SIMS only showed significant Ga-diffusion into the HfO_2 layer after annealing at 900°C. Electrical analysis of MOS capacitors showed the diffusion of Ga into the HfO_2 layer severally degraded the MOS structure resulting in poor electrical insulation for the wide bandgap semiconductor, possibly due to decreasing of the HfO_2 bandgap from Ga-incorporation.

While below 900°C significant Ga-diffusion in the HfO_2 layer was not observed, other changes occurred in the MOS structure due to these annealing processes. Grazing incidence X-ray diffraction (GIXRD) showed the HfO_2 film changes from amorphous as-deposited to nanocrystalline when annealed at relatively low temperatures of $<$500°C, which would be used for forming ohmic contacts after metal deposition. Even with the nanocrystalline ordering of the HfO_2 film, the dielectric provided good insulation for β-Ga_2O_3 showing low leakage current in both forward and reverse bias. With a higher annealing temperature of 700°C, the MOSCAPs showed increased leakage in forward bias, as well as, an increase in interface traps laying between 0.3 and 0.9 eV below the conduction band of Ga_2O_3. While no changes were observed in GIXRD results of the nanocrystalline films (as-prepared versus 700°C), changes in the crystal grain boundaries could be contributing to the higher leakage observed in forward bias.

For the first time, this study investigates the impact of various high temperature processing (between 500°C to 900°C) on the ALD HfO_2 β-Ga_2O_3 interface and MOS structure. The conclusions from this study will benefit device researchers as they developed the fabrication processes of β-Ga_2O_3 power MOSFETs with ALD HfO_2 gate dielectric. Additional research on developing a more thermally stable dielectric for β-Ga_2O_3 would be very beneficial; these studies could include incorporating SiO_2 to create a ternary dielectric with HfO_2 to increase the crystallization temperature or a bilayer gate stack to reduce leakage current with a larger conduction band offset and possibly

impede the out-diffusion of Ga atoms. Similar thermal stability studies would also need to be conducted on these gate stacks.

CHAPTER 6

Sidewall Traps on Etched β-Ga_2O_3 in ALD HfO_2/β-Ga_2O_3 (010) Fin MOSCAPs

6.1 Introduction

In the previous chapters, I have focused on analyzing dielectric/β-Ga_2O_3 compatibility on planar surfaces, specifically (010) Sn-doped β-Ga_2O_3 substrates. I have used planar metal-oxide-semiconductor capacitors (MOSCAPs) to investigate the reliability of the ALD HfO_2/β-Ga_2O_3 MOS structure under electrical and thermal stress. This information is crucial for the development of stable power MOSFETs as charge trapping and changes at the dielectric-semiconductor interfaces degrade device performance, e.g. cause threshold voltage (V_{th}) instability. While these planar MOSCAP studies are very useful for understanding the ultra-wide bandgap (UWBG) semiconductor and for power MOSFETs with planar channel regions, devices with vertical channel regions pose new questions about interface traps and MOS reliability.

6.1.1 Vertical Fin MOSFET

As previously mentioned, the vertical fin MOSFET has become the most promising device structure for achieving an enhancement-mode, or normally off, vertical power MOSFET with β-Ga_2O_3. The Jena-Xing research group at Cornell University has become the pioneer in the β-Ga_2O_3 fin MOSFET field. In 2018, they reported the first vertical β-Ga_2O_3 fin MOSFET with

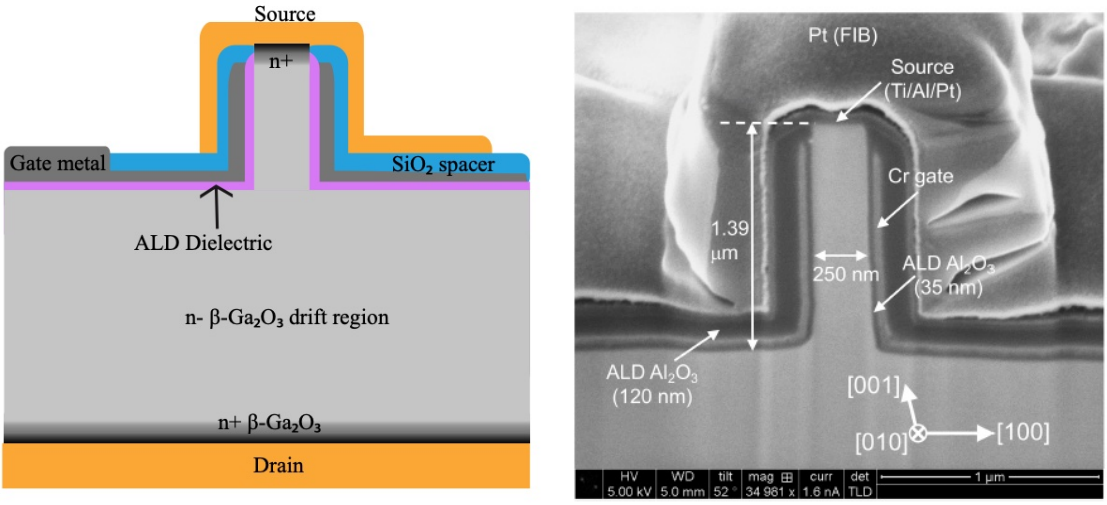


Figure 6.1: Left: Typical β-Ga_2O_3 vertical fin MOSFET cross-section schematic on. **Right:** SEM cross-sectional image of a of a β-Ga_2O_3 vertical fin MOSFET from Li, *et al.*, "Single and multi-fin normally-off Ga_2O_3 vertical transistors with a breakdown voltage over 2.6 kV", IEEE International Electron Device Meeting, © 2019 IEEE [5].

enhancement-mode operation with a breakdown voltage of $>$ 1 kV [37]. More recently, they have implemented field-plating in their devices and achieved a breakdown voltage $>$ 2.6 kV for a multi-fin transistor [5]. A typical vertical fin MOSFET structure is shown on the left in Figure 6.1 adapted from [37]. This structure includes an etched fin, approximately 100 - 400 nm in width, with the source contact connected to the highly doped region at the top of the fin. The gate dielectric, typically deposited by atomic layer deposition (ALD), and the gate contact is formed on both sides of the fin. The voltage applied at this gate controls the width of the conductive channel in the fin and thus, controls the current flowing from the source down to the drift region and then drain contact that is located at the bottom of the device [23]. The right image in Figure 6.1 shows an example SEM of the β-Ga_2O_3 fin MOSFET from the Jena-Xing group [5].

The highlight of the vertical fin MOSFET device structure is the controllable threshold voltage, which is determined by the width of the fin, meaning p-type doping is not necessary to achieve enhancement mode. An ideal fin width can be determined from the doping concentration (ideally low, $< 1 \times 10^{17}$ cm^{-3}) that is required for full depletion of the fin channel at zero bias due to the work function difference between the gate metal and β-Ga_2O_3 [23]. Figure 6.2 shows

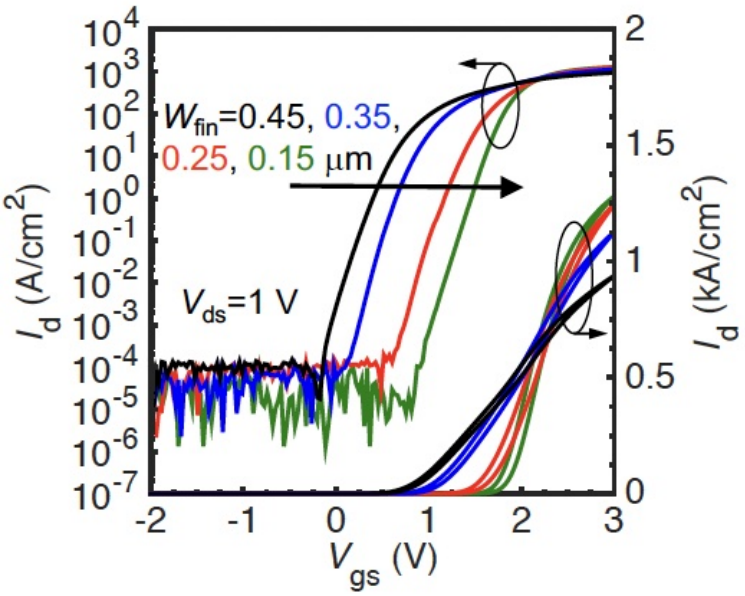


Figure 6.2: Transfer *I-V* characteristics of β-Ga_2O_3 single fin MOSFETs with varying fin widths illustrating how the threshold voltage shifts positively with the narrowing of the fin. From [5] © 2019 IEEE.

the transfer curves of the β-Ga_2O_3 fin MOSFETs shift in the positive direction as the fin width becomes more narrow [5]. The best method to form these fins is by using a plasma dry etching process, typically a BCl_3/Ar etch chemistry. There have been several inductively-coupled-plasma (ICP) reactive ion etching (RIE) studies done on β-Ga_2O_3 and on other phases of Ga_2O_3 in order to achieve optimal etch characteristics [104–106]. One clear disadvantage to these plasma dry etching processes is the inevitable plasma damage to the surrounding Ga_2O_3 [107].

6.1.2 Plasma damage on etched fin sidewall

Degradation of electrical device characteristics have been observed in β-Ga_2O_3 devices on dry-etched surfaces. Yang, *et al.* observed a reduction in the Schottky barrier height and an increase in the ideality factors of $(\bar{2}01)$ β-Ga_2O_3 Schottky diodes due to BCl_3/Ar ICP dry etching [108]. Plasma damage also contributed to a decrease in breakdown voltage of β-Ga_2O_3 Schottky diodes [108, 109]. In β-Ga_2O_3 vertical fin MOSFETs, interface traps along the fin channel, possibly due to the etch damage, contributed to drain-induced barrier lowering and premature

breakdown of the devices [50]. The physical mechanism behind the plasma damage could be a variety or combination of changes occurring at the near-surface β-Ga_2O_3 region, including stoichiometric changes relative to bulk, ion bombardment causing lattice atoms to be displaced, or etch residues remaining on the surface [13]. Lee, *et al.*, used X-ray photoelectron spectroscopy (XPS) to show volatile $BClO_x$ residue left on the dry etched Ga_2O_3 sample [107]. Some studies have started to provide solutions for removing the damage at the surface of the β-Ga_2O_3 using various wet etching chemical treatments, including tetramethyl ammonium hydroxide (TMAH) [107] and hot phosphoric-acid (H_3PO_4) [110], but these studies have focused on planar etched β-Ga_2O_3 surfaces.

Unlike the majority of β-Ga_2O_3 MOSFETs, the MOS gate structure in the fin MOSFET is along the sidewalls of the etched β-Ga_2O_3. As previously mentioned, a reliable MOS structure is crucial for the development of stable power MOSFETs, therefore interface trap and dielectric reliability studies need to be performed on the etched sidewalls of β-Ga_2O_3. In this chapter, I will investigate the sidewall interface of etched β-Ga_2O_3 with ALD HfO_2 using a fin MOSCAP structure and using various capacitance - voltage (*C-V*) techniques, which have been demonstrated in previous chapters on planar MOSCAPs. First, the design and fabrication process for the fin MOSCAP will be discussed, along with discussion about issues that were encountered during fabrication process, how they were resolved, and which further improvements need to be made. The results from the fabrication HfO_2/β-Ga_2O_3 fin MOSCAPs will be discussed and initial conclusions about the sidewall interface quality will be reported. Lastly, I will discuss the remaining scientific questions that have not been answered yet with this study and suggest additional experiments which will bring us closer to a deeper understanding of the sidewall interface traps on etched β-Ga_2O_3.

6.2 Experimental Methods

6.2.1 Fin MOSCAP Designs

MOSCAPs are very useful for investigating the oxide-semiconductor interface without the need of a complicated device structure. In order to investigate the oxide interface to the sidewall

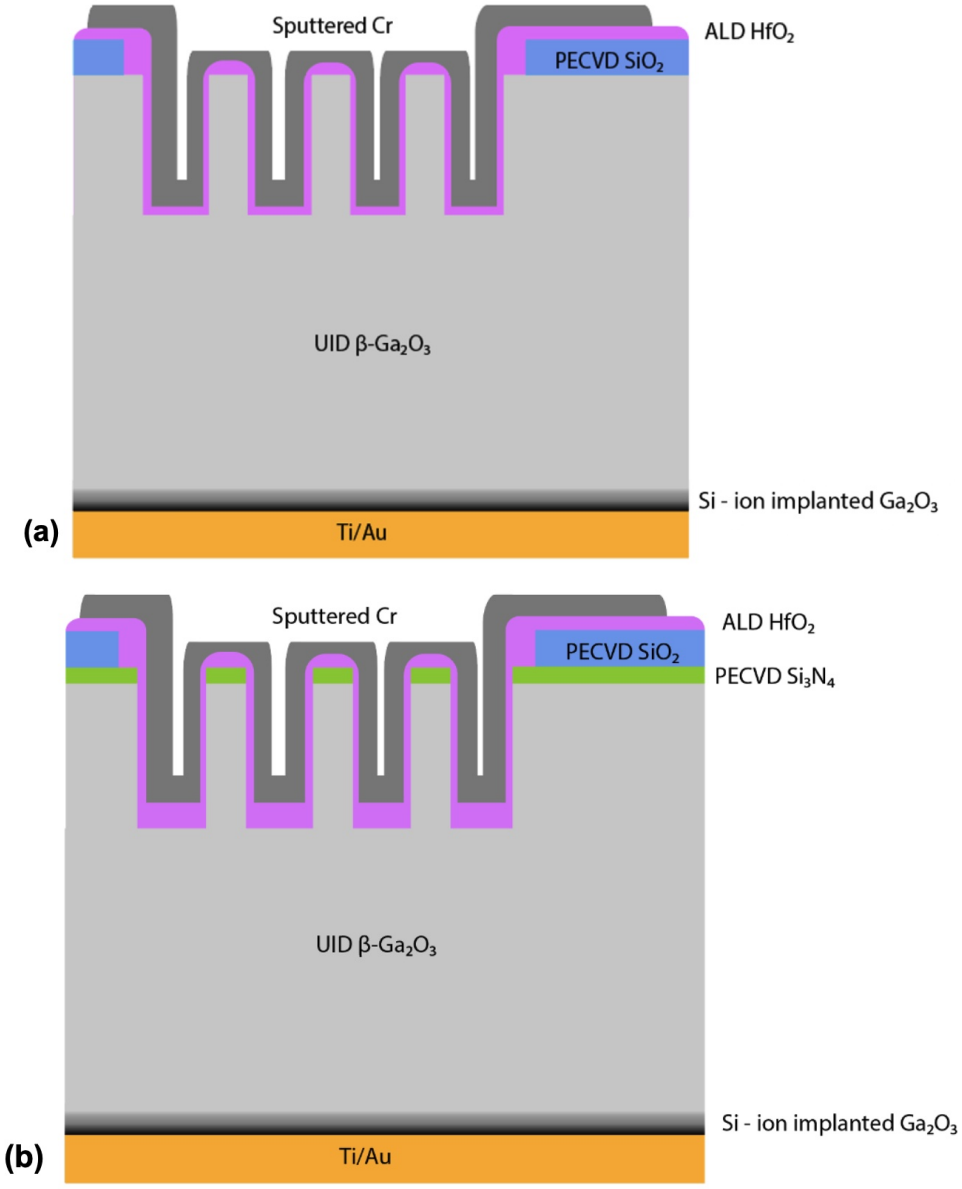


Figure 6.3: Fin MOSCAP cross section (not drawn to scale) showing (a) first design or sample A and (b) second design or sample B. The main improvements made in the second design, compared to the first design, include leaving the remaining Si_3N_4 hard mask at the top of the fins and adding a layer of sputtered Au on top of the Cr top contact to prevent metal oxidation.

of the etched β-Ga_2O_3, a fin MOSCAP structure was designed. Similar structures have been fabricated with β-Ga_2O_3 in order to investigate a new etching technique for this semiconductor, inverse metal-assisted chemical etching [111]. For this study, the focus was placed on the sidewalls of the fins which led to several of the design decisions.

The fin MOSCAP structure is designed to resemble the finFET, but without the source contact. During the fabrication process, I encountered a few issues trying to obtain straight fin sidewalls, which led to some changes to the overall design and fabrication process. Figure 6.3 shows the cross sections of the fin MOSCAP structure (a) first design or Sample A and (b) second design or Sample B. A single fin MOSCAP contains an array of fins with a targeted fin height of 1 μm. The number of fins in each array varies between 100, 150, and 200 fins. The spacing between each individual fin is set to 500 nm, to provide enough space to achieve a straight sidewall during the etch. Approximately 100 by 100 μm area is left unetched next to the fins which is included under the metal top contact as the probing area. In addition to the number of fins in each array, the fin width and fin sidewall direction is varied within the mask design. The fin widths are either 200 nm, 300 nm, or 400 nm. As mentioned earlier, the fin width in FinMOSFETs plays a significant role on the threshold voltage of the device. A smaller fin width would result in better efficiency of depleting the carriers within the fin. Due to the anisotropy of the β-Ga_2O_3 substrate, it is important to take note of the crystal orientation of the sidewall. Crystal orientation has been reported to have an effect on interface trap density and on-current for trench Schottky barrier diodes [112]. β-Ga_2O_3's surface energy can vary significantly depending on the surface plane. First principle study show relaxed surface energies can range from 0.34 J/m^2 for (100) surfaces to 1.95 J/m^2 for (001) surfaces [113]. In our preliminary study, (010) substrates were used and the fins were etched to have sidewalls in the crystal direction of [$\bar{1}$02], [001], [102], [100], and [$\bar{2}$01]. Due to a low yield, the various crystal directions are not discussed at-length. In future iterations, the crystal directions [001] and [100] will be the primary focus.

The last significant design feature in this structure is the additional field oxide layer. Due to the focus on the MOS structure at the sidewalls of the etched Ga_2O_3, a thick SiO_2 layer is included

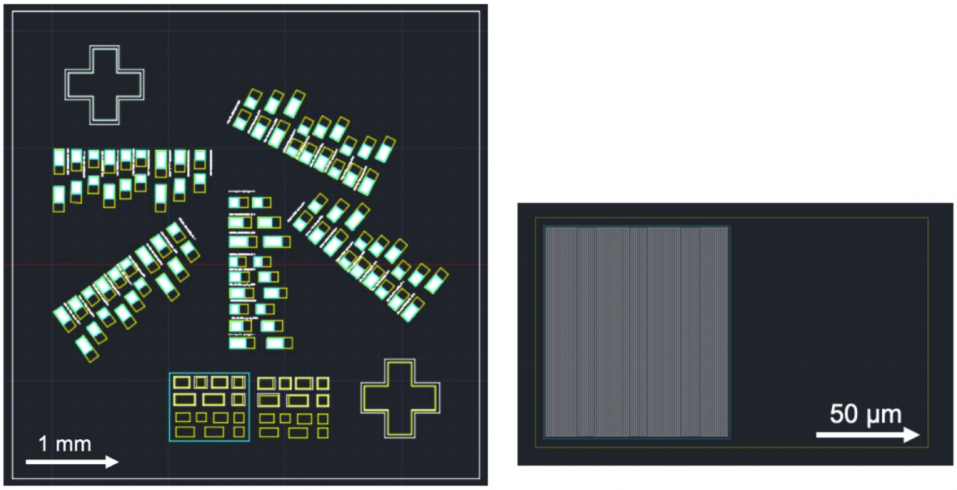


Figure 6.4: (a) Fin MOSCAP sample mask design with (b) an example of a single fin MOSCAP array. The mask layers are as followed: white - e-beam pattern for etching Ga_2O_3, blue - pattern for SiO_2 etch, and yellow - pattern for metal top contact.

on the unetched portions of the sample. This ensures that those areas, including the area under the probing pad, contribute a negligible portion of the total capacitance. With this design, significant changes in *C-V* data are attributed to the etched sidewalls. By taking into consideration the fin MOSCAP parameters, including fin width, length, height, and spacing between fins, a total surface area is calculated for each fin array and the percentage of surface area due to the fin sidewalls is then calculated. An estimated 70% and 75% of the surface area is attributed to the fin sidewalls for the 200 nm and 400 nm fin array, respectively; therefore, the capacitance from the sidewalls contributes to $\sim$ 70 - 75% of the total measured capacitance. The mask design for the fin MOSCAPs is shown in Figure 6.4 (a). Along with the fin MOSCAPs, planar MOSCAPs, on etched and unetched Ga_2O_3, are included at the bottom of the mask design as control MOSCAPs. Figure 6.4 (b) shows an example of the fin MOSCAP array; the white outline indicates the e-beam pattern for the individual fins, the blue rectangles show where the SiO_2 layer will be removed, and the yellow rectangles indicate the top metal contacts.

6.2.2 Fin MOSCAP Fabrication Process

Fin MOSCAPs are formed on UID (010) β-Ga_2O_3 substrates from Tamura Corporation. The fabrication process starts with performing a Si-ion implant on the backside of the wafer in order to achieve a backside ohmic contact following the implant process from Lee and Peterson [85]. The Si-ions are activated at 950°C in N_2 for 30 minutes. The wafer is then etched on the backside $\sim$ 80 nm using ICP-RIE; this ensures the highly doped portion of the substrate is in contact to the back metal contact.

A Si_3N_4 hard mask is used in this process due to its higher selectivity to the BCl_3/Cl_2 RIE which is needed to etch the $\sim$1 μm β-Ga_2O_3 fins. The selectivity of Ga_2O_3 to Si_3N_4 is $\sim$ 1.5, while to SiO_2 and SPR the selectivity is below one [106]. Others have used a Cr mask for etching β-Ga_2O_3 fins [37], but the use of metal masks for plasma etching was not allowed in the shared cleanroom facility. A Si_3N_4 layer ($\sim$300 nm) is deposited on the top side of the sample using plasma enhanced chemical vapor deposition (PECVD) at 350°C. The hard mask is then patterned by electron beam (e-beam) lithography in order to achieve fin widths between 200 - 400 nm. After etching the hard mask, the fins are etched using another RIE step. Both Ga_2O_3 etches (backside and fins), use a BCl_3/Cl_2/Ar chemistry of 30/10/10 sccm, a plasma power of 500 W, and a pressure of 5 mTorr, following the process described in [106]. The resulting fin height was approximately 1.2 μm. The backside etch uses a bias power of 100 W, while the fin etch uses a bias power of 25 W, in order to achieve a straight, sharp sidewall and a higher selectivity to the Si_3N_4 hard mask. The approximate etch rates for the backside and fin etch are $\sim$ 65 nm/min [106] and $\sim$ 43 - 60 nm/min, respectively. During the lower bias fin etch, longer etch times resulted in higher etch rates possibly due to changes in the chamber's environment. Additional testing on the fin etch process will be needed in future iterations to optimize the etch recipe and to understand the impact of chamber conditions on the etch rate.

After the Ga_2O_3 fin etch step, the fabrication process slightly deviates between Sample A and Sample B as displayed in Figure 6.3 (a) and (b). For Sample A, the remaining Si_3N_4 hard mask is then removed using a buffered hydrofluoric acid (BHF) etch. During processing, it was difficult

to verify the thorough removal of the Si_3N_4 layer with an optical microscope as both Si_3N_4 and Ga_2O_3 are transparent. This difficulty led to the decision for during Sample B's processing to leave the remaining Si_3N_4 on top of the fins. This additional layer will not greatly affect the results of the electrical measurements as the focus of the experiment is on the sidewalls of the fins. The Si_3N_4 layer adds an extra dielectric layer to the top of the fins resulting in a decrease in capacitance for this portion of the fin array. A decrease in the capacitance from the top of the fins means a more significant portion of the total capacitance is due to the sidewalls.

The fabrication process continues for both designs with the deposition of the field oxide layer, which is a layer of SiO_2 deposited by PECVD at 350°C. Initially the thickness of the layer was 200 nm; this layer thickness was increased to 500 nm for Sample B. The SiO_2 on and around the fins is etched with BHF and the sample is then annealed in O_2 at 520°C for 3 minutes. The next main step in the fin MOSCAP process is the dielectric deposition. It has been well observed that RIE can damage the Ga_2O_3 surface, especially the sidewalls [50]. Several wet etching treatments have been suggested for improving the damage caused by the dry etch including hydrochloric acid (HCl) and hydrofluoric acid HF, TMAH, and hot H_3PO_4 [37, 107, 110]. For this study, a hot H_3PO_4 etch at 80°C for 10 minutes was performed before the dielectric deposition. A 26 nm layer of HfO_2 is deposited by atomic layer deposition (ALD) at 200°C using tetrakis(dimethylamido)hafnium (TDMAH) precursor and H_2O oxygen source. The top and backside metal contacts are then formed. 100 nm of Cr is sputtered; Sample B included an additional Au layer on top of the chrome to prevent oxidation. The gate metal is then patterned and etched to form the top contact. The backside contact is formed by a brief ion mill etch of 5 min, followed with a deposition of Ti/Au (20/230 nm) by electron beam evaporation, and lastly, annealing the sample at 470°C in N_2 for one minute.

6.2.3 Measurement details

Capacitance - voltage (*C-V*) and current - voltage (*J-V*) measurements were performed with an HP4284A LCR meter and an HP4156A semiconductor parameter analyzer, respectively. All measurements were performed in the dark at room temperature. A frequency of 1MHz was used

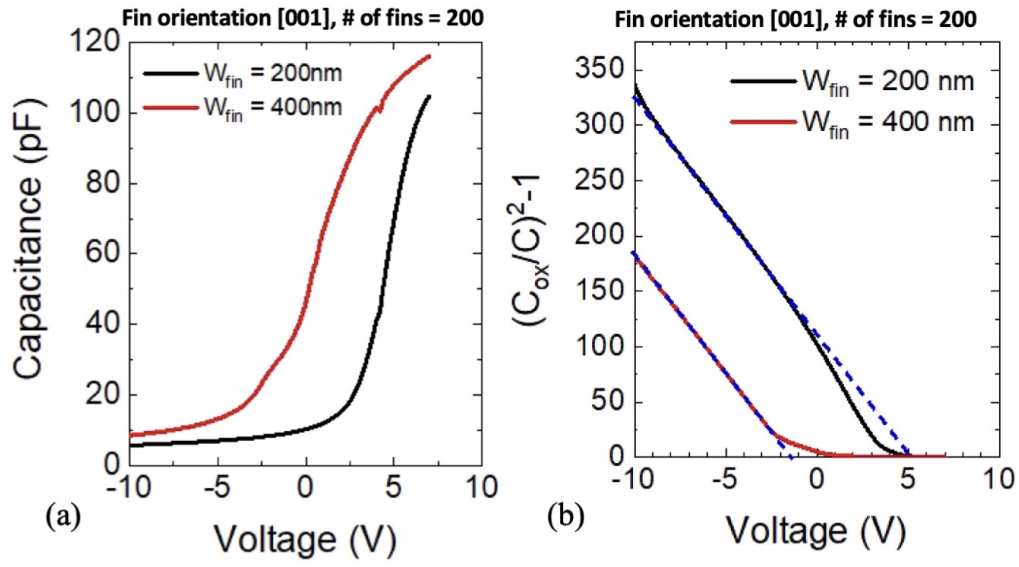


Figure 6.5: (a) *C*-*V* results from fresh fin MOSCAPs in the crystal orientation of [001] with 200 fins within the array and (b) $(C_{ox}/C)^2$-1 - *V* plot, where the x-intercept indicates the V_{fb}. The doping level (N_d), extracted from the $1/C^2$ slope, is $\sim 2 \times 10^{17}$ cm^{-3}, which matches the expected N_d from Tamura Corporation. Fin height is estimated to be approximately 1.2 μm.

for the *C*-*V* measurements, unless otherwise specified. *C*-*V* sweeps were taken in the direction from depletion (-*V*) to accumulation (+*V*) and with a sweep rate of 1 V/s. Due to the nonplanar structure of the fin MOSCAP, capacitance data is given in units of Farads (F) and not F/cm^2. *J*-*V* measurements were taken with slow integration starting at 0 V and increasing to 5 - 7 V. SEM images were taken with a Hitachi SU8000 cold field emission SEM.

6.3 Results and discussion

Results will be discussed from completed fabrication runs of both fin MOSCAP designs. A few fabrication issues came to light, which resulted in a low yield of the fin MOSCAPs. While these results presented some interesting observations, additional fin MOSCAP studies will be needed to optimize this vertical gate structure.

6.3.1 Fin MOSCAP electrical results: Sample A

Here I examine the *C-V* results from Sample A. First, differences in the *C-V* curve shape between fin widths (W_{fin}) of 200 nm and 400 nm are observed. Figure 6.5 (a) shows examples of the *C-V* results from the fresh fin MOSCAPs in the fin orientation of [001] for both W_{fin} of 200 nm and 400 nm. The flatband voltage (V_{fb}), which is determined by the x-intercept in the $(C_{ox}/C)^2$-1 data (Figure 6.5 (b)), is significantly higher for the 200 nm case. V_{fb} is +6 V and -1.5 V for the 200 nm and 400 nm fins, respectively. Based on the correlation between V_{fb} and V_{th}, a more positive V_{fb} for smaller fins is expected. The 200 nm fin is fully depleted at 0 V, while the 400 nm fin is only partially depleted at 0 V.

Another significant difference is the shape of the *C-V* curves: a hump appears in the 400 nm fin case between -3 and 0 V, while the 200 nm fin case shows a smoother curve. In this region of the *C-V* curve, the middle of the 400 nm fins is no longer depleted and starts to accumulate electrons. Beyond 0 V, the fin MOSCAP can accumulate electrons along the sidewalls, which leads to a rise in the capacitance value. Due to the thinner structure of the 200 nm fins, the hump in the *C-V* curve is much less apparent. In Figure 6.5 (b), the $(C_{ox}/C)^2$-1 slope change observed between 1 V and 5 V in the 200 nm fin array shows the transition of the middle of the fins beginning to accumulate electrons.

Silvaco Atlas simulations are used to further illustrate how the electron accumulation in the fins correlates to the *C-V* curves. Figure 6.6 (a) and (b) show the fin MOSCAP structures created in Silvaco using similar parameters as the experimental fin MOSCAPs with a W_{fin} of (a) 400 nm and (b) 200 nm. Figure 6.6 (c) shows the high frequency *C-V* curves of both simulated structures. Interface traps were not included in the simulated Fin MOSCAP structures, which leads to the V_{fb} differences in the simulated versus the experimental data. Both structures show similar behavior beyond 0V, where the accumulation of electron occurs at the sidewalls. In the depletion region (<0 V), both curves show a similar hump as the 400 nm fin MOSCAP in Figure 6.7 (a). Those initial increases in capacitance as the MOSCAP is moving from depletion (-*V*) to 0V indicate the middle of the fins beginning to accumulate with charge as shown by Figure 6.8 (a)-(d). Both the *C-V*

curves in Figure 6.6 (c) and Figure 6.7 (a)-(d), which are simulated fin cross-sections displaying the electron concentration at various depletion biases, show that a larger fin width will require a stronger depletion bias to fully deplete the center of the fins. At a V_{gate} (bias applied to the top contact surrounding the fins) of -2 V (Figure 6.7 (c)), the 200 nm fins are mostly depleted which correlates to the drop in capacitance from -1.6V to -2V in the *C-V* curve in Figure 6.6 (c). In contrast, the 400 nm fins still have a high electron concentration in the center of the fins at -6 V (Figure 6.9 (b)) and requires a bias of -8 V to mostly deplete the fins (Figure 6.7 (a)). This correlation between W_{fin} and charge accumulation is also shown in Figure 6.7 (d), where the $(C_{ox}/C)^2$-1 versus V plot indicates a $\sim$ 6 V difference in the V_{fb} for the two simulation fin MOSCAPs. The simulated results and the experimental data illustrates the impact of W_{fin} on electron depletion and accumulation within the fin structure, which correlates directly to achieving an enhancement-mode fin-MOSFET.

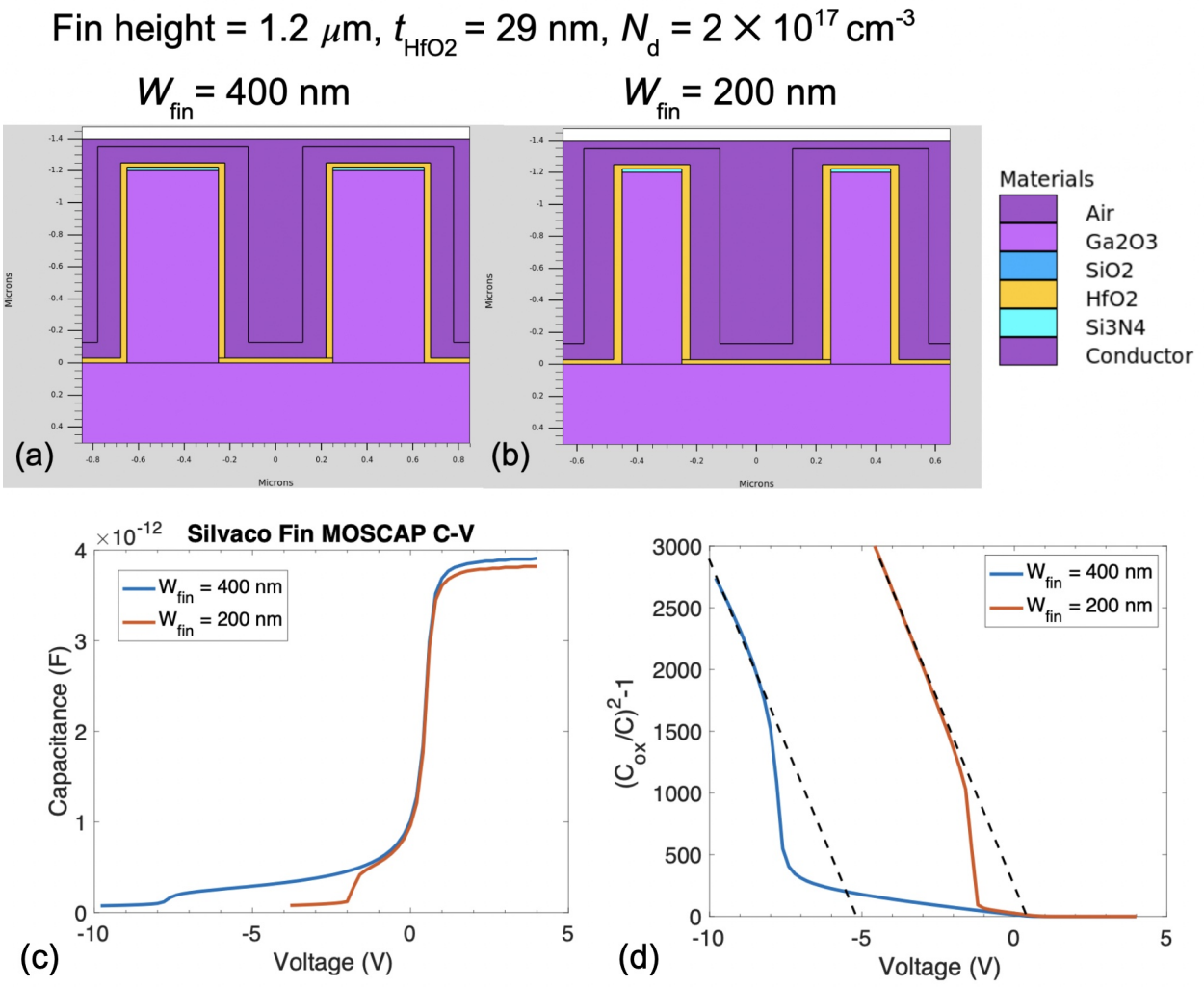


Figure 6.6: Fin MOSCAP structure used in Silvaco Atlas simulation with (a) W_{fin} of 400 nm and (b) W_{fin} of 200 nm, and (c) the resulting high frequency (1 MHz) *C-V* sweep of both structures. (d) $(C_{ox}/C)^2$-1 versus voltage showing how the flatband voltage varies based on W_{fin}. The width (into the page) of the Silvaco structure is set to 100 μm.

In Sample A, fin MOSCAP arrays are included with 5 different fin orientations to observe differences in interface traps along various crystal planes. Due to a low yield only three of the five directions are discussed here: [001], [102], [100]. Based on the collected data, no significant differences in *C-V* curves are observed. Examples of the *C-V* results for 400 nm fin MOSCAPs arrays in the directions of [001] and [102] are shown in Figure 6.8 (a), and Figure 6.8 (b) shows the results for the 200 nm case in the directions of [001], [102], and [100]. The accumulation region in Figure 6.8 (b) shows one of the main reasons no strong conclusions can be made at this time; past

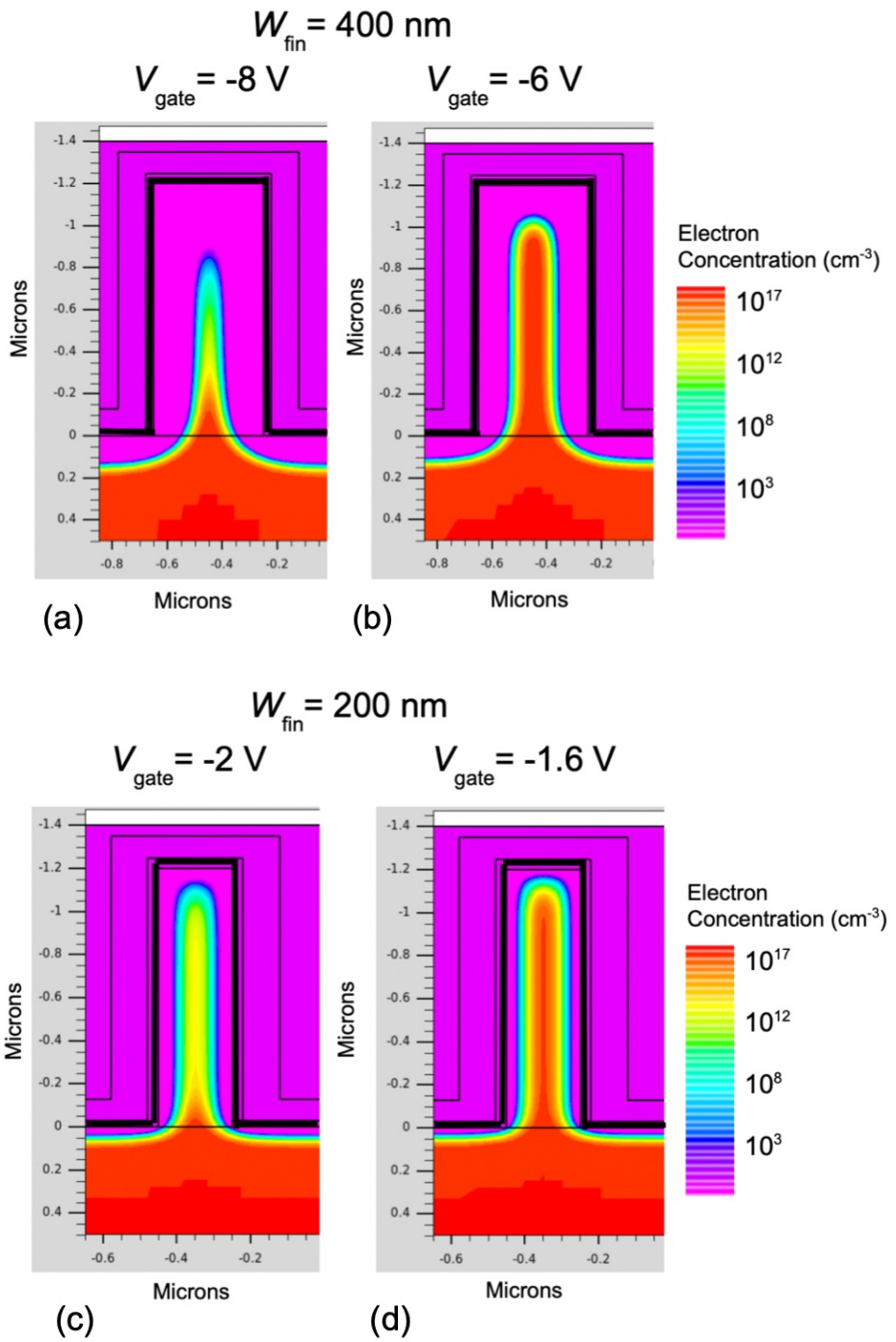


Figure 6.7: Silvaco Atlas simulations of the electron concentration within the fin MOSCAP structure with a W_{fin} of 400 nm at a voltage bias of (a) -8 V and (b) -6V, and a W_{fin} of 200 nm at a voltage bias of (c) -2 V and (d) -1.6V. The color indicates the electron concentration with red being 10^{17} cm^{-3} and green/yellow being $\sim 10^{11}$ - 10^{12} cm^{-3}. V_{gate} refers to the voltage bias applied to the top contact that surrounds the fins. Figures show half of the whole simulated structure (shown in Figure 6.6); the second fin in each case displays the same electron concentration profile as shown here.

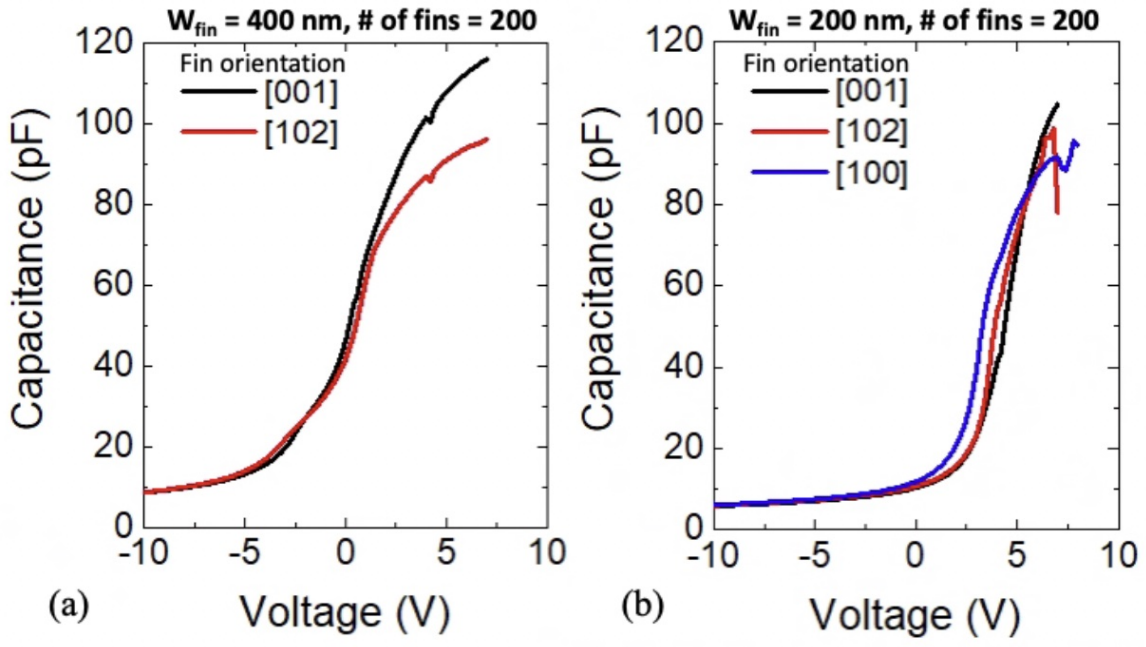


Figure 6.8: (a) *C-V* results for fresh fin MOSCAPs in various crystal orientations for W_{fin} of 400 nm and (b) 200 nm.

+5 V the fin MOSCAPs show unreliable behavior and frequently break down without any intentional stress, as shown by the drop in capacitance for the 200 nm, [102] case (red curve).

Along with the breakdown of the fin MOSCAPs, significant V_{fb} shifting is observed with repeated *C-V* sweeps as shown in Figure 6.9 (a). In Chapter 3, I analyzed the shifting *C-V* curves from "fresh" to "stable" in planar HfO_2/β-Ga_2O_3 MOSCAPs and contributed it to filling of border traps in the dielectric. While the *C-V* curves appear to become stable, partial breakdown occurs, which results in the C_{ox} being reduced significantly. We also see similar behavior for the *J-V* sweeps as shown in Figure 6.9 (b). Another fresh 400 nm fin MOSCAP array with the fin orientation of [102] is measured for leakage current, and a repeated *J-V* sweep showed a +2.5 V shift and breakdown of the MOSCAP at 6 V. Due to the premature breakdown, D_{it} was not extracted from this sample.

To assess the quality of the dielectric layer, I characterized planar MOSCAP test structures included in the piece. Figure 6.10 (a) and (b) show repeated *C-V* sweeps of the planar HfO_2/β-Ga_2O_3 MOSCAPs on an unetched surface and etched surface, respectively. The shifting *C-V*

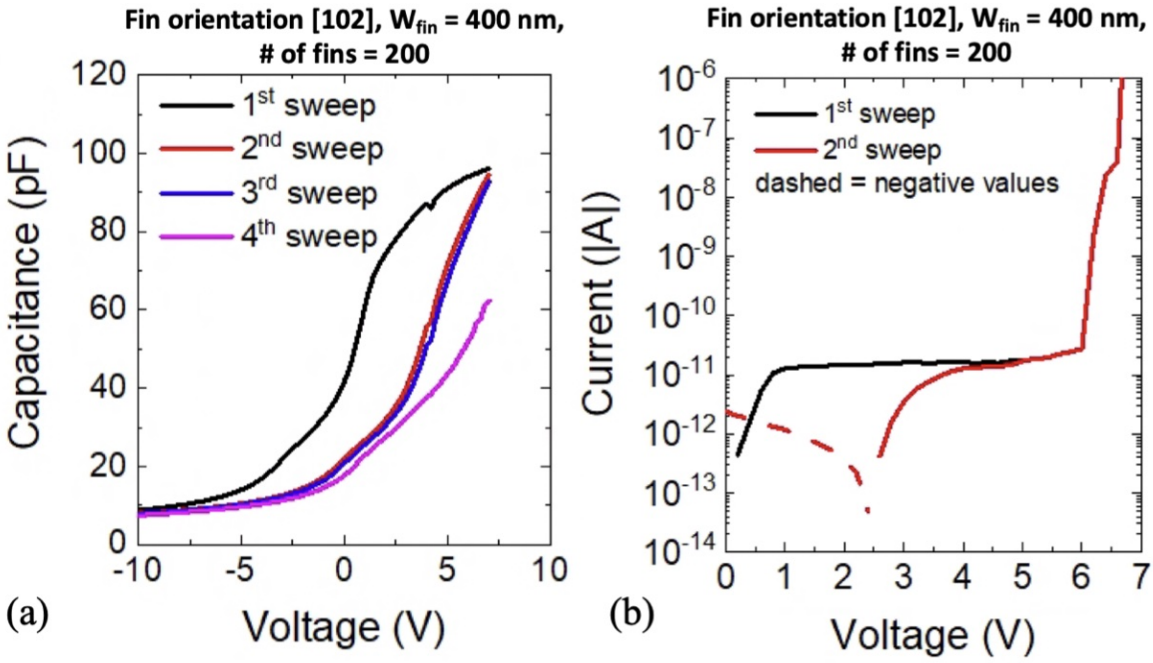


Figure 6.9: (a) Repeated *C*-*V* sweeps starting from "fresh", or 1st sweep, for W_{fin} of 400 nm with fin orientation [102] showing significant shifting in V_{fb}. (b) Consecutive *J*-*V* sweeps on "fresh" fin MOSCAP with the same W_{fin} and orientation. 2nd sweep shows +2.5 V shift in *J*-*V* and breakdown at 6 V. Similar shifts in *C*-*V* and *J*-*V* are observed with repeated sweeps. Sweep direction is from depletion (left) to accumulation (right).

curves were expected based on the fin MOSCAP results, but the C_{ox} value was significantly lower than expected. C_{ox} is defined by the following equation,

$$C_{ox} = \frac{\varepsilon_{ox} \times \varepsilon_o}{t_{ox}} \tag{6.1}$$

where ε_{ox}, ε_o, t_{ox} are the dielectric permittivity, vacuum permittivity, and the dielectric thickness. Based on an expected ε_{ox} of 12-13 and a t_{ox} of 26 nm, the C_{ox} should be over 400 nF/cm^2. C_{ox} for both the unetched and etched planar surface MOSCAPs are $<$50% of the expected value indicating that the dielectric appears to be of low quality. While the ALD HfO_2 quality may be degraded resulting in a lower ε_{ox} similar to the HfO_2 results presented in Chapter 5, that and small variations in oxide thickness would not account for this significant decrease in oxide capacitance. Similar to the fin MOSCAPs, the planar MOSCAPs are degrading after a few repeated sweeps and at low

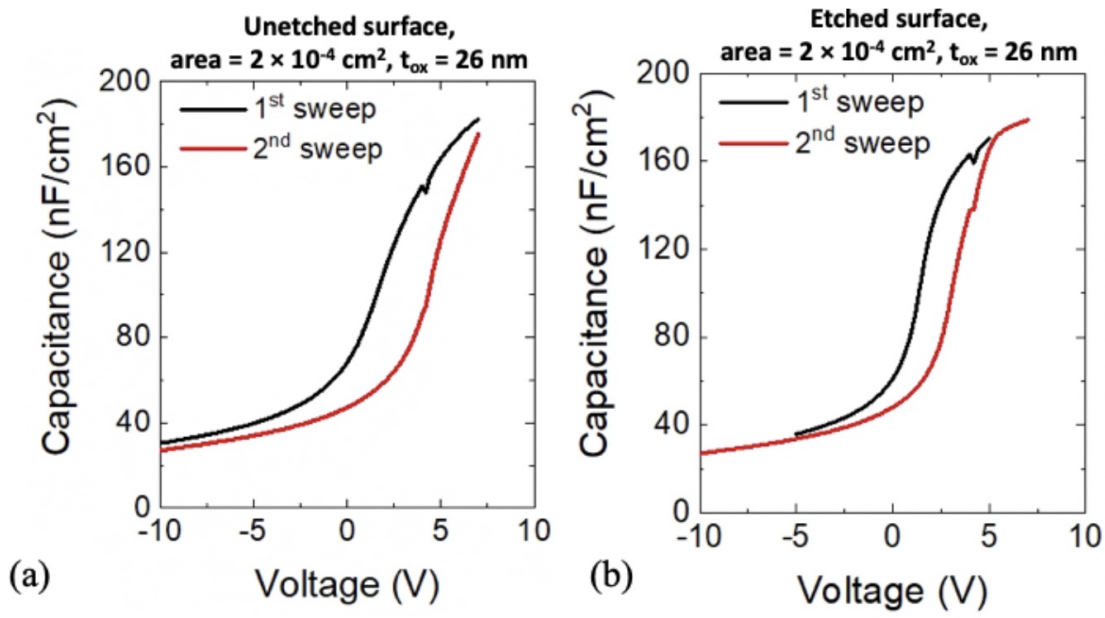


Figure 6.10: (a) Repeated *C-V* sweeps of unetched planar MOSCAPs, and (b) etched planar MOSCAPs. Expected C_{ox} is determined to be ∼400 nF/cm^2, more than 2x the current C_{ox} indicating an issue with the fabricated Fin MOSCAPs.

voltages.

6.3.2 Fin MOSCAP electrical results: Sample B

As described in Section 6.2.2, for Sample B I did not remove the Si_3N_4 layer and added a thicker SiO_2 field oxide. Figure 6.11 shows an example of repeated *C-V* sweeps at a frequency of 1 MHz for a [100]-oriented 400 nm fin array. There are two important observations to note. First, the C_{ox} is less than 100 pF, which is even lower than the previous sample. The cause of this decrease could be partially the smaller total surface area due to the remaining Si_3N_4 hard mask that is left on the sample. The lower C_{ox} value could also be attributed to a higher interface traps density (D_{it}) on the sidewalls of the fins. Since in the previous sample the remaining Si_3N_4 hard mask was removed with BHF; that additional BHF treatment may have removed some of the etch damage from the sidewalls of fins resulting in a lower D_{it}. Because of the premature breakdown of the Sample A, I was not able to extract D_{it} to make a comparison.

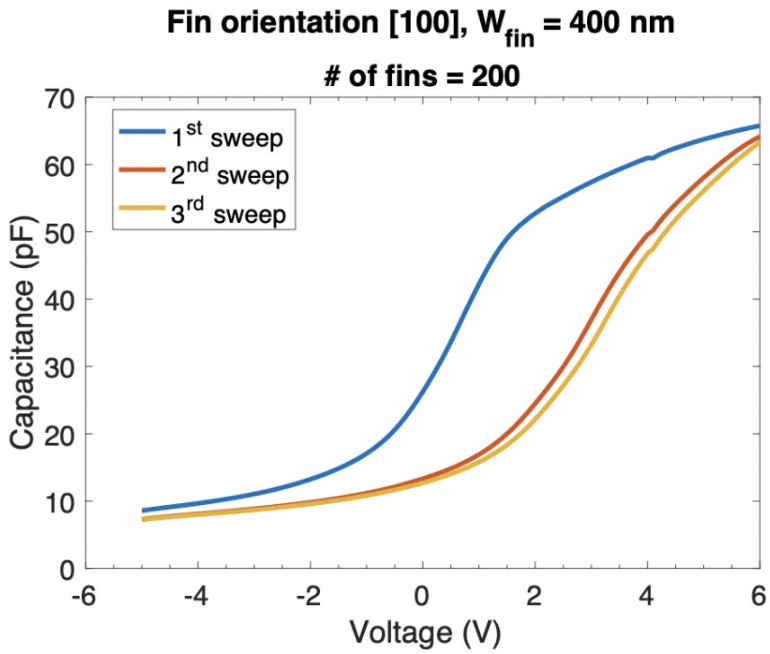


Figure 6.11: Repeated *C-V* sweeps starting from "fresh", or 1st sweep, of a fin MOSCAP from Sample B (W_{fin} = 400 nm and fin orientation [100]) showing a +2.5 V shift in V_{fb}. Fin height is estimated to be approximately 1.2 μm.

Second, although Sample B is still showing a lower C_{ox} than expected, the fin MOSCAP arrays appear to be more stable in this sample compared to previously. Figure 6.11 shows that there is a +2.5 V flatband voltage shift (ΔV_{fb}) between the first and second sweep but appears to stabilize and the C_{ox} does not decrease significantly as in Figure 6.9 (a). A ΔV_{fb} of +2.5 V equates to an oxide trap density (D_{ox}) of approximately 1.7 $\times 10^{12}$ cm^{-2} [41]. As previously explained, an initial shift in the *C-V* curves is expected with the filling of border traps in the dielectric and the absence of mobile holes from the β-Ga_2O_3 substrate that would normally recombined with the trapped electrons [10].

The stable *C-V* behavior allowed me to perform additional electrical testing to analyze the sidewall interface quality. Figure 6.12 shows *C-V* curves at various frequencies for a [100]-oriented fin MOSCAP array. There is significant frequency dispersion near accumulation with a frequency of 1 kHz showing maximum *C* values double of what is observed for 1 MHz. This frequency dispersion can possibly be attributed to a high density of interface traps and border traps [98].

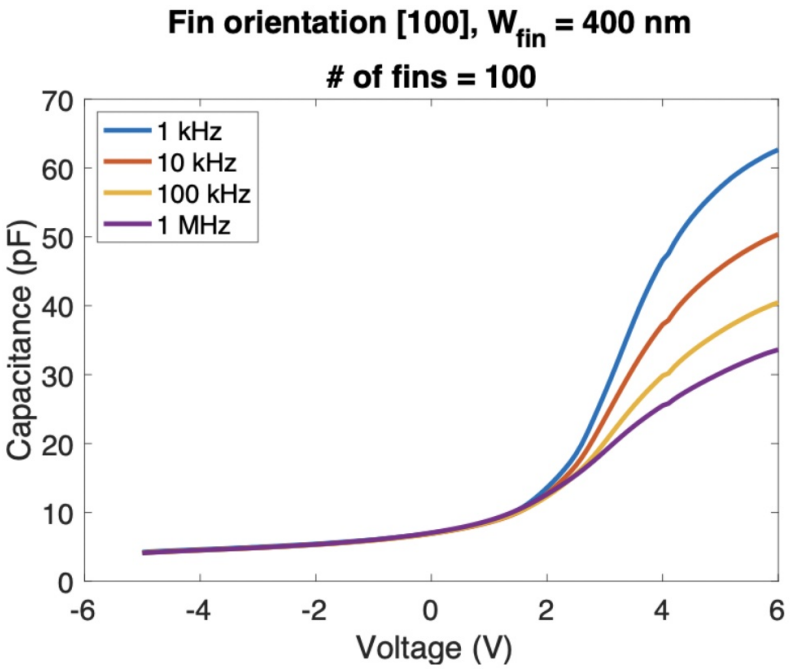


Figure 6.12: *C-V* sweeps at various frequencies for a fin MOSCAP array with W_{fin} = 400 nm and fin orientation [100].

The photo-assisted *C-V* and AC conductance method are used further investigate the interface quality of the etched fins to the dielectric. These methods have been demonstrated previously on planar β-Ga_2O_3 MOSCAPs in this thesis as well as in other β-Ga_2O_3 planar MOSCAPs [39, 45, 73, 97]. The photo-assisted *C-V* has also been demonstrated to extract an average D_{it} on β-Ga_2O_3 fin arrays formed by inverse metal-assisted chemical etching [111]. Here, I use the same method as described in chapter 3 to extract a distribution of D_{it} across a significant portion of the β-Ga_2O_3 bandgap. Figure 6.13 (a) shows the *C-V* curves before (solid curve) and after (dashed curve) the deep ultraviolet (DUV) illumination (265 nm) and depletion bias (-5 V). The distribution of D_{it} is shown in Figure 6.13 (c) which was calculated following the same method as described in Chapter 3 using equation 3.3. The table in Figure 6.13 (d) includes several parameters for the fin MOSCAP measured here. In previous planar MOSCAP studies, high D_{it} values $>10^{12}\,\text{cm}^{-2}\text{eV}^{-1}$ are observed near the conduction band (E_{C}) as also displayed in Figure 6.13 (c), but D_{it} tends to decrease to around $10^{11}\,\text{cm}^{-2}\text{eV}^{-1}$ near the mid-bandgap. In Figure 6.13 (c) the D_{it} stays consistently around $10^{12}\,\text{cm}^{-2}\text{eV}^{-1}$ from 0.5 eV to 1.8 eV below E_{C}. This may indicate an increase in D_{it} compared to

planar HfO_2 MOSCAPs discussed in Chapter 5, due to the plasma damage during the β-Ga_2O_3 etch. Though it is also important to note that previous D_{it} results were measured on Sn-doped β-Ga_2O_3 substrates and in this study UID substrates are used. Integrating D_{it} from 0.2 eV to 1.8 eV below E_C gives a total D_{it} of 2.8 $\times 10^{12}\ \mathrm{cm}^{-2}$ for the fin MOSCAP array. For a comparison to literature, a low average D_{it} of 2.7 - 3.7 $\times 10^{11}\ \mathrm{cm}^{-2}\mathrm{eV}^{-1}$ has been extracted from the ΔV_{fb} due to UV illumination on β-Ga_2O_3 fin arrays that were formed by inverse metal-assisted chemical etching; the low D_{it} was achieved by using a fin-formation process that does not require plasma dry etching [111]. An estimated D_{it} of $< 10^{12}\ \mathrm{cm}^{-2}\mathrm{eV}^{-1}$ was calculated based on the subthreshold slope of a β-Ga_2O_3 fin MOSFET, where the fins were formed by ICP-RIE [5]. A comparison between etched and unetched planar MOSCAPs on the same sample would be very beneficial to determine the cause of the higher D_{it}, but because the Si_3N_4 layer was not fully removed from the sample I was not able to measure the unetched planar MOSCAPs.

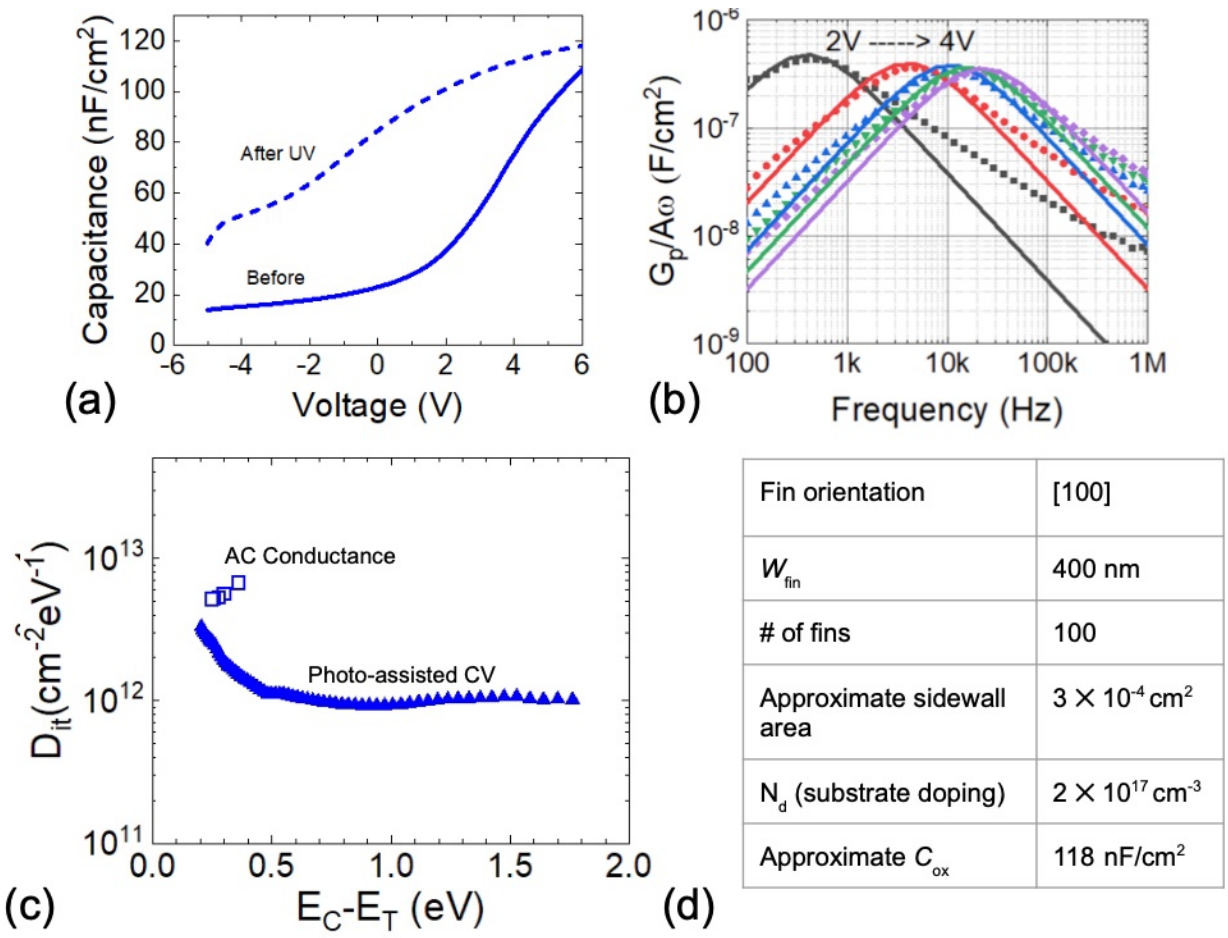
The AC conductance method is also utilized to extract D_{it} near the conduction band. This method is described in more detail in Chapter 2. Figure 6.13 (b) shows the $G_p/A\omega$ versus frequency data from the same fin MOSCAP as in Figure 6.13 (a). This data is calculated from the parallel capacitance (C_m) - parallel conductance (G_m) circuit model using equation 2.8. D_{it} is calculated from the maximum $G_p/A\omega$ value for each voltage bias using equation 2.9 [41]. The energy level of the measured interface trap is determined by the corresponding frequency of the maximum $G_p/A\omega$ value. This conversion uses the following equation,

$$E_C - E_t = ln[\tau_{it}\sigma_N v_T N_C] \times kT, \tag{6.2}$$

where τ_{it} is time constant of the trapped electron emission ($1/\omega$), σ_N is the capture cross-section of electrons, v_T is the electron thermal velocity, N_C is the conduction band density of states, k is the Boltzmann's constant, and T is the temperature [56]. Figure 6.13 (b) also includes fittings to the following theoretical equation discussed in Chapter 2 (equation 2.7) [41].

The resulting D_{it} versus E_C-E_T is displayed with the photo-assisted D_{it} results in Figure 6.13 (c). From the AC conductance method, D_{it} ranges from 4 to 6 $\times 10^{12}\ \mathrm{cm}^{-2}\mathrm{eV}^{-1}$ in the energy range

from 0.2 eV to 0.3 eV below E_C. Both D_{it} methods indicate a high quantity of interface traps near the conduction band. Figure 6.14 shows a band diagram illustration of the approximate interface trap distribute that is observed in these fin MOSCAPs. More analysis is needed to verify that the cause of the high D_{it}, especially near the mid-bandgap, which previously was an order of magnitude lower in planar MOSCAPs, is caused by plasma damage to the sidewalls of the fins. Deep level transient spectroscopy (DLTS) showed that halide vapor phase epitaxy (HVPE) β-Ga_2O_3 (001) films had a significant increase in near-surface defects at energy levels of 0.8, 1.05, and 2.3 eV below E_C after being exposed to Ar plasma [114]. While an improved fin MOSCAP fabrication process will be needed to fully investigate the differences in fin sidewall interface traps, this work demonstrates the ability to utilize a fin MOSCAP structure for this type of analysis. Due to the significant undercutting observed during the β-Ga_2O_3 etch of Sample B, only fin MOSCAP arrays of 400 nm W_{fin} with the fin orientation of [100] are discussed in this section.



Fin orientation	[100]
W_{fin}	400 nm
# of fins	100
Approximate sidewall area	3×10^{-4} cm^2
N_d (substrate doping)	2×10^{17} cm^{-3}
Approximate C_{ox}	118 nF/cm^2

Figure 6.13: (a) Photo-assisted *C-V* method results showing the shift in *C-V* curves due to the filling of traps from the DUV illumination and depletion bias. The MOSCAPs were held in depletion (-5 V) for 10 minutes while the DUV LED was illuminated. Solid curves – before DUV, Dash curves – After DUV & -5V bias. (b) AC conductance method data showing $G_p/A\omega$ versus frequency data. Experimental data are the symbols and lines show the fitting to equation 6.6. (c) The resulting D_{it} distribution from 0.2 eV to 1.8 eV below E_C from (a) photo-assisted *C-V* and from (b) the AC conductance method. (d) Table here contains various information about the measured fin MOSCAP for (a)-(c).

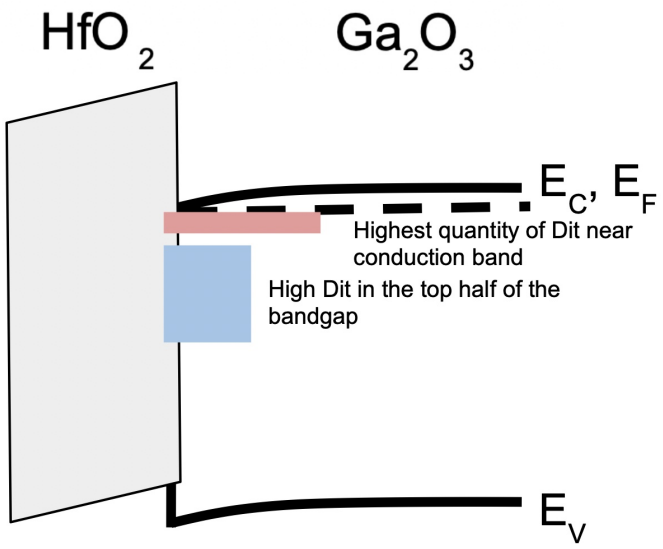


Figure 6.14: HfO_2/β-Ga_2O_3 band diagram illustrating the approximate interface trap distribution of the etched fin sidewall. I was only able to measure D_{it} in the top half of the bandgap, due to energetic and time-scale limits.

6.3.3 Fin MOSCAP fabrication challenges

During the fabrication process of both fin MOSCAP samples, some issues were encountered, which may have affected the electrical results. The following SEM images were taken after the SiO_2 field oxide layer was etched away from the fins using BHF. The images were taken in order to see the depth of the etch into Ga_2O_3 and the quality of the etched fins. Following the SEM images, the fins would then be treated with hot H_3PO_4 acid before the ALD HfO_2 deposition, which should improve the quality of the fin sidewalls. In future iterations of the fin MOSCAPs an extra sample will be included to take SEM images before and after the pre-ALD treatment (hot H_3PO_4) to observe how the treatment affects the fin quality without letting the SEM affect the electrical measurements.

Figure 6.15 shows the etched Ga_2O_3 fins from Sample A. A rough pattern and ”strings” between the fins is observed on the etched surface. These features are possibly due to the e-beam resist (ZEP520A) being underdeveloped. An underdeveloped resist could result in these ”strings” being etched into the Si_3N_4 hard mask, which would then be etched into the Ga_2O_3. This was resolved for Sample B by adding a descum step before etching the Si_3N_4 layer. The rough, wavy

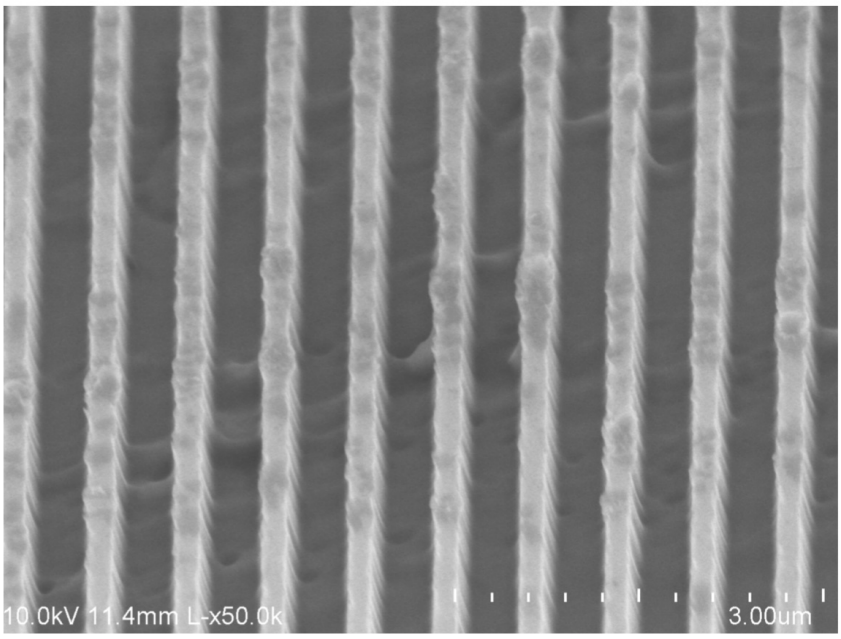


Figure 6.15: SEM of etched β-Ga_2O_3 fins from Sample A, which shows the rough etched surface, wavy sidewalls, and "strings" along the bottom of the fins. The only material shown is Ga_2O_3.

pattern of the sidewalls of the fins may also have been caused by an unoptimized etch of the Si_3N_4 hard mask, which would also transfer into the Ga_2O_3 etch. An improved Si_3N_4 etch recipe is used for Sample B.

The sidewall features of the fins were significantly improved during Sample B's fabrication run as shown in Figure 6.16 (a) and (b) with the improved Si_3N_4 etch process. However, another issue appeared during the Ga_2O_3 etch. Insufficient sidewall passivation occurred during the Ga_2O_3 etch which caused the sidewalls near the top of the 400 nm fins to become rough. The smaller fins widths (200 and 300 nm) experienced very severe undercutting due to this issue causing the fins to be completely etched through. The reason for the insufficient sidewall passivation in Sample B is not yet clear. Due to the low bias power of 25 W, the fin etching process is fairly long, $\sim$ 20 minutes, which may have caused the chamber conditions to shift, resulting in the poor sidewall passivation and undercutting. Additional testing of the Ga_2O_3 etch process will be required to produce smooth, straight sidewalls.

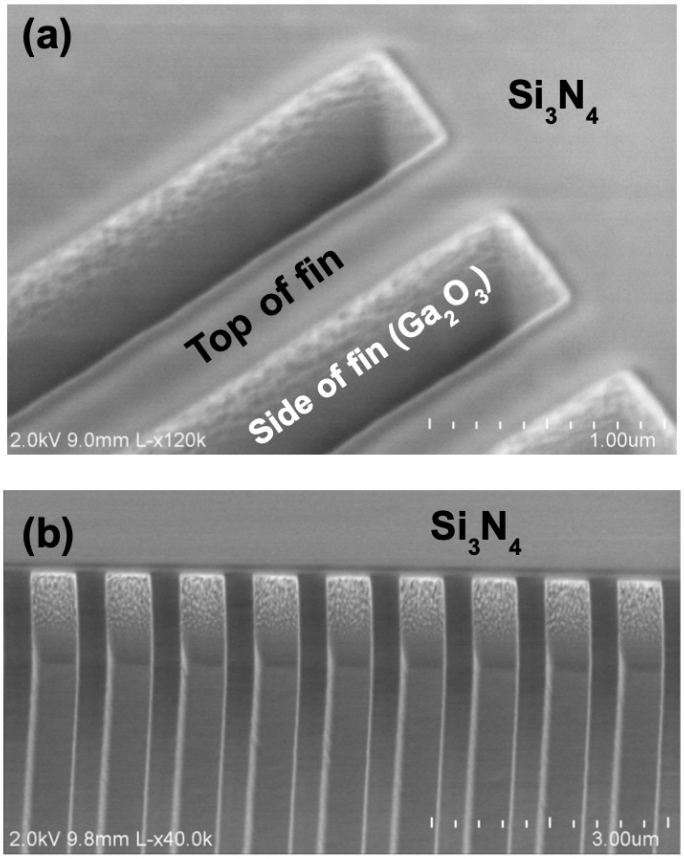


Figure 6.16: (a) (b) SEM images of the etched 400 nm β-Ga_2O_3 fins from Sample B, which shows the rough sidewall near the top of the fins caused by the poor sidewall passivation. The Si_3N_4 hard mask is still covering the etched fins.

6.4 Conclusions

In this chapter a fabrication process for HfO_2/β-Ga_2O_3 fin MOSCAP arrays has been developed and initial capacitance - voltage (C-V) analysis of the ALD HfO_2 interface quality to the plasma-etched β-Ga_2O_3 fin sidewalls was conducted. In the first set of fin MOSCAPs, the effect of the fin width (W_{fin}) on the flatband voltage (V_{fb}) is observed. A W_{fin} of 200 nm results in a V_{fb} of +6 V, while 400 nm W_{fin} results in V_{fb} of -1.5 V. This difference, which correlates to differences in threshold voltage in β-Ga_2O_3 fin MOSFETs, demonstrate the need for thin fin structures in order to achieve enhancement-mode vertical fin-MOSFETs. Variations in C-V shape within the depletion region was also observed when comparing fin MOSCAPs of the two W_{fin}. Using Silvaco Atlas

simulations I show how electrons accumulate within the middle of fin at various voltage biases as a result of the fin architecture. No significant differences in *C-V* are observed in the various fin orientations studied here, but additional fin MOSCAP samples and analyses will be required to further explore this aspect of the fin sidewalls.

From the second fin MOSCAP arrays, the interface quality of the ALD dielectric to the fin sidewalls is examined through *C-V* frequency dispersion and D_{it} analysis. Significant frequency dispersion is observed in the accumulation region of the fin MOSCAPs resulting in the maximum *C* value being doubled at a frequency of 1 kHz compared to 1 MHz. While the physical origin of this *C-V* behavior is not yet clear, it may be attributed to significant density of interface and border traps that impede the full accumulation of the fins. The photo-assisted *C-V* results show a distribution of interface traps which includes a fairly high D_{it} of $10^{12}\ \mathrm{cm}^{-2}\mathrm{eV}^{-1}$ between 1.8 and 0.5 eV below the conduction band with increasing D_{it} as you approach the conduction band. The AC conductance method results also showed a high D_{it} of $4 - 6 \times 10^{12}\ \mathrm{cm}^{-2}\mathrm{eV}^{-1}$ between 0.2 to 0.3 eV below the conduction band. The high D_{it} is most likely attributed to the plasma damage caused during the reaction ion etching (RIE) process that is required to form the β-Ga_2O_3 fins, as also shown by device researchers [50, 107, 108, 110]. These results indicate sidewall interfaces appear to have higher interface state density and frequency dispersion, and more work is needed to understand the physical origin of these phenomena and identify pathways to reduce them. This work demonstrates the ability of use the fin MOSCAP structure and various *C-V* analysis to understand the fin structure which is crucial for the development of enhancement-mode β-Ga_2O_3 vertical power fin-MOSFETs.

CHAPTER 7

Conclusions and Future Work

7.1 Contributions to date

This thesis provides important insight into the relationship between dielectrics and the ultra-wide bandgap (UWBG) semiconductor, β-Ga_2O_3, within metal-oxide-semiconductor (MOS) structures. These dielectric reliability studies are critical for the development of future β-Ga_2O_3 power devices. The following contributions from this work are listed below:

1. I investigated a novel solution-processed ternary dielectric, $(Y_{0.6}Sc_{0.4})_2O_3$, in β-Ga_2O_3 MOSCAPs, and developed a set of techniques to analyze MOS structures with a UWBG semiconductor.

    - The interface quality was studied through the use of multiple interface trap density (D_{it}) extraction methods including the photo-assisted capacitance - voltage (C-V) method. This technique was demonstrated for the first time with β-Ga_2O_3 showing its capability of extracting a D_{it} distribution across a larger portion of the wide bandgap compared to other traditional techniques.
    - Current conduction mechanisms of the $(Y_{0.6}Sc_{0.4})_2O_3$/β-Ga_2O_3 MOSCAPs were also investigated through temperature-dependent current density - voltage (J-V) measurements. The rising forward bias leakage was attributed to bulk-limited transport of majority carrier electrons through dielectric traps near the conduction band, known as

modified Poole-Frenkel emission. In contrast, reverse (or depletion) bias leakage current is governed by generation of holes from deep-level Ga_2O_3 traps.

2. For the first time, the reliability of ALD HfO_2/β-Ga_2O_3 MOSCAPs was tested using positive bias stress, and the results were compared to ALD HfO_2/Si MOSCAPs. The comparison to Si MOSCAPs enabled the investigation of how charge trapping in dielectrics is affected by the UWBG semiconductor.

    - It was observed that β-Ga_2O_3 MOSCAPs are more susceptible to charge trapping at lower electric field stress biases compared to smaller bandgap semiconductors.
    - During initial *C-V* sweeps, border traps in the HfO_2 play a significant role in charge trapping for the β-Ga_2O_3 MOSCAPs due to the lack of recombination from mobile holes in the semiconductor.
    - Lastly, I showed full recovery from stress-induced charge trapping with 0V bias and deep ultra-violet (DUV) illumination, due to the recombination of photo-generated holes, from the semiconductor, with the trapped charges in the dielectric.

3. The effects of a dielectric's negative valence band offset (ΔE_v) with β-Ga_2O_3 was investigated for the first time, in Chapter 3 with $(Y_{0.6}Sc_{0.4})_2O_3$ and in Chapter 4 with HfO_2. Due to the self-trapping behavior of holes in β-Ga_2O_3, the type-II band alignment with a negative ΔE_v has not been of previous concern among the community. In both cases, reverse bias photo-current was observed indicating that previously trapped holes can be excited by DUV illumination and can contribute to current leakage with the help of a depletion bias and absence of a hole barrier. The negative ΔE_v may have also contributed to the expedited recovery from stress-induced charge trapping with illumination that was observed with HfO_2.

4. For the first time, the impact of high temperature annealing was studied on the ALD HfO_2/β-Ga_2O_3 interface and diffusion of Ga atoms into the HfO_2 dielectric was observed after annealing at 900°C. Secondary ion mass spectrometry (SIMS) results showed negligible Ga

diffusion into the dielectric at 850°C and below, but MOSCAP electrical results indicated an increase in forward bias leakage and interface trap density after annealing at 700 °C compared to MOSCAPs which only experienced annealing processes below 500°C. The significant Ga diffusion into the HfO_2 resulted in a degraded dielectric quality that did not provide sufficient electrical insulation for the UWBG semiconductor. Future β-Ga_2O_3 devices need to be both electrically and thermally reliable, and a stable dielectric/semiconductor interface is essential to achieve this. Many processes within device fabrication requires high temperature processes, including post-ion implant anneal and epilayer regrowth. My results will be helpful for device researchers to understand the impacts of these high temperature processes on the MOS structure.

5. A β-Ga_2O_3 fin MOSCAP array fabrication process has been developed and initial *C-V* analysis has been performed to investigate the interface between ALD HfO_2 and the etched β-Ga_2O_3 fin sidewall. The β-Ga_2O_3 fin sidewall's D_{it} energy distribution was extracted for the first time using the photo-assisted *C-V* method. These results showed a higher density of interface traps in the mid-bandgap region compared to the previous studies presented in this thesis, possibly due to the plasma damage from the Ga_2O_3 etch. This work demonstrates the ability to use a fin MOSCAP structure to analyze the sidewall interface quality, which can be used in future studies to achieve a reliable MOS sidewall structure, and therefore, improved β-Ga_2O_3 fin-MOSFETs.

7.2 Future Work

This investigation into dielectric reliability with β-Ga_2O_3 will be beneficial for device researchers as they seek to develop high-performing, reliable power MOSFETs with this exciting UWBG semiconductor. Still future studies will be necessary to develop the best MOS structure for these future devices. A few suggestions of future work are listed below, which could help continue to expand our understanding of dielectrics with β-Ga_2O_3 and result in a superior MOS β-Ga_2O_3

structure for future power devices.

1. **Investigate alternative atomic layer deposited (ALD) dielectrics for improved MOS reliability with β-Ga_2O_3:** Much of the focus in this thesis was on the reliability of ALD HfO_2 with β-Ga_2O_3; outside of this work, ALD Al_2O_3 and SiO_2 have been the most frequently used dielectrics with β-Ga_2O_3. While the large bandgap of β-Ga_2O_3 limits the options of high-κ dielectrics, there are other dielectrics that may provide a better interface in these MOS structures.

    - **ALD $HfSiO_4$** may be a great option as a dielectric for β-Ga_2O_3 as it would provide the benefits of HfO_2's high dielectric constant and SiO_2's large bandgap. This dielectric can be formed with alternating ALD cycles of HfO_2 and SiO_2. The band alignment of this ternary dielectric to β-Ga_2O_3 was measured with X-ray photoelectron spectroscopy and the conduction band offset was determine to be 2.38 eV [115]. This resulting large conduction band offset may help minimized charge trapping under positive bias stress, which was observed with ALD HfO_2 in Chapter 4. Also ternary dielectric tend to have higher crystallization temperatures compared to many binary dielectrics [61]. As shown in Chapter 5, HfO_2 easily crystallizes at temperatures below 500°C. A ternary alloy of HfO_2 may provide a more thermally stable interface to β-Ga_2O_3.
    - **ALD $(Y_{0.6}Sc_{0.4})_2O_3$** would be another interesting ternary dielectric to try with β-Ga_2O_3. In Chapter 3, the compatibility of solution-processed $(Y_{0.6}Sc_{0.4})_2O_3$ to β-Ga_2O_3 was explored and showed very promising results for an unoptimized deposition method. ALD is the preferred deposition method for gate dielectrics to produce a thin, conformal film, which is necessary for nonplanar structures like fin-MOSFETs. ALD $YScO_3$ has been demonstrated to have a high dielectric constant of 14-16 and low leakage [71].

2. **Improve fin MOSCAP fabrication process to minimize sidewall defects due to plasma etching used to form the fin:** The fin-MOSFET structure is the current front-runner for achieving enhancement-mode vertical β-Ga_2O_3 MOSFETs. This structure uses a vertical

MOS structure along the sidewalls of the fins to control the current flowing through the vertical device without the need of p-type doping, which is currently not available with β-Ga_2O_3. In Chapter 6, a fabrication process for fin MOSCAPs was developed and various *C-V* techniques were used to analyze the sidewall interface between the etched β-Ga_2O_3 and the ALD dielectric. There are several scientific questions that should be addressed in future studies which will help lead to improvements in the dielectric reliability of β-Ga_2O_3 fin MOSFETs. A few of those questions, along with suggested experiments are listed below.

- Which substrate orientation and fin orientation combination provides the highest quality interface (lowest D_{it}) to the ALD dielectrics? While no significant differences are observed between different fin orientations in this study, due to the poor dielectric film quality in the fin MOSCAPs, more work is needed to confirm these preliminary results. Studies on fin Schottky barrier diodes and finFETs showed improved device characteristics when the fin was oriented along the [010] direction on an (001) β-Ga_2O_3 substrate [5, 112]. If there are differences in interface trap densities when comparing fins aligned to different crystal orientations, are these differences inherent to the material or can these defects be suppressed with the right post-etching treatment?
- This leads to the next question of, which post-etching treatments are necessary and the best at removing the plasma damage on the sidewalls of the etched β-Ga_2O_3 fins? In Chapter 6 hot phosphoric acid (H_3PO_4), at a temperature of 80°C for 10 minutes is used to improve the sidewall quality after plasma etching, following [110], but there are many other acid treatments that can be tested, including using a higher temperature for the H_3PO_4 etch which would more aggressively etched the sidewall of the fins as shown by [116]. Annealing treatments may also help reduce the sidewall defects and therefore lower D_{it}, as diode characteristics have shown to improve from their degraded plasma-etched state after annealing at 400 and 450°C for 10 minutes [109]. This analysis will require many fin MOSCAP samples of the same structure with only the post-etching/pre-ALD treatment varying. Various C-V and current density - voltage

(J-V) analyses, including D_{it}, frequency dispersion, positive bias stress, and breakdown, can be used to determine which method is the best for forming reliability vertical MOS structures along these etched sidewalls.

- Lastly, only BCl_3/Cl_2/Ar etch chemistry was used in Chapter 6 to form the β-Ga_2O_3 fins. The poor selectively to photo-resist resulted in the need of a Si_3N_4 hard mask, and the removal of the remaining hard mask was shown to be difficult. It may be beneficial to investigate other etch chemistries which have a higher selectivity to photo-resist. GaN etching with BCl_3/HBr chemistry has been demonstrated have a selectivity of 1.6 while maintaining a high GaN etch rate [117]. This BCl_3/HBr chemistry might work for etching β-Ga_2O_3 and would remove the need of the Si_3N_4 hard mask. This could possibly result in improved fin structures, but would require significant etch characterization and optimization. Using a different etch chemistry could result in different sidewall defects, which would also need to be characterized using a fin MOSCAP structure.

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