Power Converters Optimization for Electrified Transportation Applications

by

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DEDICATION

This dissertation is dedicated to...

My Parents

Bakhat Gul and Ziarat Gul

and

My Wife

Laila

ACKNOWLEDGEMENTS

All praise is to Allah, the Most Gracious, the Most Merciful

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I will conclude with *"Persistence is the key to achieving your dreams."*

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ABSTRACT

The recent advancements in the power electronics and semiconductor domain, aided by its competitive advantage against traditional power conversion, have resulted in new research avenues utilizing power electronics converters. Power electronics converters are the backbone of an electrified transportation system, which is pivotal to curb climate change and achieve a sustainable mode of transportation. This research aims to step up and optimize the current power converters for electrified transportation applications to achieve enhanced power and energy density, performance efficiency, reliability, and dynamic stability, which will help to raise the electrification factor. It covers the broader domain of electrified transportation, which includes small mobility, electric vehicles, electric aviation, etc., to broaden the impact of this research on the community. Multiple new approaches, such as bare-die embedding technology, modern thermal management techniques, planar magnetics, wide-bandgap electronics, and modern control theory, are applied to advance and accelerate the electrification revolution.

CHAPTER 1

Introduction

1.1 Introduction to Electrified Transportation

Electrified transportation is considered as a major breakthrough in tackling the global climate change and Carbon emissions. Electric Vehicles are the backbone of the transition towards clean energy and to meet the zero-emission targets [3]. The transportation sector is responsible for contributing 24% to the global carbon emissions [4], and vehicle transport directly emits 70% of the emissions [5]. To reduce these emissions and to slow the threats of world climate change, electrified transportation in general and electric vehicles (EVs) in particular have attained great attention due to their zero emissions operation, low noise, improved performance, and efficiency. The U.S. government mandates that the average fuel economy of a passenger car should rise to 54.5 miles/gallon by 2025 [6]. These targets cannot be achieved by using the internal combustion engine technology. Instead, electric machines driven by power electronics converters can provide such higher efficiencies. Therefore, electrification is the only way forward. Electrified transportation vision includes utilizing more electrical energy to power traction and non-traction loads in the vehicle. It is still a hot research and development area due to the various technical challenges the EV industry is facing such as battery cost, charging infrastructure, power electronics reliability and converter's functionality in the drive train. Specifically, the challenges in the power converter's domain include a large number of components leading to low power density, high current stress, high switching loss, slow dynamic response, and computational complexity [7]. Moreover, Power Density and cost are the key design criteria for the modern power electronics unit in Electric Vehicles (EVs). However, the vertical space on the chassis for charging electronics is very limited. Moreover, with a non-compact package comes a high damaging probability due to unpredictable road conditions, higher costs, and vehicle integration issues.

Markets for electric cars are expanding exponentially, with sales expected to reach 10 million by 2022. In 2022, 14% of all new automobiles sold were electric, an increase from

less than 5% in 2020 and approximately 9% in 2021. Global sales were led by three markets. China led the way once more, making up over 60% of sales of electric vehicles worldwide. China currently has more electric vehicles on the road than any other country, and the nation has already surpassed its 2025 new energy vehicle sales target. Sales of electric cars rose by more than 15% in 2022 in Europe, the second-largest market, indicating that more than one in five vehicles sold there were electric. The third-largest market in the world, the United States, saw a 55% growth in electric vehicle sales in 2022, reaching an 8% market share. Sales of electric vehicles are predicted to rise significantly through 2023. In the first quarter, over 2.3 million electric automobiles were sold, which represents a 25% increase over the same period the previous year. By the end of 2023, we project sales of 14 million, a 35% annual growth, with new purchases picking up speed in the second part of the current year. Accordingly, during the course of the entire calendar year, sales of automobiles might be made up of 18% electric vehicles. Figure 1.1 shows the global increasing EV sales scenario and the share of the big three markets in terms of EV registrations [8].

Road transportation is becoming more electrified than just autos. Nowadays, two- and three-wheelers are the most electrified market sector; in developing and growing nations, their numbers exceed those of vehicles. In 2022, over half of all three-wheeler registrations in India were electric. This indicates that electric vehicles are becoming more and more popular because of government incentives and their cheaper lifespan costs as compared to conventional models—especially in light of rising fuel prices. In 2022, the global sales of light commercial vehicles (LCVs) had a fall of over 15%, but the number of electric cars sold surged by over 90% to over 310 000 units. Approximately 66,000 electric buses and 60,000 medium- and heavy-duty trucks were sold globally in 2022, accounting for 1.2% of vehicle sales and approximately 4.5% of all bus sales. Electric bus sales have increased to even larger percentages in places where governments have pledged to cut emissions from public transportation, such as in crowded urban regions. In Finland, for instance, electric bus sales accounted for more than 65% of total sales in 2022 [9]. Figure 1.2 presents the small mobility share and market performance [8].

Although investors and financial markets continue to express optimism in the electric vehicle (EV) industry, 2022 proved to be a challenging year for EV startups. Over the past few years, even during the COVID-19 pandemic, the stocks of EV-related companies have shown amazing growth, routinely surpassing traditional carmakers since 2019. Growth, however, stalled in 2022, and financial markets were rationalized in the face of more intense competition (particularly in China, where there is a downward price war for electric cars), higher inflation rates, supply chain disruptions, and increased risks. As a result, the gap between established automakers and pure-play EV businesses has shrunk. EV firms' market

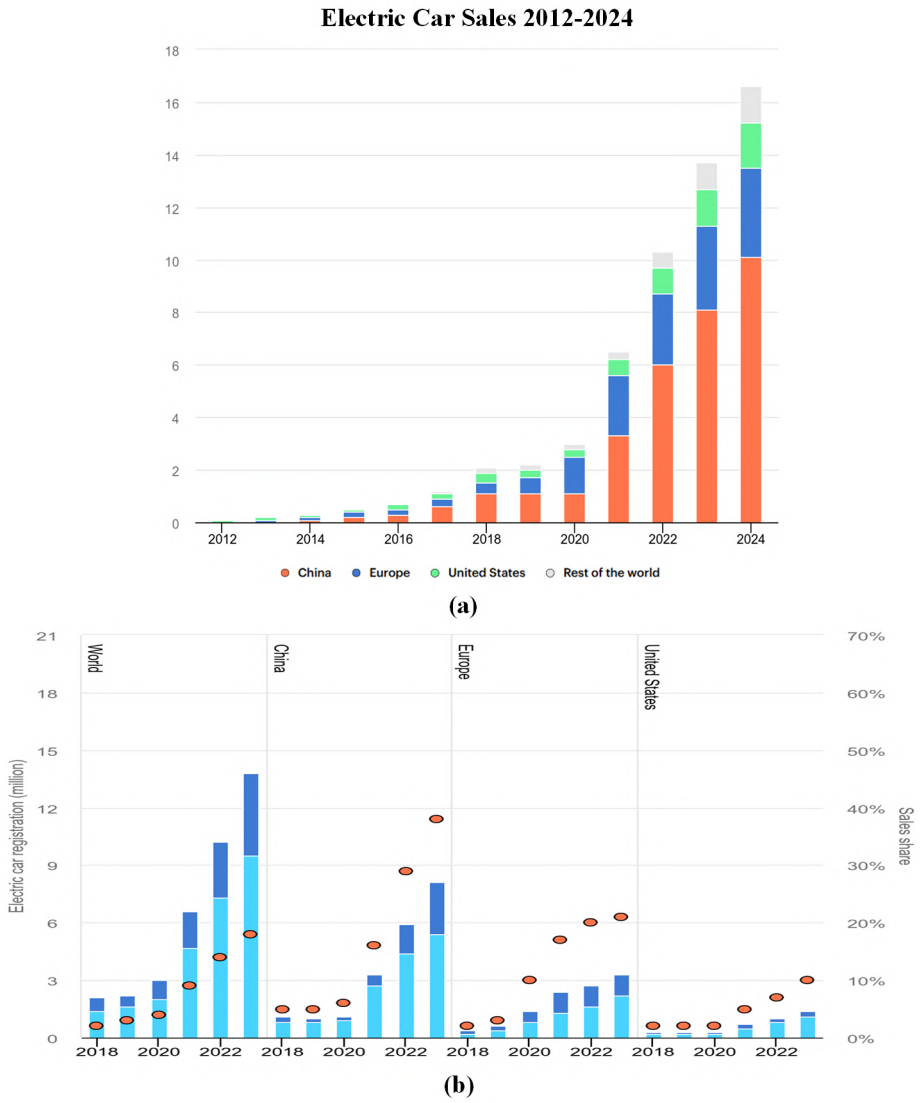


Figure 1.1: (a) Global EV Sales Data(b) Three Biggest Regions EV Registration Data

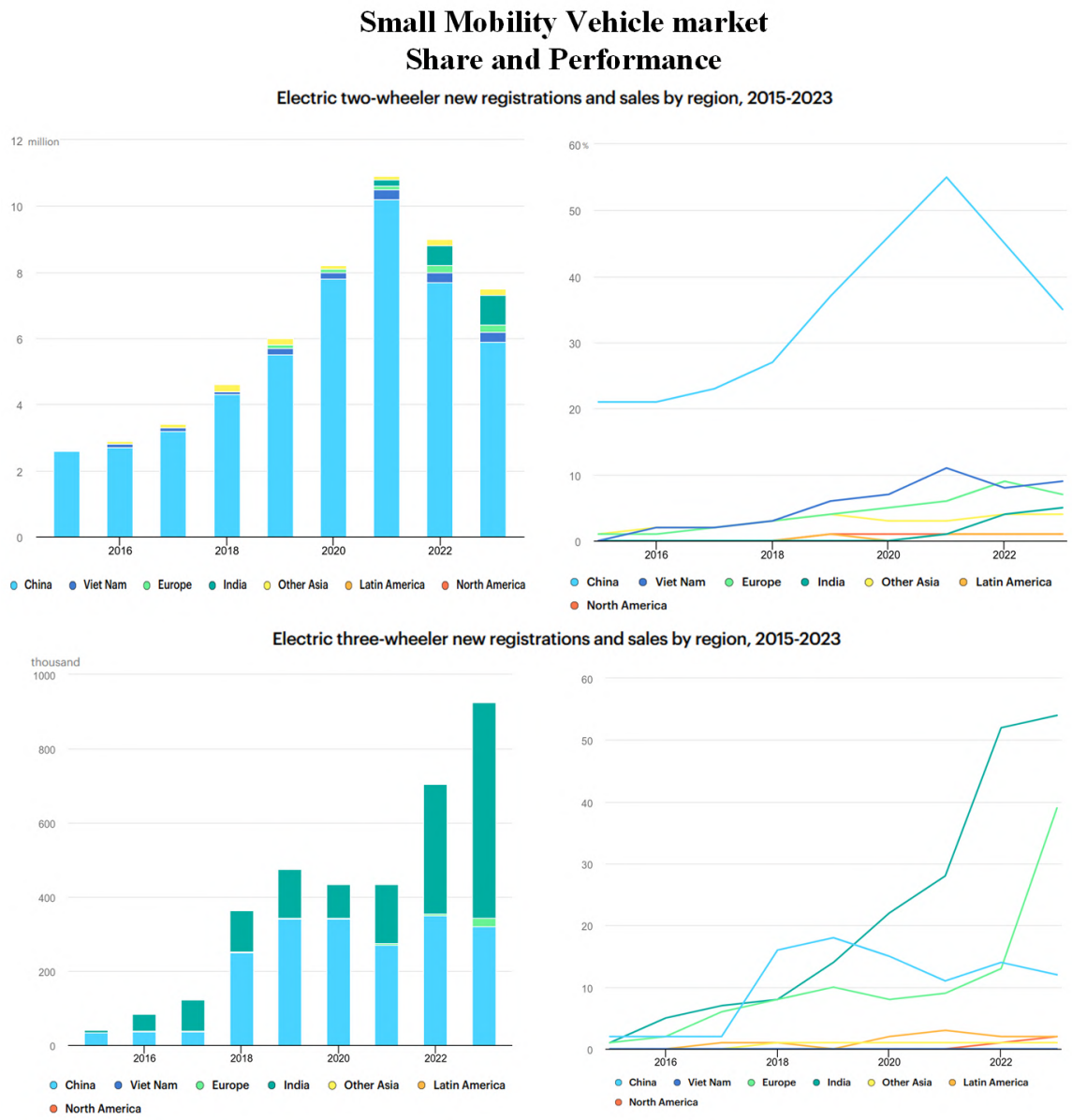


Figure 1.2: Global Small Mobility Vehicles Sales and Market Share

capitalization had a significant decline in 2022, following an all-time high at the end of 2021. The company's market capitalization dropped by around USD 870 billion between its high at the end of 2021 and early 2023, more than the combined valuation of the top 10 established automakers at that time as shown in Fig 1.3 [9]. The goal of producing low-cost vehicles is only possible through the advancement and optimization of the power converters for high efficiency, low losses, low component count, and high power density, which is the focus of this research.

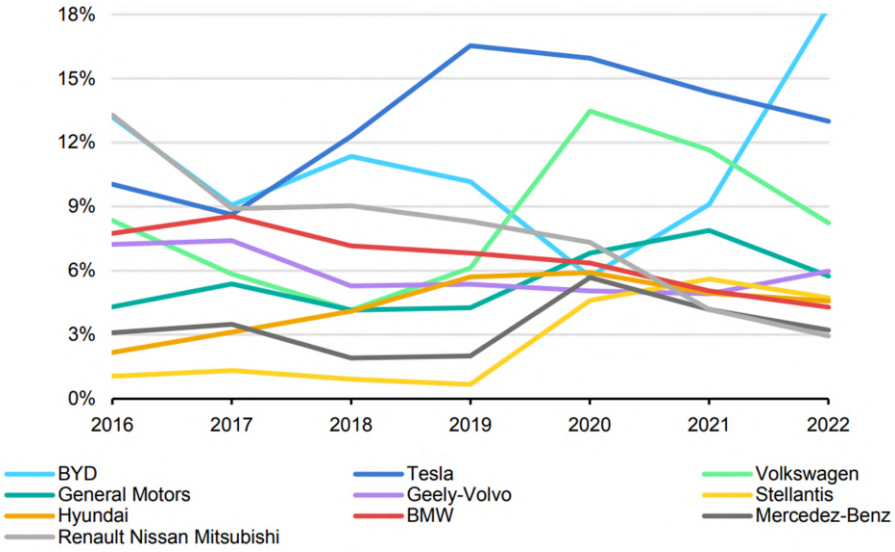


Figure 1.3: Global Market Share of EV Manufacturers

1.2 EV Charging Network: A Challenge

Depending on how much electricity is utilized as an energy source, there are three types of electric cars. In hybrid electric vehicles or HEVs, the battery and internal combustion engine are combined. An IC engine primarily powers the car, while battery power occasionally boosts performance. Regenerative braking is how the HEV's battery is charged. Regarding fuel efficiency, HEVs outperform cars with internal combustion engines. A plug-in hybrid vehicle, or PHEV, is comparable to a HEV because it has an internal combustion engine and a battery. On the other hand, a PHEV's battery is charged by connecting it to the grid. Because of this, a PHEV's battery has sufficient capacity to serve as the car's main energy source. The battery is the only source of electricity used by PHEVs. On longer routes, however, the car switches to the internal combustion engine if the battery state of charge (SOC) drops below a certain level. A PHEV can operate on daily short-range drives

without using the internal combustion engine's power. Without sacrificing the benefits of an internal combustion engine vehicle, PHEVs provide all the environmental advantages of PEVs. Because they lack an internal combustion engine, battery electric vehicles (BEVs) depend entirely on electricity. Battery electric vehicles (BEVs) have rechargeable batteries that can be charged by grid connection. BEVs are emission-free, silent, and environmentally benign as they don't have internal combustion engines. Electric vehicles face several challenges, chief among them being their low battery capacity, which leads to a reduced driving range and a protracted charging period. Installing numerous charging stations and installing faster charging equipment at such stations are two ways to solve this issue. Based on the type and level of voltage used, EV chargers can be categorized into three levels: level 1 (one), level 2 (two), and level 3 (three) / DCFC (DC fast charging) [10]. According to the study published by National Renewable Energy Lab an investment of upto $55 billion is required to meet the charging needs of the consumers by 2030 which are 1.2 million public charging ports. The government and private sector investment has boosted the manufacturing and installation of charging stations across the United States as depicted in 1.4 [11]. Range

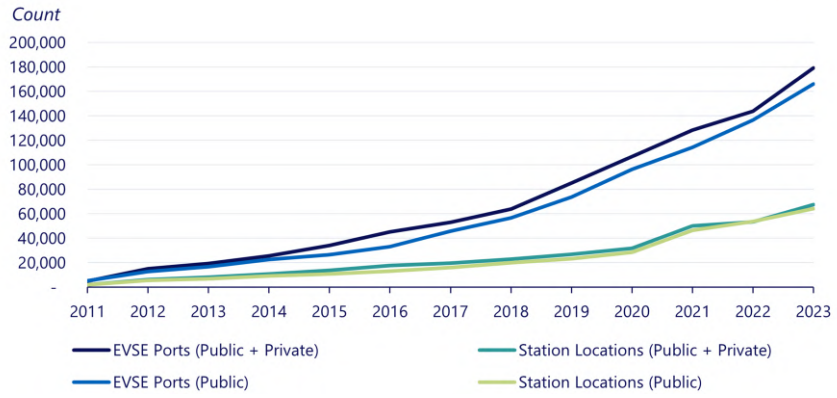


Figure 1.4: EV Charging Infrastructure-USA

anxiety is a major hurdle in today's rapid adoption of electric vehicles globally. As a test case to demonstrate the areas needing electric vehicle charging infrastructure, the National Renewable Energy lab used the EVI-Road Trip tool [12]to model the fast chargers along the highways for long-distance travel. The location of existing DC stations from all the major manufacturers was overlaid on the map for intuitive understanding and regional needs. From Fig 1.5, it's clear that more fast charging infrastructure is required to overcome the problem of range anxiety and persuade customers to adopt EVs [13]. This research verifies a magnetic less three-level power converter topology to upgrade the existing charging stations to 800V modern charging stations so that they can be compatible with the income new 800 architecture EVs, contributing to the expansion and wide use of the charging infrastructure.

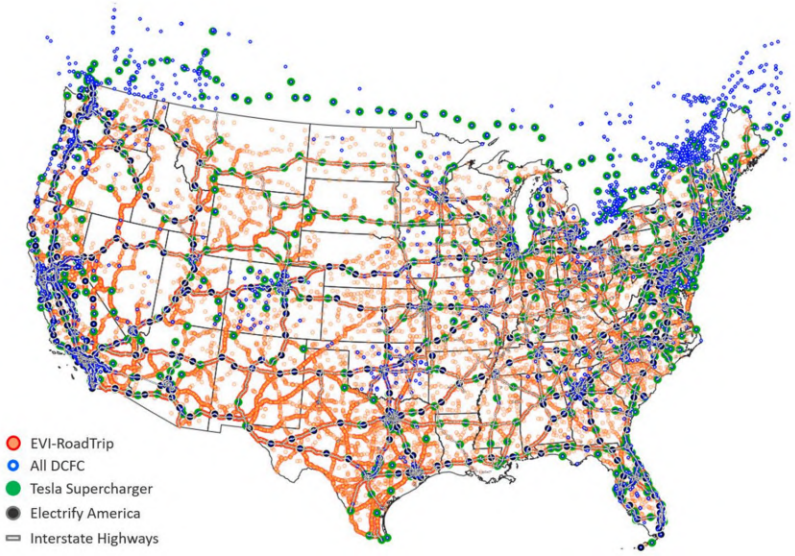


Figure 1.5: Charging Demand Simulated by EVI-RoadTrip Tool vs Existing Charging Infrastructure

Wireless charging is an advanced form of EV charging, which is very convenient but has some technical challenges, such as efficiency and cost. This research focuses on reducing the size of the rectifier inductor used in wireless charging applications. But the concept and technique can be applied to any application, including wired charging, etc.

1.3 Electric vertical take-off and landing (eVTOL) Vehicles

The global trend of urbanization has created challenges such as traffic congestion, longer commute times, and increased carbon emissions especially in urban centers. As a solution, the concept of urban air mobility (UAM) has gained significant traction recently. The UAM vision is to transform the traditional transportation system through aerial transportation that operates above the ground level traffic by utilizing electrical vertical take off and landing (eVTOL) aircraft. This will ensure fast commutes, quite operation, low emissions, and flexibility of take off and landing in an urban space. Data projections show that 68% of the global population will reside in urban centres by 2030 [172], which calls for the need to develop efficient transportation solutions such as eVTOL aircraft that don't contribute to traditional road congestion.The National Aeronautics and Space Administration (NASA) along with other industry leaders have placed UAM as a critical pillar for future smart cities. NASA's UAM Grand Challenge [173] and similar initiatives in Europe [174] and Asia [175]

are accelerating the development of certification standards, air traffic management strategies, and infrastructure requirements for aerial mobility. The major aircraft and aerospace companies, such as Airbus, Boeing, etc., have also conducted various studies to demonstrate that electric propulsion-based aircraft with distributed propulsion enhances the safety, reliability, redundancy and controllability in their Concept of Operations (ConOps) for Uncrewed Urban Air Mobility release [176]. eVTOL vehicles have different kinds of architecture and each of them has specific advantages and disadvantages as shown in 1.6, so the actual adoption of the architecture depends upon the application and nature of intended operation [14].

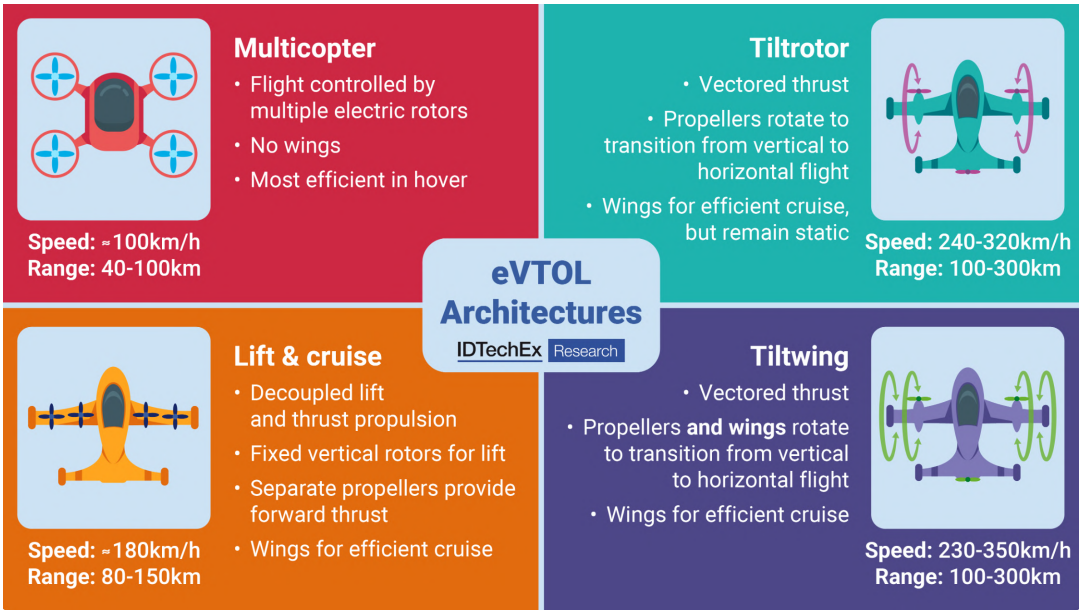


Figure 1.6: eVTOL Aircraft Architectures

Aditionally public and private investments in such startups and ventures have significantly increases with companies like Archer Aviation [176], Volocopter [177], and Vertical Aerospace [178] demonstrating their products and securing billions in funding to develop scalable air taxi platforms. According to market projections, the global UAM market is expected to exceed USD 45 billion by 2030, underscoring its economic and technological importance [172].

The global eVTOL aircraft market size is calculated at USD 2.14 billion in 2024 and is expected to be worth USD 170.60 billion by 2034, expanding at a CAGR of 54.95% from 2024 to 2034 as shown in 1.7 [15].

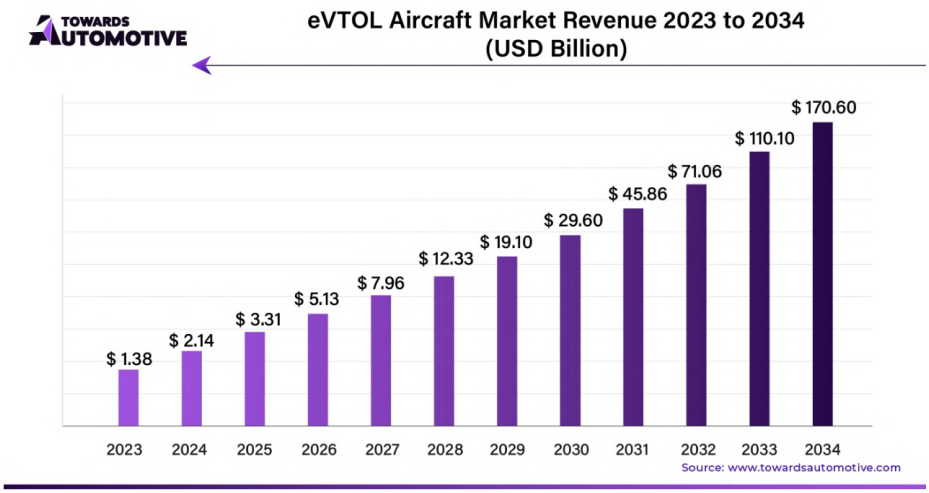


Figure 1.7: eVTOL Aircraft Market Revenue

1.4 Introduction to Power Converters

Power electronics converters are pivotal in modern electrical systems, serving as the backbone for efficient energy conversion and control. These converters are essential in various applications, ranging from renewable energy integration and electric vehicle propulsion to industrial automation. By manipulating the flow of electrical power through switches and semiconductors, power electronics converters facilitate the conversion of voltage, frequency, and current levels to match specific system requirements. Their versatility allows seamless adaptation to diverse loads and power sources, improving energy efficiency, reducing environmental impact, and enhancing system reliability. A power converter can be AC-DC, DC-AC or DC-DC, depending upon the application the converter is to be used for. Electromechanical converters primarily rotating machines were initially used to convert energy. Static power converters are utilized in a wide range of application fields. However, they are particularly useful in accelerators of particles. They perform better both statically and dynamically and have a lower weight and volume. The conversion of the power or voltage level takes place through the switching action of the semiconductor devices such as IGBTs, MOSFET, etc [16]. Figure 1.8 shows the generalized power converter operation structure.

The power converter is the backbone of the electrified transportation system, especially the backbone of the power converter, which is a switch. It is a power semiconductor device that allows and blocks current flow. It is not like a mechanical switch; rather, it turns on and off based on a pulse or a gate signal. Although the power loss associated with an electronic switch is greater than that of a mechanical switch, it has the ability to continuously switch at a very high rate without involving any moving parts. Switches can be classified into three

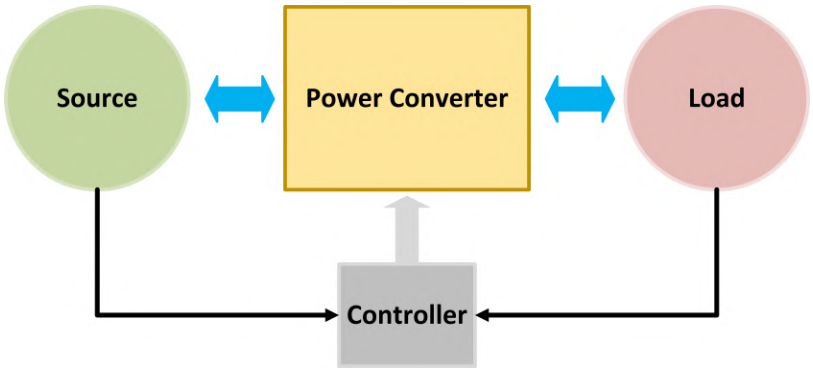


Figure 1.8: Power Converter Structure

categories.

1.4.1 Uncontrolled Switches

Power diode is a type of unchecked switch in which the turning on and off both are not controlled by the user, and it depends on the circuit.

1.4.2 Semi controlled Switches

A thyristor is a semi-controlled switch, which means the user can control when to turn on the switch by using a gate signal, but it cannot be turned off instantaneously by the user.

1.4.3 Fully Controllable Switches

These types of switches can be controlled fully, i.e., turned on and off by the user using the gate signal. These switches have many kinds; the famous one includes Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET), Insulated-Gate Bipolar Transistor (IGBT) and Gate-Turn-Off Thyristor (GTO). MOSFET is used for low-power applications. IGBT is the most suitable form of the modern power system. Due to the semiconductor advancement, It can handle high voltages and currents. That is the reason it is widely used in converters nowadays. GTO is used for specific applications because it requires a pulse of negative current to turn off, which corresponds to power loss.

1.4.4 Wide Band Gap (WBG) Devices

Due to weight, space, and operating environment constraints, power electronics converters used in transportation applications must meet stringent requirements. The mechanical

and/or electrical components of a vehicle have a limited amount of space, so each component must be small and take up as little space as feasible. Additionally, it is anticipated that they will be lightweight to maintain the vehicle's weight restriction. Less strain on the engine and/or motor, quicker acceleration, and more economy are all benefits of a lighter vehicle. More efficiency means using less gasoline or charging batteries. Ultimately, converters need to be highly dependable and reasonably priced in order to be able to operate at high temperatures for extended periods of time without experiencing any problems. Wide bandgap semiconductors, such as silicon carbide (SiC) and gallium nitride (GaN), are revolutionizing the electric vehicle (EV) industry with their remarkable performance characteristics and efficiency gains. These materials offer superior properties to traditional silicon-based semiconductors, including higher breakdown voltages, faster switching speeds, and lower on-state losses. In the context of EVs, these advantages translate into more efficient power conversion, reduced system size and weight, and extended driving range. SiC and GaN devices enable higher switching frequencies, allowing smoother operation and minimizing electromagnetic interference. Moreover, their high-temperature capability enhances the thermal management of EV powertrains, enabling greater power density and reliability. As the demand for EVs continues to soar, wide bandgap semiconductors are poised to play a crucial role in advancing the performance and efficiency of electric propulsion systems, accelerating the transition towards a sustainable transportation ecosystem. The reason for the associated advantages of the identified WBG materials is due to the difference in the required band energy as shown in Table 1.1 [17]. Electrons in a material have different energy levels that come together to form energy bands. The term "conduction band" refers to the top band, while "valence band" refers to the next lower band. The forbidden band is the area where, ideally, there are no electrons and it is located between the valence band and the conduction band. The energy band gap diagram is presented in Fig 1.9.The valence band electrons have the ability to migrate to the conduction band upon external excitation. Their energy is Ev in the valence band. They require an $Eg = Ec - Ev$ quantity of energy, where Eg is the bandgap, in order to progress to the conduction band. The energy bands overlap and the forbidden band is absent in a conductor such as copper. In contrast, this band is so large for an insulator that it takes a lot of energy for electrons to go from the valence band to the conduction band. The prohibited band gap is smaller in semiconductors than in insulators.

GaN and SiC are compound semiconductors with band-gaps about three times larger than silicon's 1.12 eV (electron volts), at 3.39 eV and 3.26 eV, respectively. This indicates that while there are a lot of distinctions between the two technologies that affect how they function and where they are utilized, both can sustain higher voltages and frequencies.GaN and SiC differ from one another in terms of electron mobility, or the rate at which electrons

Property	Si	SiC (4H)	GaN	Diamond
Bandgap Energy (ev)	1.1	3.26	3.45	35.45
Dielectric Constant	11.9	10.1	9	5.5
Breakdown Field (KV/cm)	300	2200	2000	10000
Electron Mobility (cm^2/V_s)	1500	1000	1250	2200
Hole Mobility (cm^2/V_s)	600	115	850	850
Thermal Conductivity $(W/cm-K)$	1.5	4.9	1.3	22
Thermal Expansion $(10^-6(K)$	2.6	4.2	5.6	$1-2$

Table 1.1: WBG Properties Comparison

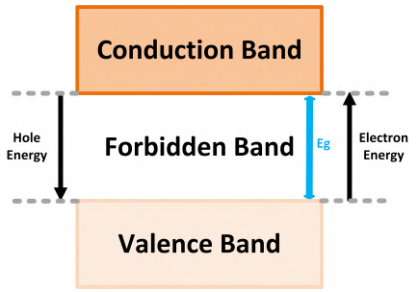


Figure 1.9: Energy Band Diagram

may pass through semiconductor materials. GaN's electron mobility is 30% faster than silicon's at 2,000 cm^2/Vs, whereas SiC's electron mobility is 650 $cm2/Vs$.For example, GaN's increased electron mobility makes it considerably more appropriate for high-performance, high-frequency applications; this is further reinforced by the fact that the gate electrode really occupies a very, very small portion of the chip. Because of the extremely low capacitance that is ensured, reaching higher frequencies is simple [18]. Conversely, SiC is better suited for higher-power applications due to its higher thermal conductivity and lower operating frequency. These applications include the higher voltages needed in data centers and electric vehicles, certain solar power designs, wind turbines, rail traction, grid distribution, and industrial and medical imaging. These applications may not always require high-frequency switching, but they do require higher voltage operation and better heat dissipation, summarized in Fig 1.10 [19].

1.5 Optimization of Power Converters

The design goals of today's power converters are low cost, high efficiency, and high power density. The methods and efforts to improve all these goals fall into the optimization category. For electric cars, power converter optimization is essential to improving the efficiency,

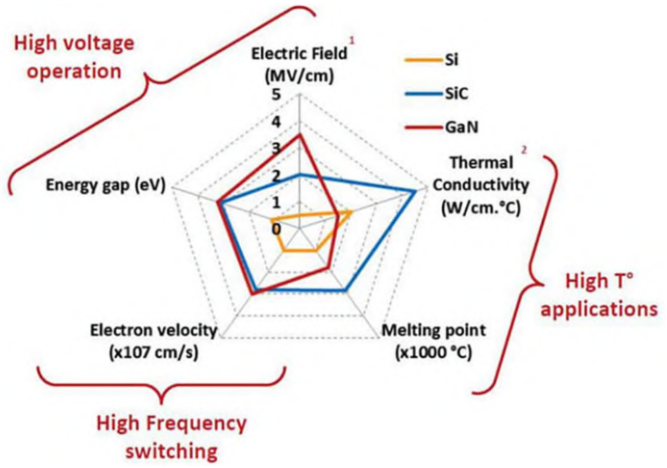


Figure 1.10: WBG Design Parameters Summary

performance, and overall sustainability of the vehicle. Power converters are essential for controlling the electrical energy transfer between an electric vehicle's (EV) battery pack and propulsion system. These converters are optimized through complex design considerations that strive to minimize losses and overall system weight while optimizing energy conversion efficiency. To accomplish these, a variety of methods are used, including high-frequency switching topologies, sophisticated control algorithms, and the integration of wide-bandgap semiconductors like silicon carbide (SiC) and gallium nitride (GaN). Moreover, optimization efforts cover system-level integration, thermal management techniques, and compatibility with new charging infrastructure standards in addition to individual converter components. EVs can gain longer range, quicker charging periods, and less environmental effect by improving power converter design and implementation. This will hasten the adoption of sustainable transportation options. The purpose of this thesis is to investigate new efforts in power converter optimization for electrified transportation applications by addressing the bottleneck challenges and designing a solution for them. In this research, multiple aspects of the power converter optimization were targetted as summarized in 1.11.

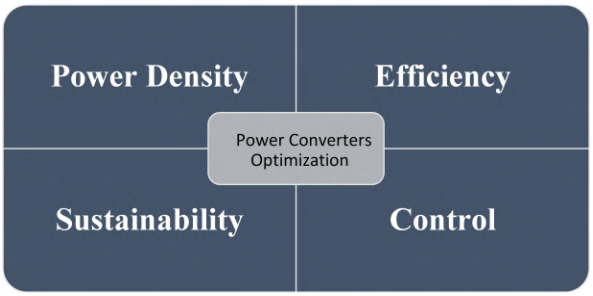


Figure 1.11: Power Converter Optimization Areas

According to the report on the road map Electrical and Electronics Technical Team Roadmap by the US Department of Energy [20] which Pre-competitive research and development (R and D) is the main emphasis of the Roadmap to facilitate more vehicle electrification. Every cutting-edge technology should ideally be scalable and modular to increase its range of uses. The Electric Traction Drive System (ETDS's) technological goals for 2025 are determined by what EDVs must have to compete with ICE vehicles in both performance and cost. Early-stage research will need to provide significant technological advancements to meet these ambitious goals. Achieving high-volume production and lowering the United States petroleum use requires the capacity to bundle power electronics and electric motors across a variety of vehicle types in an effective manner. To facilitate the wider acceptance of these vehicles, the EETT metrics concentrate on important concerns about component size and cost. The data are normalized into power density (kW/liter) and cost per kilowatt based on a system or component peak power rating. Due to the restricted space on the car in general and "under the hood," power density is a highly essential aim. Packaging requirements differ depending on the type of vehicle: in PHEV architectures, a secondary drive train, high-voltage battery, DC/DC converter, and on-board charger must all be added to a conventional ICE vehicle; in BEV applications, on the other hand, space requirements are different, mainly due to the large battery size and small vehicle footprint required to achieve an acceptable driving range (200 miles for 2020 and more than 300 for 2025). For all EDV applications, the 2025 technological targets listed in 1.2 are suitable. Previously, the targets were set at a 55 kW power level when the focus was on Hybrid Electric Vehicles (HEV) applications. Since targets were established, vehicle mass has increased, and to match consumer vehicle performance expectations, full Electric Drive Vehicle applications require higher power levels. The aim consists of one traction-drive electric motor and high-voltage power electronics (one inverter and a boost converter, if necessary). The modular chassis technique is being used by automakers creating long-range BEVs, where the energy storage and ETDS are integrated into the flat chassis, analogous to a skateboard. The chassis can be expanded to fit cars of different sizes, depending on how much energy storage is required. The 2025 annual manufacturing volume assumption rises to 500,000 units due to this design change that permits multi-platform use. Previously, traditional ETDS manufacturing levels were based on conventional automobile manufacturing standards of 100,000 yearly production units.

Year	2020	2025	Change
Cost ($/KW)	8	6	18% cost reduction
Power Density (KW/L)	4	33	$88\%volumereduction$

Table 1.2: Electric Traction Drive System (ETDS) Technical Targets

1.6 Research Significance

This research is focused on power converter optimization, which in the field of power electronics translates to improving the power converters in the aspects of power density, efficiency, and robust control. Power electronics converters utilized to convert power from one level to another are the backbone of almost every industry, especially the electric vehicles or electrified transportation industry, which is in dire need of advancements in the field of power electronics converters to accelerate the electrification revolution. A significant amount of energy is wasted during the power conversion process due to the overall low efficiency of the electronics system. Improving the power converter's efficiency is essential to enhance the overall performance and reduce energy waste. To contribute to and advance this field of knowledge, ensuring sustainable and energy-efficient electric transportation requires a broad skill set, including optimizing power converter topologies, designing advanced control algorithms, exploring new and efficient semiconductor devices to achieve higher efficiency, magnetics design, and modern electronics packaging techniques. Global energy consumption can be reduced significantly by implementing efficient power electronics technology. Due to its widespread applications, power electronics has become a very important and essential field for economic growth, industry advancement, and technological advantage. It is also considered the backbone to realize the increasing influx of renewable energy and electrification of the transportation sector. Advancements in power electronics converters directly impact the community, leading to environment-friendly, low cost and performance-efficient systems or products. Moreover, my research work is crucial and directly in line to achieve the Department of Energy (DOE) 2025 goals for the Electric Traction Drive Systems (ETDS) development at a cost of $\$6/kW$ for a 100-kW peak system. In addition, the program has a 2025 power density target of 33 kW/L for a 100-kW peak system, which translates to 18% cost reduction and 88% volume reduction. Considering these targets, this research on the bare-die embedding technology, new high power density geometry design for inductors, Planar magnetics, and wideband gap semiconductor-based converters are a significant step towards achieving these national goals. Moreover, the National Charging Network report anticipated 30–42 million EVs on the road by 2030, for which a network of EV charging infrastructure is required. My research work on the development of a fast charging con-

verter for 800V EV traction battery, proposing a new DC-DC power converter topology to upgrade the existing charging stations and Multi-source EV charging, is in line with the advancements required to achieve these national targets and build an (EV) charging network that will reach the farthest corners of the nation, helping to make convenient, reliable, and affordable charging a reality.

This thesis is organized as follows: Chapter 1 provides detailed background on power electronics for electrified transportation technology along with the latest industry trends, market growth, technical targets, and theoretical fundamentals. It also highlights the research significance and the need for this research aligning it with the industrial demand and global electrification goals.

Chapter 2 covers the high power density magnetics design which includes two approaches; a distributed magnetics approach and the preposition of a new Star shape three-phase inductor geometry. The distributed approach is especially discussed regarding the hybrid electric vehicles platform and also provides insights into design space optimization and multi-objective optimization. The Star inductor geometry contributes to an increased power density and magnetic performance for an interleaved converter in an electric vehicle.

Chapter 3 includes the new bare-die embedding technique to design highly efficient and high-power-density PCBs for EV applications. It includes the design process, design rules, design framework, and detailed analysis of the proposed technique which includes parasitic analysis, power density comparison, thermal modeling and analysis, and efficiency comparison with the benchmark product. This proposed technique offers promising results and is a good candidate for designing future high-power power electronics for transportation applications.

Chapter 4 focuses on the development of a very compact and high power density on-board charger for small mobility applications using a custom-designed planar flyback transformer having interleaved winding arrangements for low power loss profile ensuring better thermal performance. The integration of the OBC in the vehicle solves the problem of range anxiety and contributes towards the adoption of electric vehicles.

Chapter 5 focuses on the design of a very high power density and highly efficient GaN-based motor drive design for electric vertical take-off and landing (eVTOL) or agricultural drones that have a payload application. It includes a detailed design framework to optimize the parasitic of the PCB layout, which is vital for the GaN operation. Moreover, the thermal design, including the effect of the air during the flight, is considered to optimize and minimize the heatsink requirements. A performance comparison with the state-of-the-art design was carried out to establish the supremacy of the GaN-based design.

Chapter 6 conclusion summarizes the key findings and investigation of this research along

with the results achieved that resulted in the technology improvement. Moreover, the future potential research areas have also been highlighted.

CHAPTER 2

High Power Density Magnetics Design

2.1 Integrated Super Planar Inductor-Rectifier Design for EV Drive

2.1.1 Introduction

Power Density and cost are the key design criteria for the modern power electronics unit in Electric Vehicles (EVs). EVs widely adopt inductive wireless charging technology, which contains the receiving coil and the AC-DC converter on the vehicle side. However, the vertical space on the chassis for charging electronics is very limited. Moreover, with a non-compact package comes a high damaging probability due to unpredictable road conditions, higher costs, and vehicle integration issues. This research presents the concept of distributed planar magnetics with the integrated rectifier hardware design for the vehicle side charging electronics by combining the concept of planar-distributed magnetics with the design space optimization research. A planar-distributed inductor module consisting of 16 EI cores with PCB- embedded windings was designed, modeled (using a novel high-fidelity model), and fabricated using the design space optimization technique, which resulted in a 66% increase in the power density. This research treated and solved the power density problem as an optimization problem considering every constraint involved and presented a thorough investigation from the design space utilization, power loss, loss and frequency relation along with the magnetostatic and electrostatic analysis perspective. It also provides a comparative study of various materials for the inductor fabrication keeping in view the automotive application environment. Moreover, a hybrid approach (metalcore and FR4) PCB was used instead of a regular FR4 PCB after an in-depth study and performance comparison.

Electrified transportation is considered a major breakthrough in tackling global climate change and Carbon emissions. Electric Vehicles are the backbone of the transition towards clean energy and meet the zero-emission targets [21]. Recently EVs have been developed

significantly in terms of performance and drive range. However, EVs' current global charging infrastructure cannot meet the demand. The development of plug-in hybrid and battery electric vehicles demands charging infrastructure. The goal is to replace conductive charging with wireless charging, and the long-term objective is to power the moving vehicles on the road. Once accomplished, it will result in a light battery pack but an extended driving range. The charging technology can be divided into wired or contact charging and wireless or non-contact charging. The first is a traditional and mature method, while the wireless technique is a new technology. Usually, radio transmission technology is utilized for wireless power transfer (WPT)[22]. Radio transmission technology can transmit energy in three ways: inductive transfer, resonant and microwave transmission. Inductive charging is mostly used for vehicle charging due to its benefits. It's a loosely coupled structure similar to a separable transformer, which transfers the energy from the grid to the onboard chargers in close proximity, shown in Figure 2.1. There is no direct contact between the vehicle and the grid. The air gap isolates the grid side WPT transmitting pad and the vehicle side receiving coil.

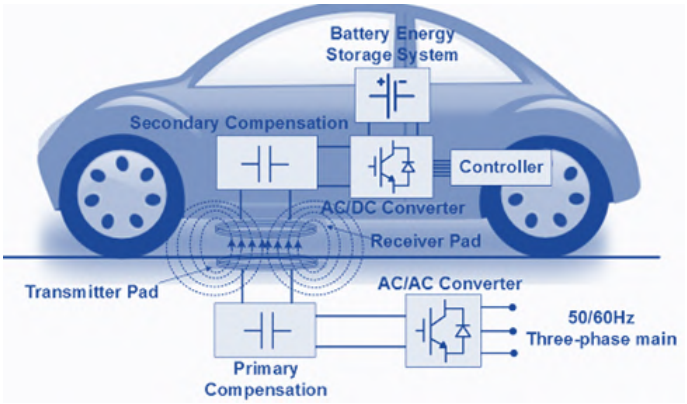


Figure 2.1: Inductive Wireless Power Transfer (WPT) Methodology [1]

The WPT transmitting pad is isolated and separated through the air gap on the grid side. Due to the absence of any contact and connectors, inductive wireless charging is very safe, convenient, and user-friendly. The resonant power transfer technique can be applied using near-field magnetic resonance coupling. Microwave a radiant energy transfer, with a lower efficiency with far-field and possess the risk of harming human health; therefore, it's not a strong candidate for commercial EV wireless charging technology. All the major automotive players, such as Tesla, Toyota, Ford, ZTE Corporation, etc., have already demonstrated their WPT technology and are racing to develop and commission the wireless charging infrastructure for their EVs[23]. The global EV wireless charging market is predicted to reach USD 221 million by 2028 [24].

The battery electric vehicle is architecture differs from the traditional combustion engine vehicles. Figure 2.2 shows the battery electric vehicle architecture where it can be seen that in the EV majority of the space is taken by the battery pack, and the remaining space needs to be distributed among motors, inverters, and onboard chargers. Thus EVs incur distinct packaging constraints to adjust electrified powertrain.

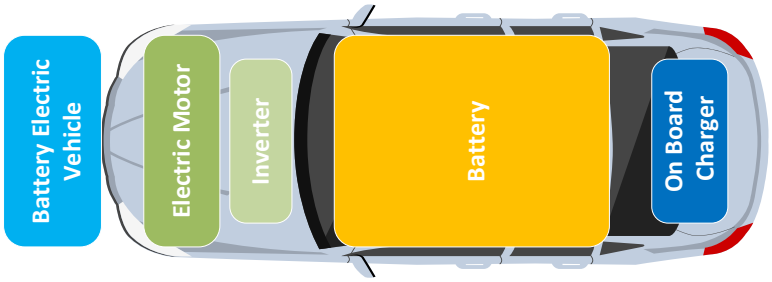


Figure 2.2: Battery Electric Vehicle Architecture.

Finding the optimal balancing point between the large battery size and the small vehicle size (to attain a longer driving range) is a design challenge. The design freedom aided by the lack of requirements for the driveline tunnel and combustion compartment, which was used to expand the cargo and passenger space, further shrinks the area available to the electronic traction drive system (ETDS) components in the chassis near the steering and suspension and away from the crash zones. An increased power density is the only solution to these constraints and to realize a skateboard chassis design with a widespread electrification platform. Figure 2.3 presents the distribution of ETDS components on the chassis [25]-[26]. The major automotive manufacturers, such as Ford, Lucid, Tesla, General Motors, Volkswagen, etc., have shown significant interest in using electric drive vehicles for mobility as a service application. The 2025 technical targets published by the US Department of Energy (DOE) aim to reach a power density of 33KW/L for a 100 KW traction drive system, which is an increase by a factor of 5.5 and an 88 percent volume reduction compared to the state of the art technology [27]-[28].

To the best of the author's knowledge, this is the first paper to combine the concept of planar and distributed magnetics considering the design space optimization constraints, therefore contributing to the increasing power density and magnetics design space optimization research.

While it is commonly known that higher switching frequencies lessen the need for energy storage on magnetic components [29]-[30], the ideal magnetic component's size is a more

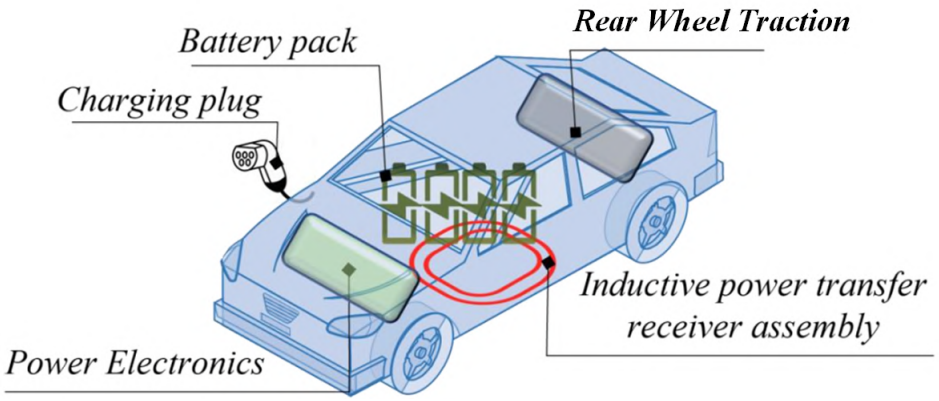


Figure 2.3: Battery Electric Vehicle Electronics Architecture.

complex issue[31]. A number of factors, including winding losses, permeability of magnetic materials, core losses, and temperature and heat transfer restrictions, must be taken into account in order to size magnetic components effectively [32]. Furthermore, the automation and repeatability of power electronic systems are hindered by the labor-intensive production complexity linked to conventional Litz wire and copper foil-based windings[33]. Features of low-profile planar magnetic components, like higher power density, superior thermal performance, unparalleled repeatability and modularity, ease of manufacturing, and predictable parasitics, have become increasingly popular with the rapid advancement of printed circuit board (PCB) technology [34].An inductor in series with the isolation transformer is necessary for many common high-power isolated DC–DC converter topologies. Integrating this series inductance as a programmable leakage of the isolation transformer further reduces the cost and boosts the power density of such converters [35]. Since the leakage flux is contained in the air, attempts to create additional leakage inductance by increasing the spacing between the primary and secondary windings in the core window are not very successful in producing a well-defined leakage inductance [36]. They also result in a reduction of core utilization. Alternative strategies for demonstrating the integration of a programmable inductor with the isolation transformer employing unique core structures can be found in the literature currently in publication [37]-[38]. A definite trade-off has been shown between component efficiency, power density, and manufacturing complexity in all of the integration strategies now in use. Perfect interleaving between a transformer's primary and secondary must be broken in order to enable the creation of programmable leakage inductance, which subsequently leads to higher AC winding losses [39]. A definite trade-off has been shown between component efficiency, power density, and manufacturing complexity in all of the integration strategies now in use. Perfect interleaving between a transformer's primary and secondary must be broken in order to enable the creation of programmable leakage inductance, which

subsequently leads to higher AC winding losses. For high-frequency planar magnetic designs with PCB-embedded windings, this technique is highly appealing because of the flexibility of routing in PCB-based winding implementation. There are two ways to design and regulate the leakage inductance in this technique, which leads to very different tradeoffs when looking at winding and core loss. For low power levels, especially in RF applications, the concept of integrated and distributed magnetics is common, but here the application is different and involves 2.5KV AC input at 100KHz on the primary side, which converts to 600V AC at 100 KHz on the secondary side. For the rectifier, the output should be around 400V and 18A to power the required load. This work increases the overall power density of WPT electronics on the vehicle side by reducing the height of the filtering network inductor, which is a bottleneck for enhancing the power density.

The key contributions of the paper are defined as follows.

1) It solves the problem of the large size of the filtering inductor associated with the rectifier stage by adopting a distributed and planar integrated magnetics approach, which is not common for such high power levels.

2) There is an upper limit up to which the size of the magnetics can be reduced by increasing the frequency due to the thermal management challenges. This research proposed a design space optimization framework for high-frequency distributed magnetics to find the optimal placement considering thermal and magnetic aspects.

3) Instead of using the traditional magnetic equivalent circuit (MEC), a high-fidelity magnetic equivalent circuit was used to model and manufacture the inductor. This approach reduces the uncertainties associated with the traditional model by accurately modeling the airgap fringing fluxes.

2.1.2 Vehicle Side WPT Electronics

The electronic structure for the WPT technology can be divided into two sides: The grid side and the vehicle side. On the grid side, the first stage is to convert the AC power into DC power using an AC-DC converter integrated with a power factor correction (PFC) circuit. The next step involves the conversion from DC power to a high-frequency AC to power up the coil on the transmission side through a compensation network. An isolation transformer is usually used between the converter and the coil for safety. An alternating magnetic field is generated in the transmitting coil due to the high-frequency current, which induces a voltage on the receiving coil. The compensation network on the secondary side improves efficiency. The last stage, also the one which this paper is focused on, is the rectification stage to charge the battery [40, 41]. This configuration is presented in figure 2.4.

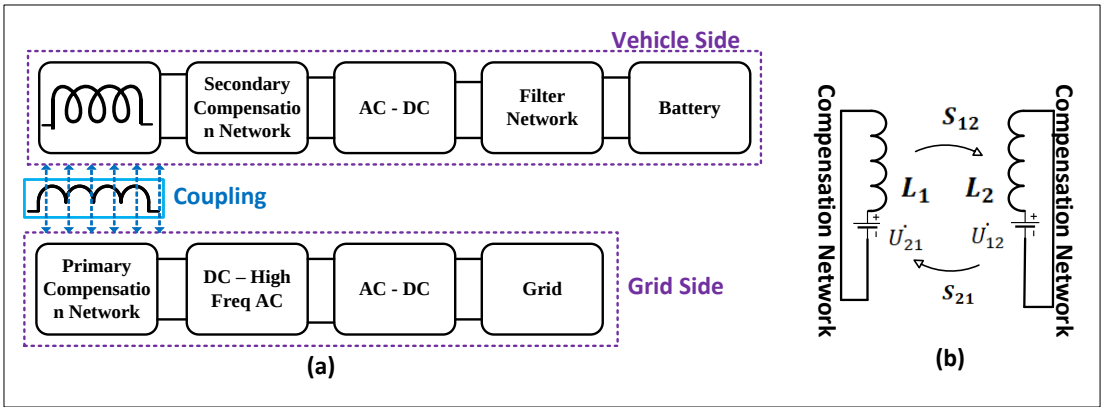


Figure 2.4: (a) WPT System Block Diagram (b) WPT Power Transfer.

Mathematically, the power transfer through the coil can be represented as [42, 43]

$$\begin{aligned} \dot{S}_{12} &= -\dot{U}_{12}\dot{I}^*{}_2 = -j\omega M\dot{I}_1\dot{I}^*{}_2 \\ &= \omega M I_1 I_2 \sin\varphi_{12} - \omega M I_1 I_2 \cos\varphi_{12} \end{aligned} \tag{2.1}$$

$$\begin{aligned} \dot{S}_{21} &= -\dot{U}_{21}\dot{I}^*{}_1 = -j\omega M\dot{I}_2\dot{I}^*{}_1 \\ &= \omega M I_1 I_2 \sin\varphi_{12} - j\omega M I_1 I_2 \cos\varphi_{12} \end{aligned} \tag{2.2}$$

I_1 and I_2 are the RMS current value and the $\varphi 12$ is the phase difference. $\dot{S}$ is the apparent power in phasor notation. Then the power transfer from the primary to the secondary side is modelled as

$$P_{12} = \omega M_1 I_2 \sin\varphi_{12} \tag{2.3}$$

To represent the total complex power transfer from one side of the coil to another we assume $\varphi_{12} = \pi/2$, and the active power can be transferred in both directions then the total complex power is given by

$$\begin{aligned} \dot{S}_{12} &= \dot{S}_1 + \dot{S}2 \\ &= j(\omega L_1\dot{I}_1 + \omega M\dot{I}_2)\dot{I}^*{}_1 + j(\omega L_2\dot{I}_2 + \omega M\dot{I}_1)\dot{I}^*{}_2 \\ &= j\omega(L_1{I_1}^2 + L_2{I_2}^2 + 2MI_1I_2\cos\varphi_{12}) \end{aligned} \tag{2.4}$$

Similarly, the reactive power can be expressed as,

$$Q = \omega(L_1 {I_1}^2 + L_2 {I_2}^2 + 2MI_1I_2 \cos\varphi_{12}) \tag{2.5}$$

After the primary side generates the high-frequency current into the sending coil through a converter, a rectification stage is implemented on the secondary side [44, 45, 46, 47]. The role of the rectifier design becomes very important when a secondary side control [48, 49] or a dual side control [50] architecture is adopted. After the rectifier, a boost converter is inserted for the control in the case of a parallel compensation also depicted in figure 2.5. However, in the series compensation scenario, a buck converter can be utilized. Moreover, the filtering and compensation network is also required. the bottom line is that no matter what control strategy we adopt the presence of the bulky inductor cannot be avoided, which is a design challenge that this research resolved.

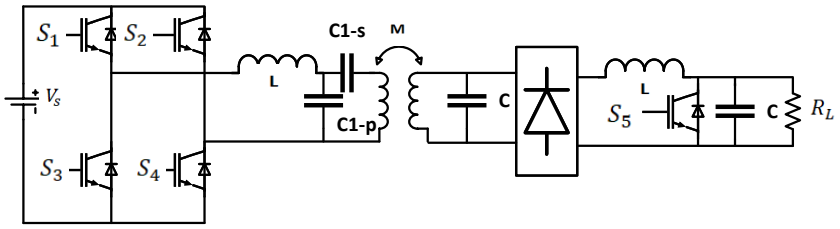


Figure 2.5: Circuit Schematics of WPT Configuration.

This research focuses on a super planar inductor design integrated with the rectification stage. The research was carried out with an automotive industrial partner where the actual space available on the chassis of the electric vehicle was measured and then the targets were set. The vertical space available on the chassis is very limited so the design needed to be spread horizontally. For this purpose, a novel approach was adopted. Instead of using and combining the market components, an EI-inductor was designed from scratch and fabricated and placed on the board in a series connection. Furthermore, an additional filtering and compensation network is required, regardless of the control strategy employed, the presence of a bulky inductor remains unavoidable; a design challenge that this research effectively addresses. Table 2.1 compares different EI-inductor approaches that can be opted for. However, remember the objective is to have an inductor with the least height to attain maximal power density and reliability.

Options	Plan Details	Core Winding	Cost	Height	Performance
Option 1	Self Design Best material	Customized Soft Core + PCB Windings	Highest	$1\sim 2cm$	1st
Option 2	Self Design Traditional Material	Available Ferrite Core + PCB Windings	3rd	$1\sim 2cm$	2nd
Option 3	Design by Manufacturer	Ferrite Core +Copper Windings	2nd	$3\sim 4cm$	3rd
Option 4	Available on Market	Common Core +Copper Windings	Cheapest	6 cm	4th

Table 2.1: Various Options for EI Core Design and Manufacturing

2.1.3 Multi-Planar Inductors Design

Using planar magnetic in power electronics applications ensures high power density, improved thermal performance, ease of manufacturability at large scale, and predictable parasitic parameters. Usually, the planar magnetic core uses a ferrite core with lamination layers. The traditional magnetic components with copper and litz wire windings have many limitations, such as bulky size, power loss, and complex fabrication methods [51]. The planar magnetics design with PCB windings is a good candidate to overcome these inherent issues. The planar magnetics also helps to achieve the best thermal performance as they enlarge the heat dissipation area. Due to the proximity of the primary and secondary windings, the overall power loss profile is improved due to the mitigation of loss phenomena such as eddy current, etc. Automatic production and high efficiency can be achieved simultaneously through planar magnetics; however, the issue of large volume and number still exist. To overcome this, an integrated approach is followed in this research where a planar EI-core inductor was designed and then placed in series with identical inductors to form an inductor board or module to achieve the required inductance and thermal performance and then integrated with the converter compactly. This distributed magnetics approach can effectively shrink many magnetic components, improving power density. Figure 6 shows the planar inductor design with the PCB-embedded windings.

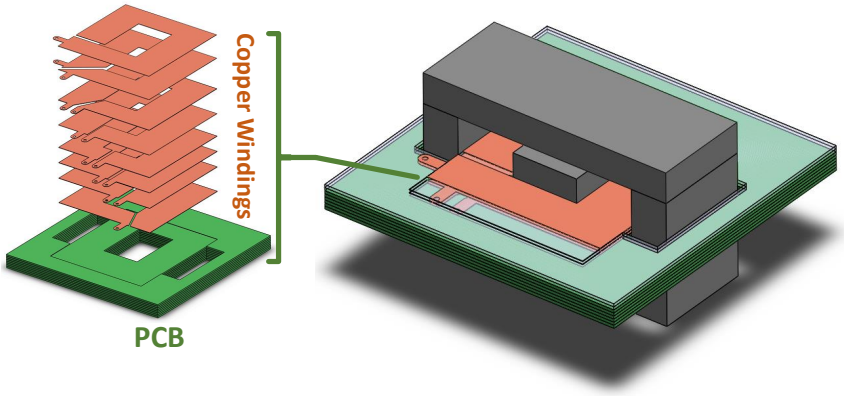


Figure 2.6: Planar inductor with embedded PCB windings.

2.1.3.1 EI-core Design Model

This research demonstrates an improved version of the distributed EI cores structure that contains a new air gap at the center leg of the E-core. It is to be noted that the value of the inductance will rely on the area of this air gap, which is helpful for multiple applications, as the desired inductance can be achieved by modifying the length of the air gap and the cross-sectional area. This research also optimises the planar inductors' distribution in the available design space. Figure 2.7 shows the EI core inductor structure. d_s is the slot depth, w_s is the

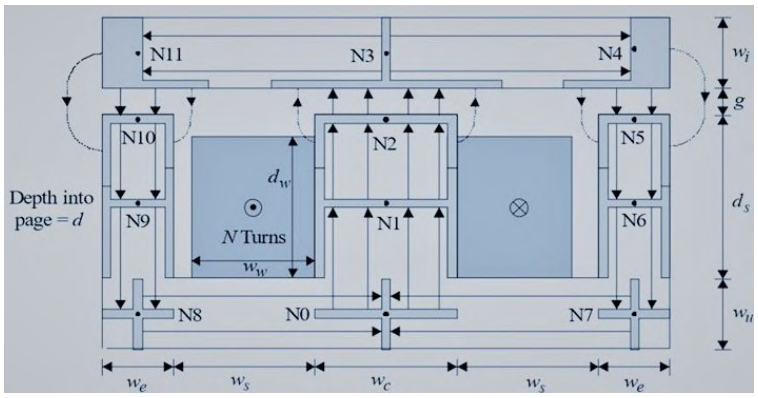


Figure 2.7: EI-core Structure labeled for modeling.

slot width, d_w is the winding depth, g is the airgap, N refers to the number of turns, w_t is the wire type, w_i is the I-core width, w_e is the E-core width, w_u is the E-core center width, w_u is the E-core underside width and d is the depth to which the inductor core extends into the page. Instead of using the normal and traditional modeling approach, here, a high-fidelity magnetic equivalent circuit (HEMEC) model is used. Compared to the traditional magnetic equivalent circuit (MEC) model approach, this model reduces the inaccuracies associated

with the traditional method[52]. The area of the column is the sum of the areas of two sides legs for an EI-type magnetic core, presented mathematically in equation 2.6.

$$w_c = \mathrm{w}_e + w_e = 2w_e \tag{2.6}$$

The HFMEC of the EI core is shown in Figure 2.8. The inductor geometry shown symbolizes

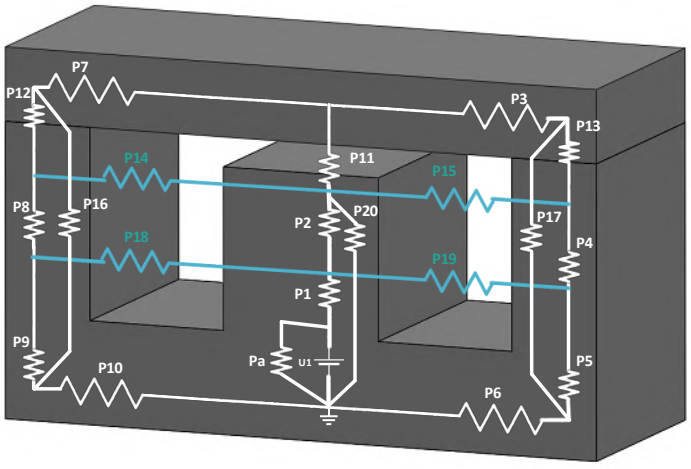


Figure 2.8: High Fidelity Magnetic Equivalent Circuit Model.

the flow of current into the page and the circular dot represents the current flow in and out of the page through the conductors with width w_w and height d_w. When inserted into a PCB the winding is wrapped around the centre post resulting in an magnetive motive force (MMF) source described by the equation. 2.7.

$$F = Ni \tag{2.7}$$

N is the number of turns and i is the flowing current. The permeance of the k_{th} branch of the HEMEC can be defined using the core material, core geometry, and winding current as,

$$P_k = \frac{(A_k)}{(L_k)}\mu \tag{2.8}$$

A_k is the magnetic flux cross-sectional area, L_k is the path length, and μ is the absolute permeability. The HEMEC model consist of straight core permeances($P_1 - P_{10}$), airgap permeances ($P_{11} - P_{13}$), and leakage permeances ($P_{14} - P_{20}$). The important difference between the traditional MEC and a HEMEC is the calculation of the air gap and leakage permeances. Table 2.2 shows the categorization of the permeances for better understanding.

Permeance Categorization	Straight Permeances	AirGap Permeances	Leakage Permeances
Permeance Element	$P_1 - P_{10}$	$P_{11} - P_{13}$,	$P_{14} - P_{20}$

Table 2.2: Permeances Categorization for HEMEC

2.1.4 Air Gap Permeances Calculation

The air-gap permeances were calculated using a standard method presented in [53]. Moreover, when the magnetic flux passes through the air gap between E and I cores, it causes a fringing effect [54]. The permeance equations can be stated as

$$P_{12} = P_{13} = P_{of} + P_{if} + P_{bf} + P_{ff} + P_{gf} \tag{2.9}$$

$$P_{11} = 2P_{if} + P_{bf} + P_{ff} + P_{gf} \tag{2.10}$$

and,

$$P_{if} = \frac{\mu_o d}{\pi} \ln|1 + \frac{\pi\omega_i}{g}| \tag{2.11}$$

$$P_{of} = \frac{2\mu_o d}{\pi} \ln|1 + \frac{\pi\omega_i}{4g}| \tag{2.12}$$

$$P_{bf} = P_{ff} = \frac{\mu_o\omega_e}{\pi} \ln|1 + \frac{\pi\omega_i}{g}| \tag{2.13}$$

$$P_{gf} = \frac{\mu_o\omega_e d}{g} \tag{2.14}$$

The leakage permeance elements $P_{14} - P_{20}$ correspond to the flux traveling outside the core's magnetic path. P_{14} and P_{15} corresponds to the horizontal flux, P_{16} and P_{17} corresponds to the verticle flux and the remaining components $P_{18} - P_{20}$ corresponds to vertical and horizontal fluxes. The leakage flux calculations can start from the field intensities calculation for the EI core utilizing Ampere's law. The horizontal leakage permeance corresponding to the elements $P_{18} - P_{19}$ in HFMEC model can be written as,

$$\begin{aligned} P_{18} = P_{19} &= P_{xs}|0 \leq y \leq d_w + 2P_{xf}|0 \leq y \leq d_w \\ &= \tfrac{\mu_o d_\omega d}{3\omega_s} + \tfrac{2\mu_o d_\omega}{3\pi} \ln|1 + \tfrac{\pi w_c}{2w_s}| \end{aligned} \tag{2.15}$$

$$P_{14} = P_{15} = P_{xs}|d_w \leq y \leq d_s w + 2P_{xf}|d_w \leq y \leq d_s \\ = \frac{\mu_o d}{\omega_s}(d_s - d_w) + \frac{2\mu_o(d_s - d_w)}{\pi} \ln|1 + \frac{\pi w_c}{2w_s}| \tag{2.16}$$

The vertical leakage permeances P_{16} and P_{17} are as follows

$$P_{16} = P_{17} = \frac{\mu_o d(\omega_s - \omega_w)}{d_s + g} \tag{2.17}$$

$$R = \frac{\omega_t + \omega_b}{\mu_o \omega_t \omega_b \omega_c}[\omega_w + \sqrt{\frac{(2d + \omega_t + \omega_b)\omega_t \omega_b}{\omega_t + \omega_b}}] \tag{2.18}$$

$$P_{20} = 2(P + R^{-}1) \tag{2.19}$$

2.1.5 Inductor Simulation and Manufacturing

Considering the application requirements, available space at the chassis of the vehicle, and the mathematics explained in the previous section, the inductor was simulated in ANSYS/Maxwell workbench. Apart from the super planar design and geometry, the contribution points of this inductor design include

1. Using individual design for each inductor to adjust the heat loss to realize the balance heat distribution, as the different inductor's locations can cause an imbalance in heat distribution.

2. Avoiding the interface between two different inductors, as two closed inductors can cause mutual inductance which will result in the reduction of the inductance value.

3. Careful performance evaluation of the Nano-materials. Table 2.3 shows the comparison of the nanocrystalline material which was evaluated.

Computing the power losses before finalizing the inductor design parameters is important. Here the focus is on calculating the copper loss and core loss. Winding resistance helps in the calculation of copper power loss.

$$R_w = \frac{\rho l_{wR}}{A} \tag{2.20}$$

Mate	Plan	Core	Cost	Height	Pere	Perf	Pence
Saturation Flux Density Bs (T)	2.03	0.5	1.55	0.74	0.58	1.56	1.25
Coercivity Hc (A/m)	40	8	12	2.4	0.4	2.4	1.2
Initial Permeability (μ_i)	1500	3000	6000	40000	100000	5000	80000
Max Permeability (μ_m)	20000	6000	60000	200000	1000000	50000	400000
Electrical Resistivity ($\mu\Omega_{cm}$)	50	$5x10^7$	30	60	140	130	115
Curie Temperature (C)	750	220	550	450	250	399	570

Table 2.3: Nanocrystalline Material Comparison

ρ is the resistivity of the material for conductor, l_{wR} is wire length and A is the cross-sectional area.As for this rectifier application, the rated current is $18A$, so the power loss comes out to be $2.5W$. For the core loss calculation according to this application and the working conditions i.e. at $13KHz$ and $77g$ for each inductor, Equation 2.21 can be used to calculate the core loss which turns out to be $4.5W$.

$$P_{core} = K_1 {}_f^x B^y V_e \tag{2.21}$$

whereas, $K1$ =core material constant, f = frequency(kHz), $B = Peak\ Flux\ density$, x = frequency exponent, y = flux density exponent, and V_e = Effective core volume. The overall dimensions of our designed inductor are $40 \times 20 \times 15$ (mm).

The inductor was simulated with different airgaps to check the airgap sensitivity. Due to the higher magnetic conductivity, it was established that the design air gap length should be strictly limited to under 0.05mm. Figure 2.9 shows the inductor behaviour for $0.05mm$ airgap. In Figure 2.9(a) the power loss of the whole planar inductor geometry is simulated. The flux linkage, associated induced voltage and the resultant core loss are presented in figure 2.9(b).

Another important aspect of the magnetics design is the magnetic field strength and energy estimation depicted in Figure2.10(a) and Figure 2.10(b), respectively on a logarithmic scale for better understanding. Planar winding design plays an important role in the overall

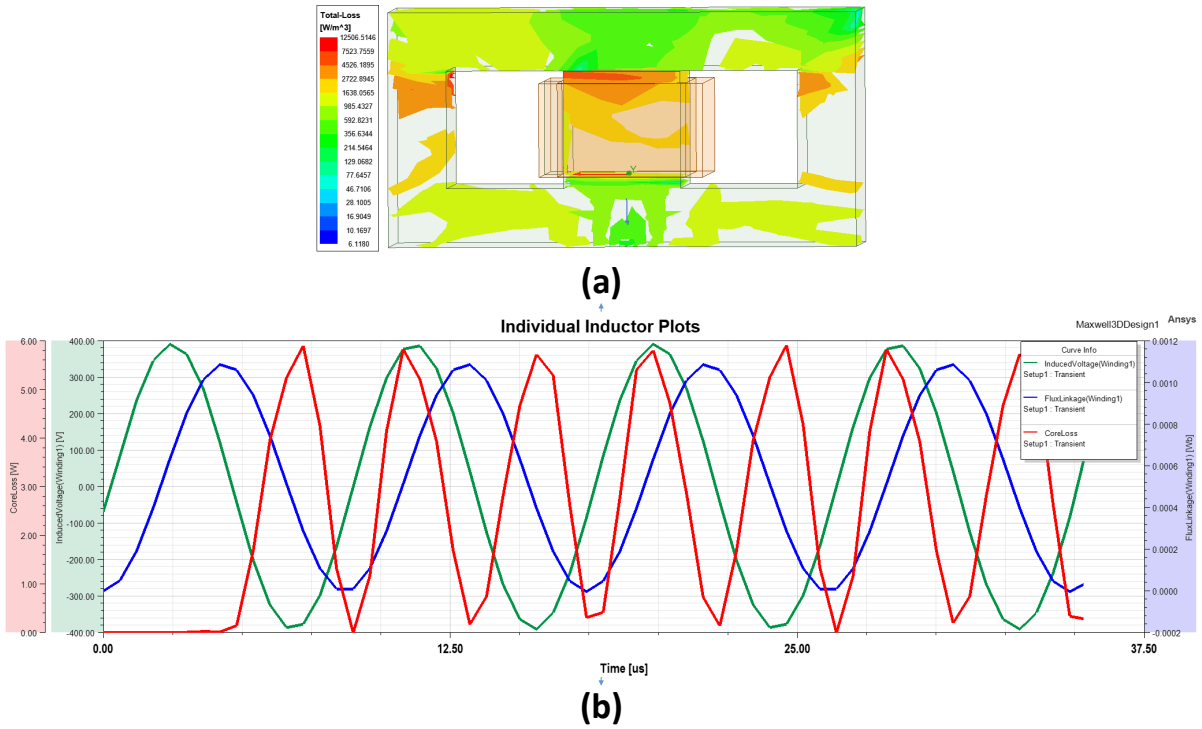


Figure 2.9: (a) Power Loss Analysis (b) Core loss, induced voltage and flux linkage waveform.

performance of the designed planar magnetic component. The copper thickness, insulation thickness, structural geometry, etc., are all important factors involved in the winding design. The current density analysis was performed to determine the designed winding's performance for this research. Figure 2.11(a) shows the magnetic field distribution, and Figure 2.11(b) shows the current density of the PCB windings. The current density distribution is not as uniform as expected due to the proximity and skin effects. The total loss that occurs across the inductor is the combination of the core loss, windings loss, and the loss due to these effects.

Figure 2.12 shows the manufactured inductor and the designed PCB Winding. An eight-layer FR4 PCB was used for the windings design of the proposed inductor, as a result, the fabricated PCB that contains the inductor windings is very thin, which offers improved window area leading to better thermal and magnetic performance.

2.1.6 Experimental Results

The simulation results of the modeled and manufactured inductors are shown in the previous section. Instead of using a single inductor for the experimental verification, based on

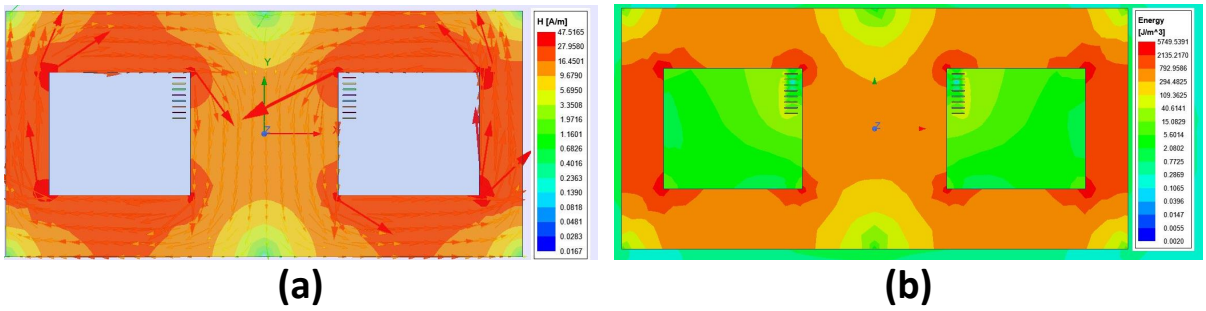


Figure 2.10: (a) Magnetic Field Strength (b) Energy

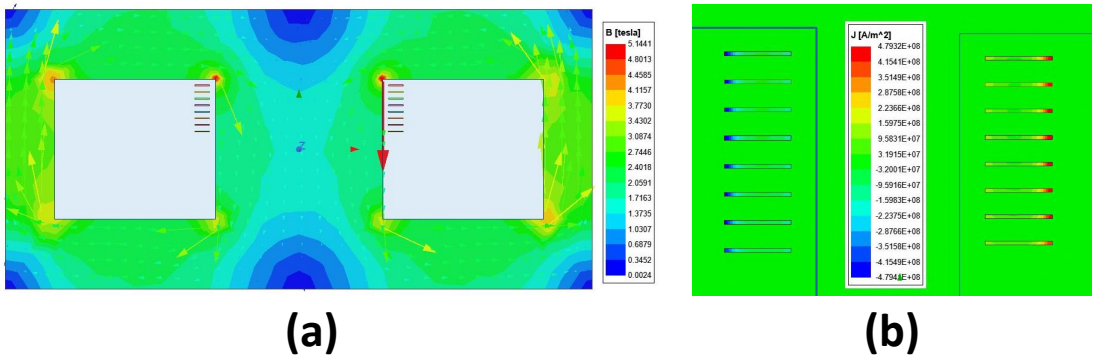


Figure 2.11: (a) Magnetic Field Distribution (b) Current Density Distribution of PCB Windings Cross section

the required power level of the application here, an inductor module board was developed containing sixteen planar distributed inductors shown in Figure 2.13. It can be seen that the inductor modules board, which acts as a high power density single inductor, is attached to the rectifier circuit; the circuit is blurred or animated due to the intellectual property of the industrial research partner involved in this research.

For a better understanding of the considered rectification stage, Figure 2.14 presents the simplest representation of the schematics. This work is focused on the highlighted load side inductance. The schematic design represents the stage in the wireless power transfer system on which this research is focused i.e. the rectification and filtering stage on the vehicle side. It means the input AC signal comes from the secondary compensation network integrated with the wireless transfer coil. High-frequency AC power is wirelessly sent to the secondary coil via the mutual inductance between the primary and secondary coils. To enhance the transfer efficiency, the secondary compensation network and secondary coil must be set to have the same resonance frequency. After passing through the rectifier stage and the filter network, the high-frequency AC power is converted to DC power. At last, the battery pack

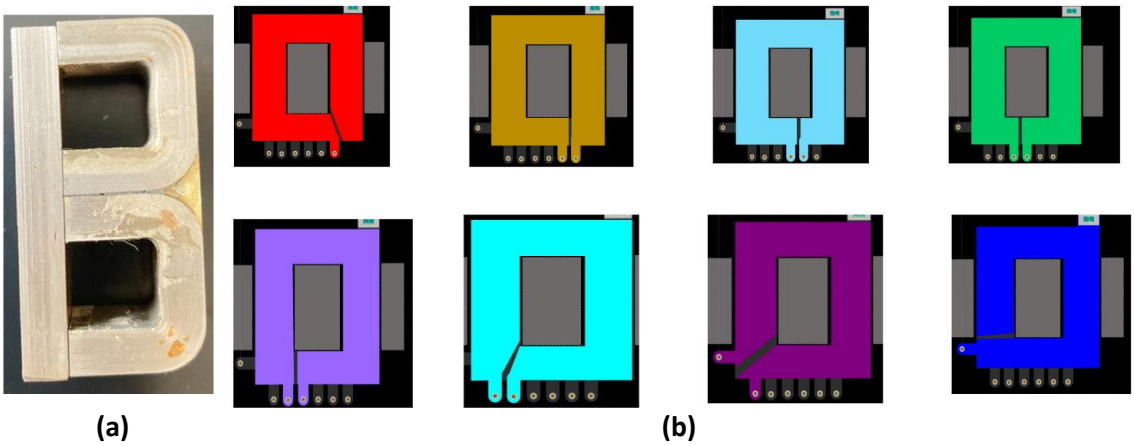


Figure 2.12: (a) Manufactured Inductor (b) Designed PCB Windings

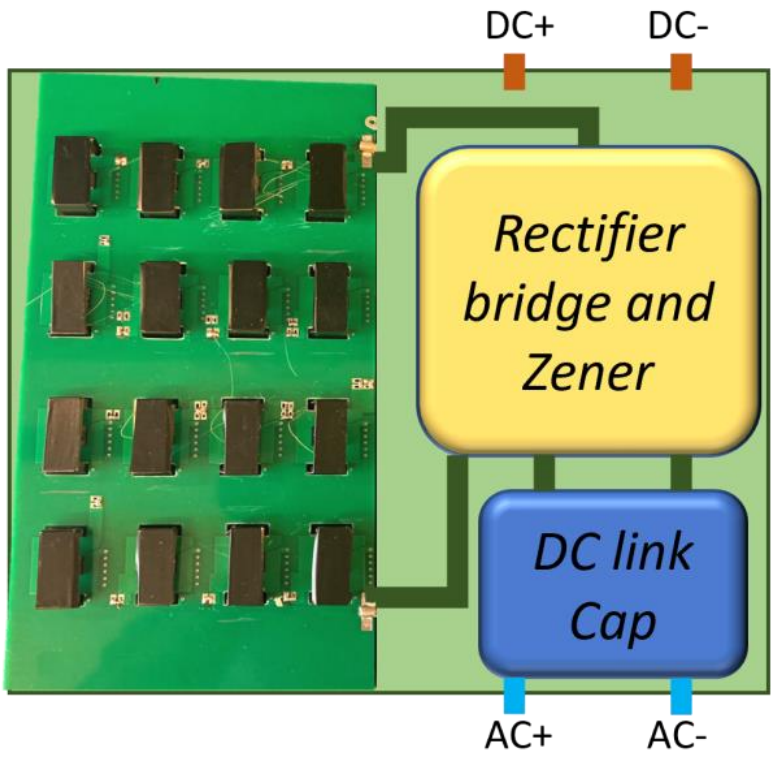


Figure 2.13: Metal core and FR4 Board Combination to form a rectifier stage integrated with distributed planar inductor module.

can be charged using DC power.

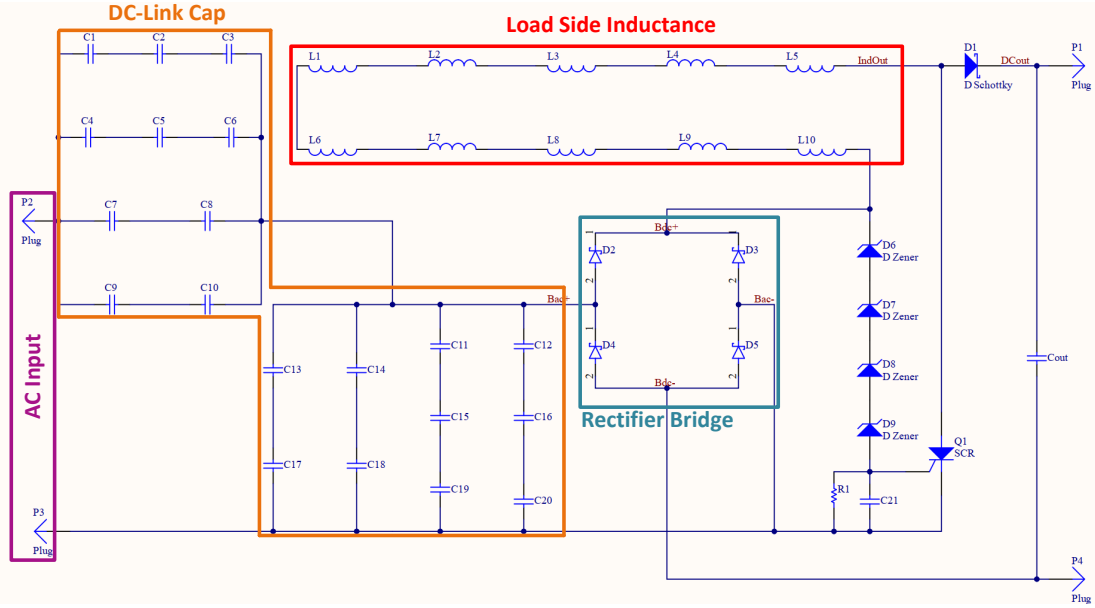


Figure 2.14: Schematics Design of the Rectification and filtering Stage

Distributed magnetics are complex to handle as many design variables are involved, such as the gap between individual magnetic components, mutual inductance, arrangement geometry, and thermal aspects. The goal is to optimize the available design space for better thermal and electromagnetic performance. Different techniques can be adopted for allocating and optimizing the design space, ranging from simple mathematical distribution to complex algorithms. This research area of design space optimization for magnetics is still evolving. Here an algorithmic approach was adopted, and multiple valid solutions can be achieved based on the targets. It's upto the design engineer to select the solution that results in better overall performance, including reliability, power density, easy integration, and cost.

Figure 2.15 presents the obtained design optimization scenario where a relation between the design space setpoints and standard deviation (SD) was established that resulted in various solutions. The design space optimization aims to identify the optimal solution among the possible solutions. Various constraints, such as the minimum and maximum distance between two individual inductors, the total area of the inductor module board, overall temperature, mutual inductance and self-inductance etc., are the constraints that control the possible solutions. Choosing the best solution manually is difficult and prone to errors; however, establishing a relationship that contains the input from all the parameters involved makes the decision-making fast, accurate and easy. This article focuses more on magnetic modeling and design, so discussing the adopted algorithm is beyond the scope and focus.

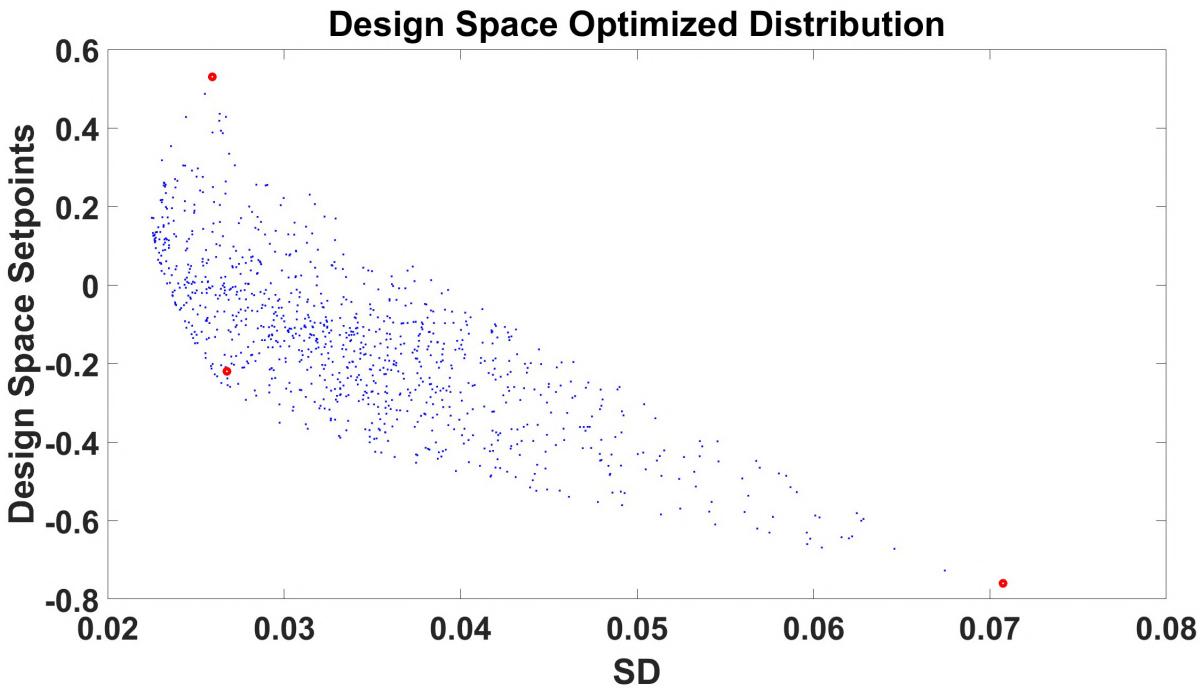


Figure 2.15: Design Space Optimized Distribution

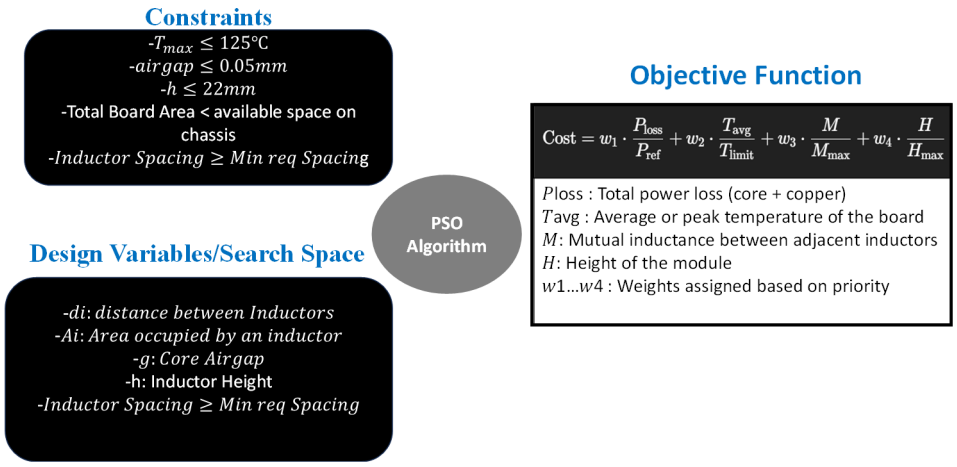


Figure 2.16: Design Space Optimized Parameters

A point corresponding to the positive value on the y-axis and with the lowest standard deviation can be considered a good solution.

Mutual inductance among such distributed magnetic components is crucial to consider, and it can significantly affect the performance. In an available design space, multiple orientations can result in various values for mutual inductance. Thus, quantifying the mutual inductance is a complex but necessary step for efficient design decision-making. However, as

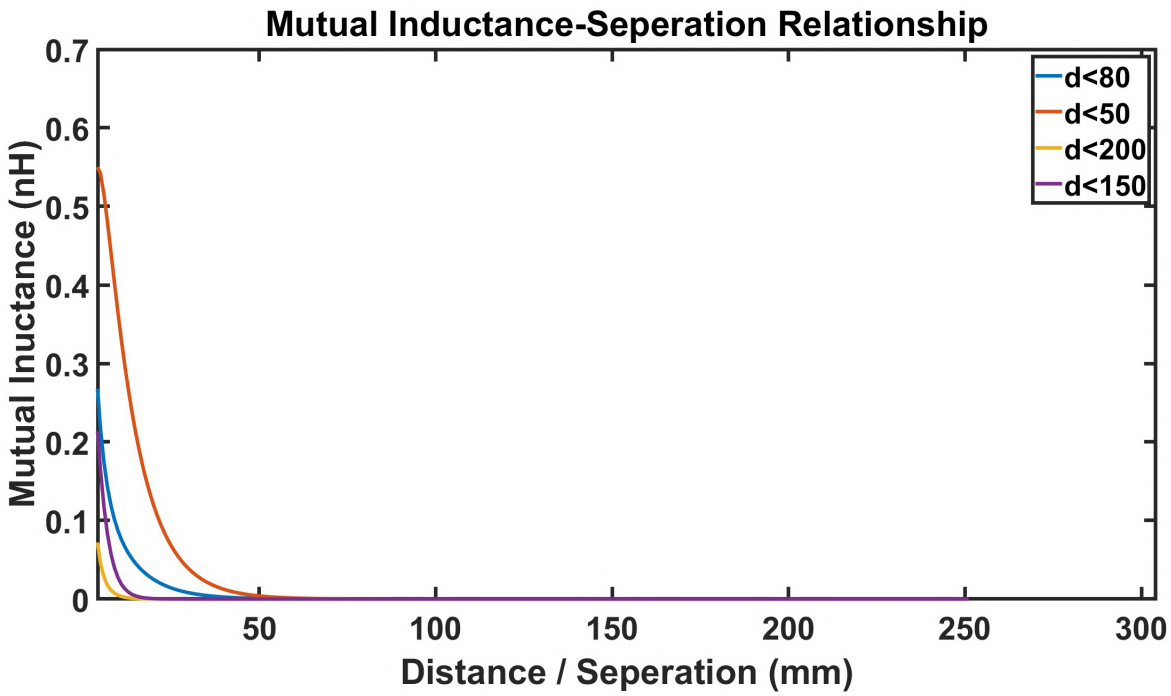


Figure 2.17: Mutual Inductance and Mutual Separation Distance

this kind of distributed magnetics approach is not common and is still an evolving research field, a relation between the separation between the planar inductors and the mutual inductance was derived for the design of the planar distributed inductor module, as shown in Figure 16 ensure an optimized distribution in the available design space. It can be observed that the mutual inductance varies with the change in the distance. However, the variation is not linear or too simple to be extrapolated. Hence, a relationship between the separation distance and mutual inductance was essential and very helpful.

According to the application, an inductor module board was developed for experimental validation and verification to attain the inductance value. The operating environment in the vehicle chassis is harsh and leads to high temperatures. Moreover, the rectifier board generates its own heat due to the associated power dissipation. An in-depth comparison of different PCB material's performance was carried out. Finally, the metal core PCB was the best in terms of structural reliability, cost and thermal performance. After different test combinations, it was established that a dual approach that uses the metal core PCB for the rectifier board and FR4 PCB for the inductor board module is the optimal choice considering weight, cost, reliability, and thermal performance. The thermal performance curves obtained after the test to compare the performance of the metal core and FR4 PCB are presented in Figure 2.18. It can be observed that the metal core PCB (red curve) provides better thermal performance compared to the conventional FR4 PCB (blue curve), which supports

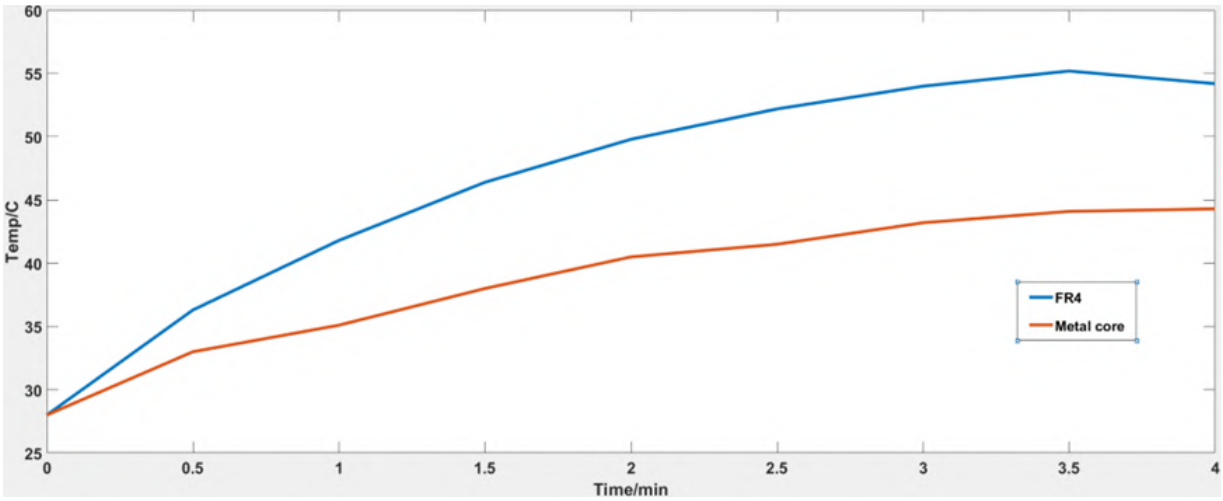


Figure 2.18: Metal Core vs FR4 board thermal performance Comparison.

the proposed design methodology of using a hybrid combination which yields better overall thermal performance.

To analyze the working of the designed planar and distributed inductor module, a frequency sweep analysis was performed with respect to the solid loss. The current can vary in different conditions for this wireless power transfer-based inductive charging application as the current flowing through the inductor can vary based on the region and type of charging. Analysis was done to test the magnetic performance under different current conditions, resulting in the fact that the solid loss increases with the increase in the frequency. The current, as well as the frequency, was varied for a wide range to observe the loss characteristics. Usually, the magnetics are tested and analyzed for a specific frequency and current, making the analysis less beneficial for researchers. Here, a very broad and detailed analysis was done with the aim of extending this result to other magnetic geometries and applications. Using this analysis, the design engineer can conclude the limitations of the designed electronics and take the required thermal dissipation measures.

Figure 2.19 presents the analysis performed under changing current scenarios. The experimental setup was tested on different frequencies, and the corresponding core loss was measured to note the behavior of the magnetic core. The resultant relationship between the core and frequency shown in Figure **??** is very similar to the results obtained through the FEA analysis, which shows the accuracy of the design. Core loss is an important factor to measure and verify when the design involves magnetics, as it leads to the critical decisions of designing the thermal dissipation strategy and estimating the system efficiency.

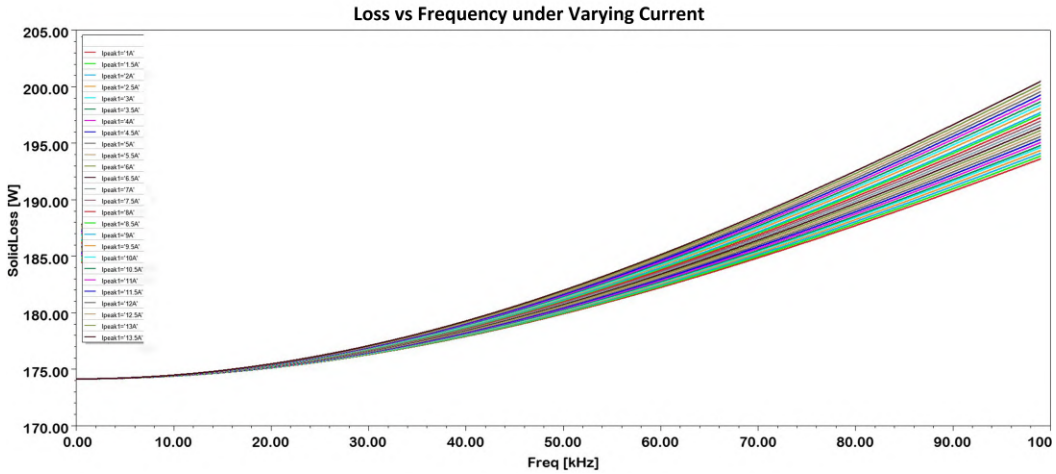


Figure 2.19: Dynamic performance under varying current and frequency.

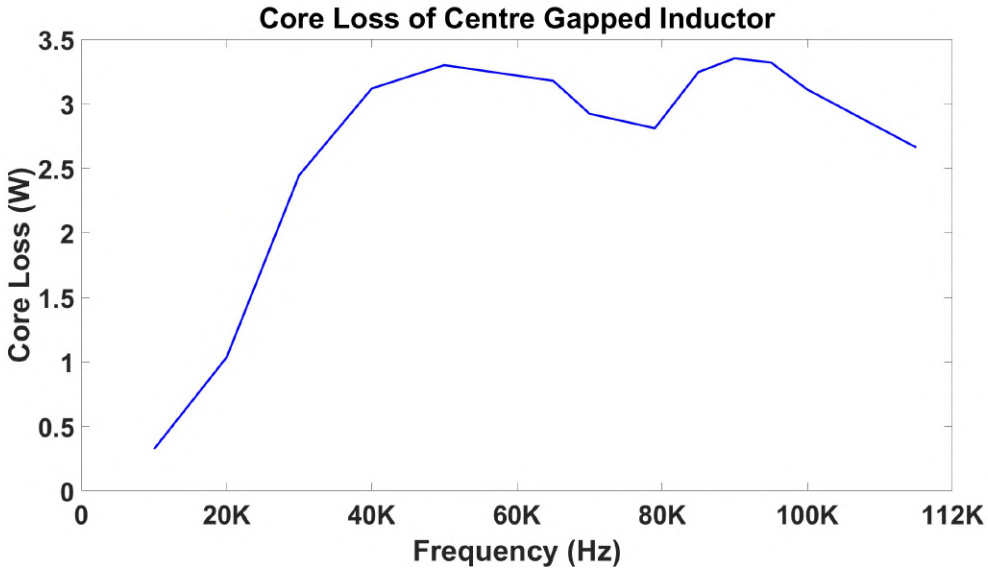


Figure 2.20: Core loss and frequency relationship

The experimental test bench is presented in Figure 20 where it can be seen that the setup consists of the AC input source, the rectifier stage integrated inductor module board connected to the load. A current probe is utilized for the output current measurement. The temperature is measured continuously through a thermal camera device to ensure and analyze the required thermal performance. Figure 21 shows the waveforms from the experimental setup. The output voltage is 91.2V with 9.8A of current. The input voltage is set at 102.8V; the difference between the input and output voltage presents the associated power loss at this rectification stage. The experimental setup consists of an AC input source emulating the stage after the secondary side compensation network in the WPT vehicle side electronics. The inductor module board integrated with the rectifier and connected to the resistive load is tested for functionality. The rectifier stage result shows that integrating the inductor module and rectifier stage board works well, achieving the required rectification.

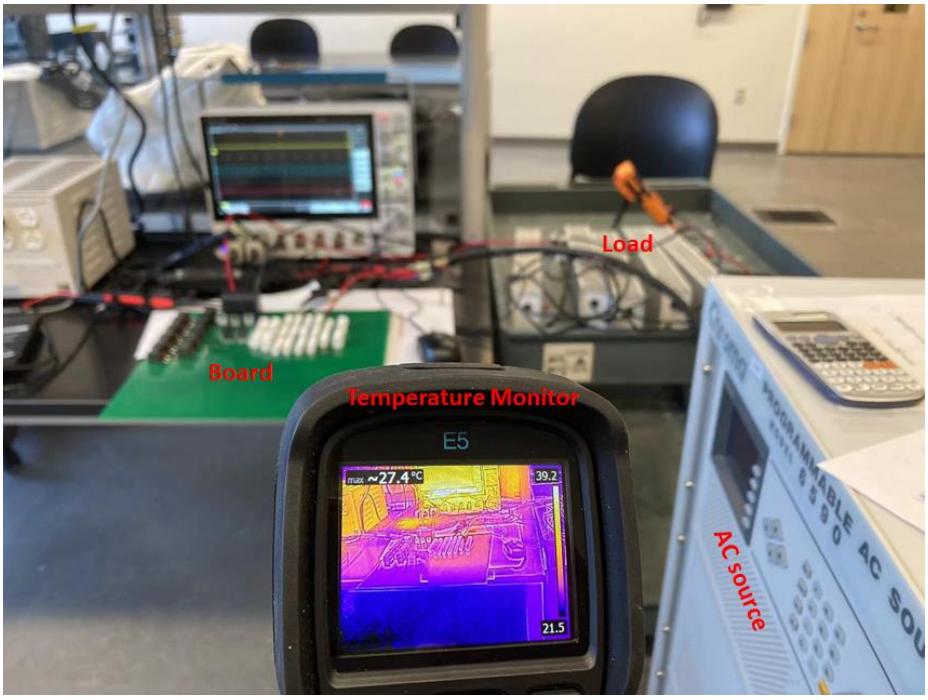


Figure 2.21: Test Bench for testing the integrated and distributed planar inductor-rectifier.

Another major goal of this research was to increase the power density, so the designed planar inductor's module height (22mm) was compared with a conventional package(65mm), capable of operating in the same operating conditions and offering similar inductance value and a decrease of 66% in package height was observed as depicted in Figure 2.23, which solved the problem of the limited verticle space in the chassis of the EV. The distribution of low-profile passive components with better heat dissipation from metal core PCB mainly

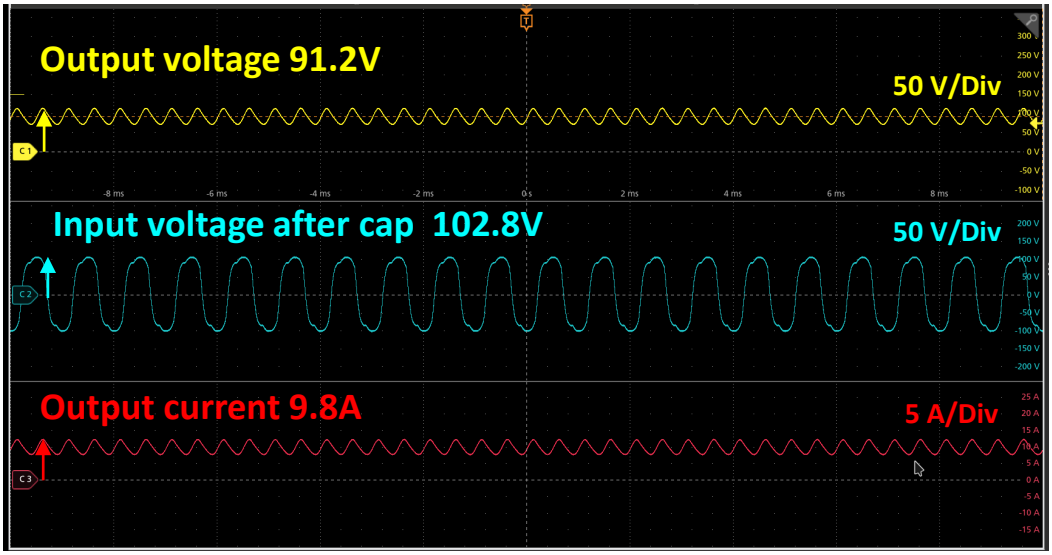


Figure 2.22: Rectifier Stage with integrated inductor module experimental results.

contributes to the power density increase. The comparison is based on the whole inductor module board integrated with the rectifier stage and contains sixteen individual inductors arranged based on the presented design space optimization approach and connected electrically forming a distributed planar magnetics concept.

The experimentally measured efficiency plot of the system is given below in Figure 2.24. As this work is focused on improving the power density and no new circuit topology is proposed, so compared to the traditional efficiencies presented in the literature for this stage in the WPT system, the measured efficiency here is similar [55]. From the graph, it is evident that the efficiency increases when the testing power level is increased.

In Conclusion, this research solved the problem of limited vertical space on the electric vehicle chassis for WPT power electronics by modeling and designing super planar-distributed magnetics with integrated PCB windings considering the design space optimization constraints. A novel and more accurate high-fidelity model was derived instead of using the available and traditional magnetic equivalent circuit (MEC) models that helped to model the magnetic component behavior accurately. Overall, this research treated and solved the power density problem as an optimization problem considering every constraint involved, resulting in a significant 66% increase in power density. Moreover, the combination of a metal core and FR4 PCB was used based on the test data for optimal thermal performance. This research paves the way for developing a high-power density WPT power electronics unit. It is also a step forward in distributed magnetics and automated magnetics design, an evolving

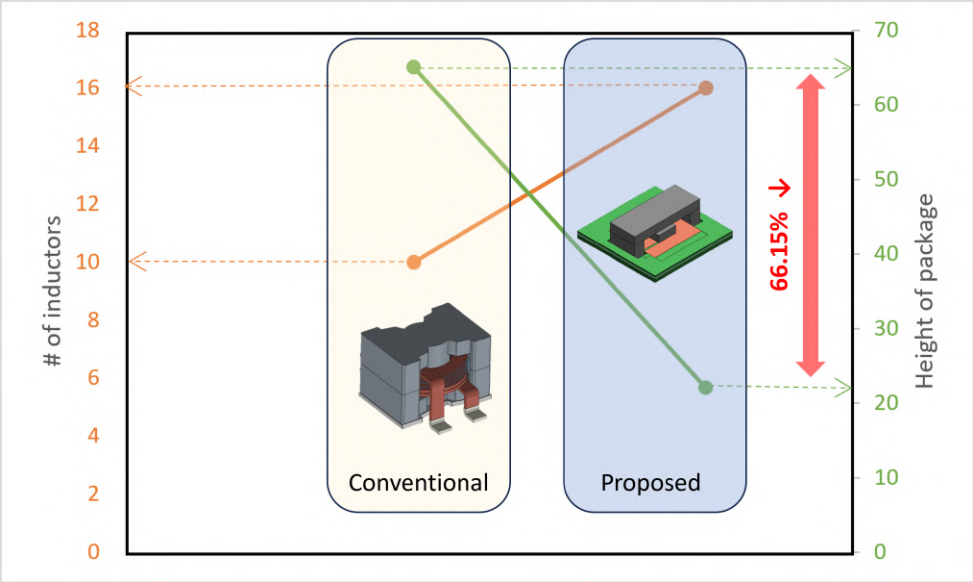


Figure 2.23: Compariosn of designed inductor package height vs conventional one

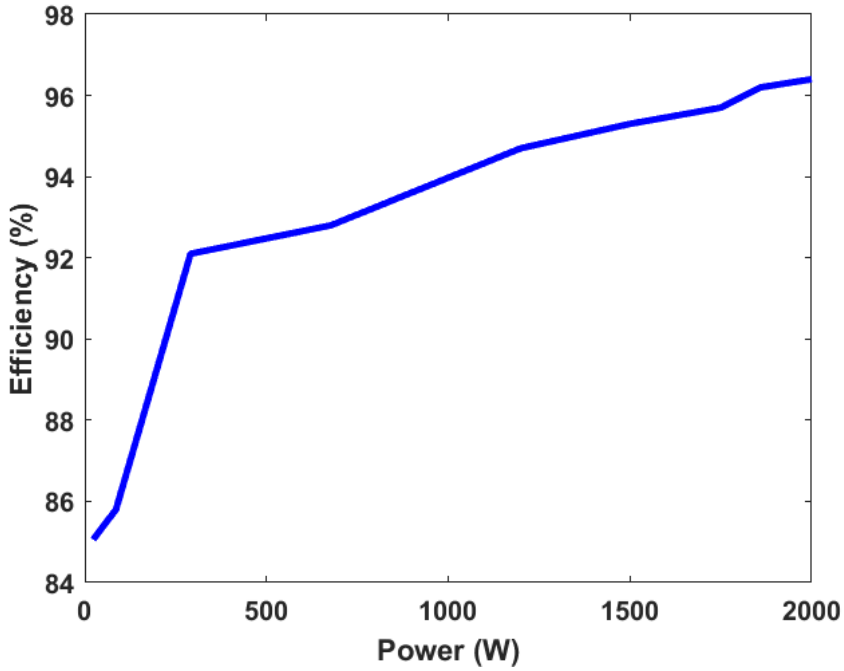


Figure 2.24: Experimentally measured efficiency of the proposed and designed system at various power levels

research area for which the concept of explained design space optimization is essential.

2.2 Novel Coupled Three-Phase Inductor Structure for Interleaved Converter in Electric Vehicles Applications

2.2.1 Introduction

Power density and efficiency are the key design criteria for the modern power electronics unit in Electric Vehicles (EVs), where the vertical space on the chassis is very limited, which calls for innovative packaged vehicle electronics and components. This has increased the importance of interleaved DC-DC converters with integrated magnetic components aiming for increased power density and system efficiency. However, the bulky inductor geometries serve as the bottleneck for increasing the power density. This research presents a novel three-phase star-shaped inductor geometry that retains the advantages of coupled inductors while ensuring high power density as it can be packaged or placed in the vehicle with minimum verti- cal space available and tackling the problems of high airgap fringing flux losses, uneven flux distribution, and three-phase current un-balancing associated with the conventional bulky inductors. Moreover, a new high-fidelity magnetic equivalent circuit (HFMEC) model was derived and applied for the design of this geometry, which reduces the inaccuracies associated with the traditional magnetic equivalent circuit (MEC) modeling. The model proved to be capable of evaluating the flux and current characteristics much quicker and with less computational cost as compared to the finite element analysis approach, especially when complex geometries are involved. The proposed inductor geometry is modeled based on HFMEC, designed in Solidworks, simulated in ANSYS (MAXWELL 3D), fabricated, and then implemented with a three-phase interleaved converter to evaluate the performance.

The demand for high power density and highly efficient boost converters has increased significantly with the global expansion of eco-friendly automobiles such as fully electric vehicles or hybrid electric vehicles [56] -[57]. To power the propulsion system in these applications, the boost converter is typically positioned between the battery and the inverter. The electric vehicle (EV) architecture differs from the traditional internal combustion engine (ICE) vehicles. In EV, the majority of the space is covered by the battery pack, and the remaining space needs to be distributed among the inverters, auxiliary converters, motors, and onboard chargers. Hence, EVs incur design and packaging constraints to accommodate the electrified power train. Finding the optimal point between the large battery pack and the small vehicle

size for an enhanced driving range is a design challenge. The area available to the electronic traction drive system (ETDS) is further limited by the lack of requirements for the driveline tunnel and combustion compartment that was used to expand the cargo and passenger space. In particular, the vertical space on the EV chassis for the power electronics unit is very limited. Thus, an increased power density is the only way forward [58]-[59]. Achieving a high power density is particularly significant since it affects both the living space for users and the performance of the vehicles. Moreover, the US Department of Energy (DOE) established 2025 technical targets that seek to achieve a power density of 33 KW/L for a 100 KW traction drive system, an increase by a factor of 5.5 and a volume reduction of 88 percent over current technology [60]. Considering these requirements and constraints, the interleaved boost converter topology is widely implemented in such vehicular applications [61].

The Wide Bandgap (WBG) semiconductor materials like Silicon Carbide (SiC) and Gallium Nitride (GaN) have drawn a lot of attention in the last decade because of their promising electrical and thermal properties. WBG switching devices, which outperform Silicon devices in terms of conduction and switching, have since been introduced to the market. More effective converters with higher power densities are now achievable thanks to these new technologies [62]-[63]. So, a lot has been done on the power electronics switches side, but the reduced footprint magnetic designs are still a bottleneck in achieving the highest power density. Inductors are the most challenging component type to integrate on a semiconductor chip or in a planar package out of the three basic component types used in power converters switches, capacitors, and inductors. This task is made more difficult by the fact that there has been relatively little research work because most types of electronics don't require inductors, which is partially the result of difficulties with process compatibility with magnetic materials [64]. But the performance scaling of magnetics with size presents a more basic problem. Although hundreds of tiny cells connected in parallel can be used to create capacitors and semiconductor devices, the performance of magnetic components would be drastically reduced [65]-[66].

Electric vehicles frequently use interleaved architecture because of its benefits of minimal input current ripple, power density, and high efficiency. PFC converters [67, 68, 69], solar applications [70], and automotive applications [71, 72, 73, 74] have all used interleaved technology. Magnetically coupled inductors can be utilized to minimize the input current ripple. The inductance volume can be decreased in the meantime by the magnetic coupled inductor. The requirement for the capacitor value may be reduced due to the lower ripple current. Compared to the double dual boost [75]-[76] or switched capacitor converter [77]-[78], the interleaved boost converter uses fewer capacitor and inductor components. In order to lower

the phase current stress, the connected inductor could also share the current stress in each phase. Interleaved boost converters can reduce input current ripple and simplify hardware design when compared to cascade and quadratic converters [79]-[80].In most cases, connected three-phase inductors' characteristics are not identical due to associated drawbacks and fabrication faults of traditional inductors, which results in an unbalanced phase current. The MOSFET drive signal values for the various phases may also change from time to time, which results in an imbalanced phase current. One phase will experience increased current stress due to the imbalanced current, which will eventually result in a shorter MOSFET lifetime of that particular phase leg. Additionally, a larger single-phase inductance current might result in a saturated one-phase inductor, which will eventually destroy components.

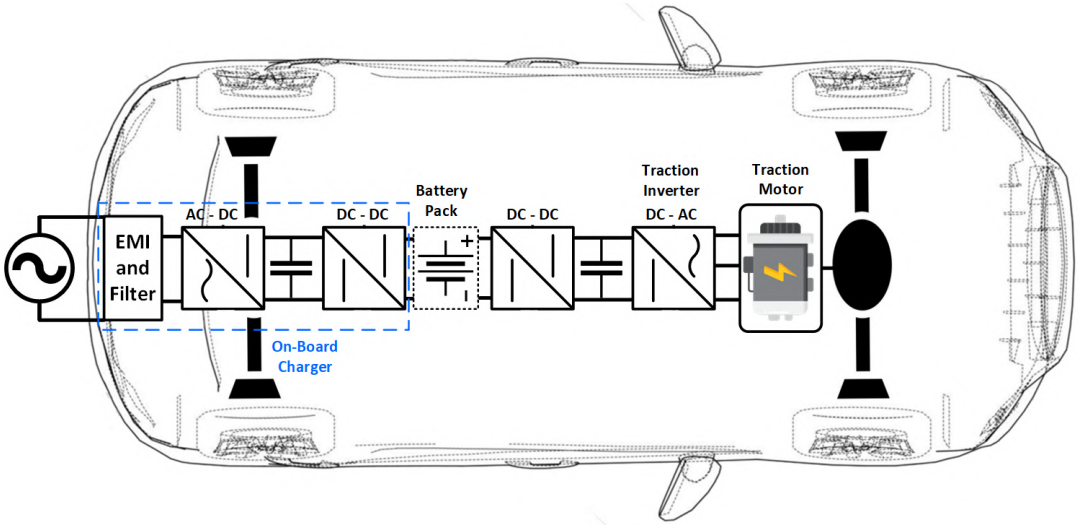


Figure 2.25: Electric vehicle (EV) Architecture

A typical EV drivetrain architecture and battery charger setup are shown in Fig. 2.25. These batteries can be charged using either the energy sources built inside the EV vehicle or the specialized charging stations. Battery chargers that are independent (off-board) or mounted can have power flow topologies that are either unidirectional or bidirectional. Since most battery electric vehicles (BEVs) use battery systems with an expected voltage range of 150–450 Vdc, a step-up DC/DC converter is required to enhance the dc-bus voltage level to 400–800 Vdc [81]-[82].To improve the system's overall efficiency and dependability, a DC/DC converter should draw a consistent, low ripple current and maximize battery power. A method that holds promise for stepping up or stepping down the voltage level of DC/DC converters is magnetic coupling or coupled inductors. Coupled inductors have been designed to be used in the interleaved DC/DC converter, and the design principles have been adequately examined in the manner described in [83]. In [84]-[85], for automotive

applications, a bi-directional multi-device interleaved DC-DC converter is described. In [86], another coupled inductor-based interleaved topology has been presented, which shows good efficiency and power density. Instead of using numerous discrete inductors, coupled inductors offer a straightforward and more adaptable way to step-up or step down the voltage, as well as help current sharing among semiconductors. This is potentially advantageous and is receiving more attention for improving the performance of dc/dc converters [87, 88, 89]. Even so, since most of the research work that has been done so far has only focused on single or dual phases, there are still unanswered questions regarding how to reduce the overall inductor volume, core and winding losses, faster transient responses, reduced turns ratio, which lessens the effects of leakage inductance, simple winding structure, as well as improved current ripples for a three-phase coupled inductor. The main reason for the limitation of the existing studies is their choice of inductor geometry, as no new inductor geometry is proposed, and the focus is more on the control and design optimization of the existing inductor geometries. The conventional inductor geometries have inherent problems, which lead to current unbalance in the phase legs of the inductors [90]. A lot of research is focused on improving the current sharing and minimizing the current imbalance using complicated control theories. However, no significant effort has been made to deal with the root of the problem by proposing new inductor geometries that ensure better current handling as well as offer significantly high power density compared to the conventional ones [91]-[92]. The typical three-phase interleaved boost converter topology is shown in Fig 2.2.1 and the working principle for balanced phase currents is depicted in Fig 2.27.

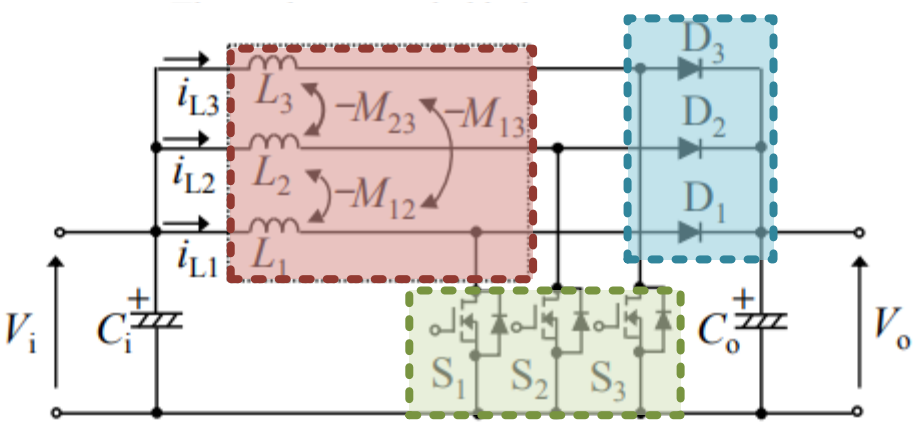


Figure 2.26: Three-Phase Interleaved Converter Topology

Finite-element analysis (FEA) of magnetic inductors provides a precise prediction of inductor performance, including fringing effects, leakage, and saturation, based on shape and material factors. However, the long nonlinear magnetic FEA's computational time requirements make them unsuitable for automated design. Researchers have recently achieved

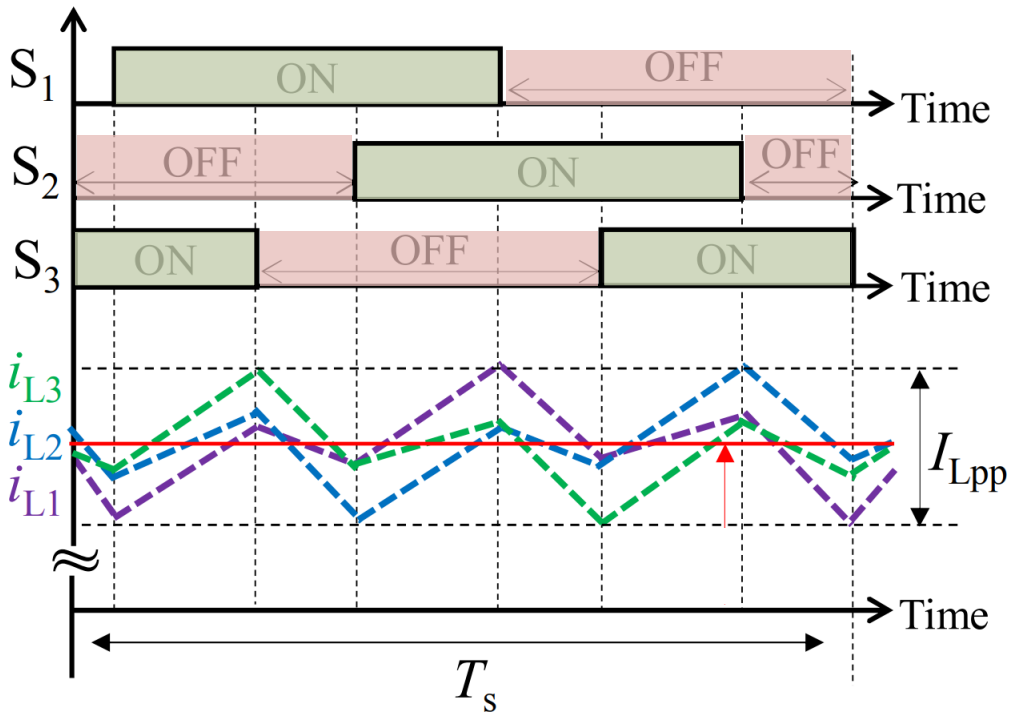


Figure 2.27: Working Principal of Interleaved Converter Topology

tremendous success in reducing the calculation time of magnetic FEA by developing reduced-order state-space models [93]-[94]. These models, however, necessitate an initial FEA for every modification to the geometry or material, making them unsuitable for automated design. In contrast, magnetic equivalent circuit analysis (MEC), which is highly efficient from a computational perspective, is also based on physical geometry and material properties. Almost every basic course of magnetics introduces this well-known approach. However, the method necessitates a high degree of engineering judgment; the accuracy is fairly low unless much care is used in determining the various permeances.Many times, MEC modeling is thought of just a crude approximation. In order to address the shortcomings of the conventional MEC methodology, more simplified circuit components have been added [95]-[96]. In [97], to determine the inductance about an operational point, more circuit components and a linearized model were employed. Its ability to estimate the incremental inductance in both the linear and saturated regimes, however, has not been demonstrated. Additionally, these techniques do not address the closed-formed fringing and leakage path models with an analytical method applicable to any core dimension.

This research proposes a new star-shaped inductor geometry designed especially for an interleaved DC-DC converter application that offers high power density due to reduced

height, tackles the problems of high airgap fringing flux losses, uneven flux distribution, overall improved magnetic behavior, and three-phase current un-balancing associated with the conventional bulky inductors. Additionally, a new high-fidelity magnetic equivalent circuit (HFMEC) model is developed and used in the design of this star shape. This model incorporates magnetic saturation as well as improved analytical formulas for all leakage and fringing flux routes. By including the three-dimensional (3-D) component of both horizontal and vertical slot leakage, which are both typically disregarded, the errors related to the conventional magnetic equivalent circuit (MEC) modeling are decreased. As far as the author is aware, this is the first work to use a three-phase inductor geometry with the high-fidelity technique.

2.2.2 high-fidelity magnetic equivalent circuit modeling

The goal of the proposed HFMEC model is to detail expressions for the proposed inductor geometry along with the anhysteretic flux and current relationship. Figure 4a presents the HFMEC of the proposed inductor geometry. The core is represented with J nodes and K branches. f_j is the magnetomotive force of the j^{th} node with respect to ground. Each branch consists of an MMF source (F_k) with a series permeance element P_k, which corresponds to voltage sources and conductances, respectively, in the circuits analogy. The three windings are wrapped around each core, resulting in a magnetomotive force (MMF) $U = Ni$, where N is the number of turns and i is the current. Then the branch k permeance can be defined as in Equation 2.22.

$$P_k = \frac{(A_k)}{(L_k)}\mu \tag{2.22}$$

where A_k is the magnetic flux cross-sectional area, L_k is the path length, and μ is the absolute permeability that can be the function of field intensity μ_B or flux density μ_H. For ease of understanding, the permeances can be divided into three categories for each phase, as shown in Table 2.4.

Table 2.4. Permeances Categorization for HEMEC

The auxiliary leakage permeances P_{U1}, P_{U2} and P_{U3} are easily dealt with separately for computational efficiency as the potential across these elements is known. The representation and calculation of airgap and leakage permeances is the major difference between the proposed HFMEC and the traditional MEC approach. The calculation for the straight permeances is straight forwarded and computed using Eq 2.22.

Phase	Straight Permeances	AirGap Permeances	Leakage Permeances
Phase 1	$P_1 - P_{10}$	$P_{11} - P_{13}$, P_{111}	$P_{14} - P_{20}$
Phase 2	$P_4 - P_6$, $P_{21} - P_{27}$	P_{13}, P_{28}, P_{281}, P_{31}	$P_{29} - P_{34}$, P_{44}
Phase 3	$P_8 - P_{10}, P_{24} - P_{26}$ $P_{36}, P_{37}, P_{40}, P_{41}$	P_{38}, P_{381} P_{31}, P_{12}	$P_{37} - P_{40}$, P_{35}, P_{42}, P_{43}

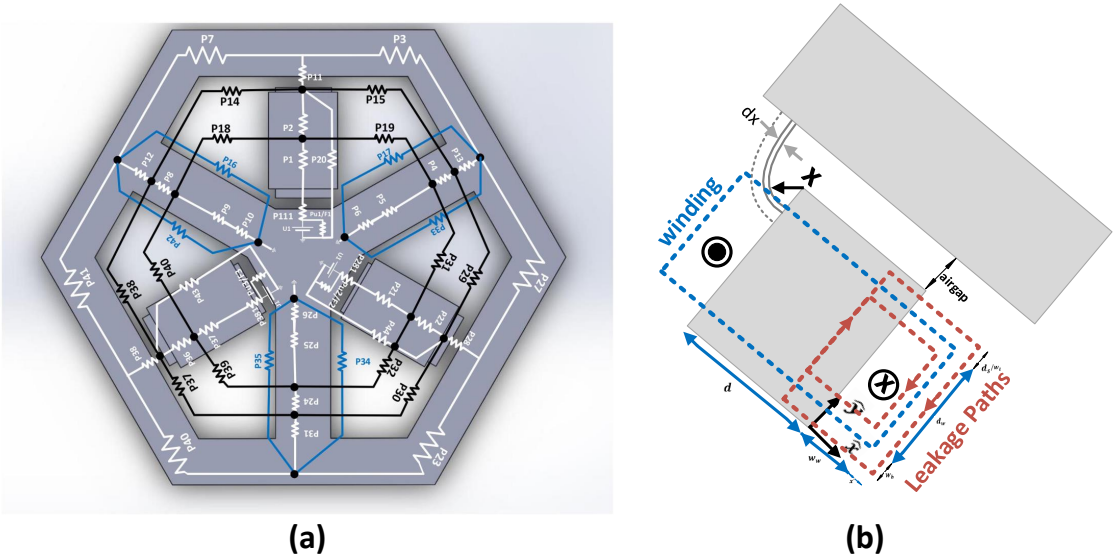


Figure 2.28: (a) HFMEC Model (b) Air-Gap Fringing and Leakage Paths

2.2.2.1 Air Gap Permeances

To start with the air gap permeances calculation, it is to be taken into account that the magnetic flux through the airgap causes a fringing effect [98]. The permeances in the gapped region were calculated using the established method described in [99]. The fringing paths for the geometrical structure are depicted in Fig 2.28. here, the detailed equations for one phase will be presented, which can be easily replicated for the other phases. So for phase 1, the airgap permeances can be expressed as

$$P_{12} = P_{13} = P_{of} + P_{if} + P_{bf} + P_{ff} + P_{gf} \tag{2.23}$$

$$P_{111} = P_{11} = 2P_{if} + P_{bf} + P_{ff} + P_{gf} \tag{2.24}$$

The total airgap permeance can be distributed into the fringing effect on the outside face (P_{of}), inside face (P_{if}), tangent (P_{bf}), radial (P_{ff}) and gap permeances (P_{gf}), whereas ω is the width of the legs in the inductor geometry.

$$P_{of} = \frac{\mu_o d}{\pi} ln|1 + \frac{\pi\omega}{g}| \tag{2.25}$$

$$P_{if} = \frac{2\mu_o d}{\pi} ln|1 + \frac{\pi\omega}{g}| \tag{2.26}$$

$$P_{bf} = P_{ff} = \frac{\mu_o \omega}{\pi} ln|1 + \frac{\pi\omega}{g} \tag{2.27}$$

$$P_{gf} = \frac{\mu_o \omega d}{g} \tag{2.28}$$

2.2.2.2 Leakage Permeances

For phase 1, considering the HFMEC model, the leakage permeances P_{14} and P_{15} correspond to the horizontal flux, which doesn't enter the windings and also avoids crossing the center and air gaps. P_{16} and P_{17} corresponds to the vertical flux along the edges. Moreover, the P_{18}, P_{19} , P_{20} and P_{U1} similarly also corresponds to vertical and horizontal flux components. However, the penetration of these flux elements into the windings increases the complexity due to the fact that now all the fluxes are not linking the windings. Ampere's law can be used to find the leakage flux intensities.

$$H_{xs} = \frac{Ni}{d_w \omega_s} y \quad for$$

$0 \leq y \leq d_\omega$
$\mathrm{Ni}\frac{}{\omega_s for}\ \mathrm{d}_\omega \leq y \leq d_s$ (2.29)

H_{xs} presents the horizontal field intensities at the vertical y position where the current is i with a winding of N number of turns. From utilizing the concept of energy in a volume of space,

$$P = \frac{\mu_o}{N^2 i^2} \int_V |\vec{H}| dv \tag{2.30}$$

After substitution,

$$P_{xs} = \frac{1}{3} \frac{\mu_o d_w d}{\omega_s} \quad for$$

$0 \leq y \leq d_w$
$\mu_o d(d_s - d_w)\frac{}{\omega_s for}\ \mathrm{d}_\omega \leq y \leq d_s$ (2.31)

In addition to the presented permeance, there is also a portion of permeance of the horizontal component that fringes out on both the front and back sides of the core (P_{xf}). Considering the path length of $\pi r + \omega$, the horizontal fringing field intensity (H_{xf}) can be found through a similar approach used in Eq 2.30 which yields

$$P_{xf} = \frac{1}{3}\frac{\mu_o d_w}{\pi} ln|1 + \frac{\pi w}{w_s}| \quad for$$

$0 \leq y \leq d_w$
$\mu_o(d_s - d_w)_{\overline{\pi ln|1+\frac{\pi w}{w_s}|for}}$ $\mathrm{d}_\omega \leq y \leq d_s$ (2.32)

As the P_{18} and P_{19} corresponds to the horizontal leakage permeance for the region $0 \leq y \leq d_w$, and can be represented as:

$$\begin{aligned} P_{18} = P_{19} &= P_{xs|0\leq y\leq dw} + 2P_{xf}|_{0\leq y\leq dw} \\ &= \tfrac{1}{3}\tfrac{\mu_o d_w d}{w_s} + \tfrac{2\mu_o d_w}{3\pi} \ln|1 + \tfrac{\pi w}{2w_s}| \end{aligned} \tag{2.33}$$

P_{14} and P_{15} corresponds to the horizontal leakage permeance for the region $d_w \leq y \leq d_s$, and can be represented as:

$$\begin{aligned} P_{14} = P_{15} &= P_{xs|dw\leq y\leq ds} + 2P_{xf}|_{dw\leq y\leq ds} \\ &= \tfrac{\mu_o d}{w_s}(d_s - d_w) + \tfrac{2\mu_o(d_s - d_w)}{\pi} \ln|1 + \tfrac{\pi w}{2w_s}| \end{aligned} \tag{2.34}$$

Because of the vertical component $\vec{H}$, there are vertical leakage penetrations. The verticle component $\vec{H}$ in the descending direction must logically equal the verticle component in the upward or opposite direction. By applying the ampere's law in a similar fashion as it was applied to the horizontal components, we get

$$\int_0^{d_s+g} H_{ys} dx = Ni\frac{2x}{w_w}$$

Using the same energy in a volume space concept, it can be written that

$$\begin{aligned} P_{ys} &= \tfrac{1}{12}\tfrac{\mu_o d w_w}{d_s+g} \\ for\ &\text{-w}_w/2 \leq y \leq w_w/2 \end{aligned} \tag{2.35}$$

The auxiliary leakage permeance is given by

$$P_{U1} = 2P_{ys|\frac{-w_w}{2}\leq x\leq\frac{w_w}{2}} = \tfrac{\mu_o d w_w}{6(d_s+g)} \tag{2.36}$$

Thus the vertical leakage permeances can be obtained as,

$$P_{16} = P_{17} = \frac{\mu_o d(w_s - w_w)}{d_s + g} \tag{2.37}$$

Considering the P_{20}, which is associated with the windings end, the leakage flux comprises two paths, i.e. the internal leakage path and the external leakage path. So for ease of computation, a rectangular path shown in Fig 4b will be considered. This term plays a very minimal role in the overall result, so the approximation doesn't affect the accuracy. If x' is the maximum distance beyond the winding width w_w, to which the external flux propagates, then the reluctance (inverse of permeance) can be expressed as

$$R = \frac{1}{\mu_o w_c}[(\frac{1}{w_t} + \frac{1}{w_b})(w_w + \frac{x'}{2}) + \frac{2d_w + w_t + w_b}{2x'}] \tag{2.38}$$

x' will be such that it minimizes the reluctance

$$x' = \sqrt{\frac{(2d + w_t + w_b) w_t w_b}{w_t + w_b}} \tag{2.39}$$

For the internal permeance, the path length (p) and area (a) can be depicted as a function of x

$$p(x) = 2\sqrt{2}x + |d_w - 2w_w| \tag{2.40}$$

$$a(x) = x^2 + \frac{x}{\sqrt{2}}|d_w - 2w_w| \tag{2.41}$$

From Eq 2.40 and 2.41, the internal field intensity expression can be o obtained as $H_{ilc}(x) = \frac{Nia(x)}{w_w d_w p(x)}$. Substituting into Eq 2.30 yields,

$$P = \frac{\mu_o \omega}{8\omega_w^2 d_w^2}[k_2^4 + \sqrt{2}k_1 k_2^3 + \frac{1}{4}k_1^2 k_2^2 - \frac{\sqrt{2}}{8}k_1^3 k_2 + \frac{k_1^4}{16} ln(1 + \frac{2\sqrt{2}k_2}{k_1})] \tag{2.42}$$

where $k_1 = |d_w - 2w_w|$,
$k_2 = \sqrt{2}w_w(d_w > 2w_w)\, and\, \sqrt{2}\frac{d_w}{2}(d_w <= 2w_w)$. Hence the element's total internal permeance comes out to be $P_{20} = 2(P + R^{-1})$

2.2.2.3 Model Validation

To validate the presented HFMEC model, the designed core made of FINEMET® FT-3M material from Hitachi was used, and the inductor was fabricated. This nanocrystalline material is formed through the annealing of amorphous ribbon that consist of Fe, Nb, B, Si

and Cu. The molten alloy is spun and cast onto a cooling wheel to achieve quick quenching,

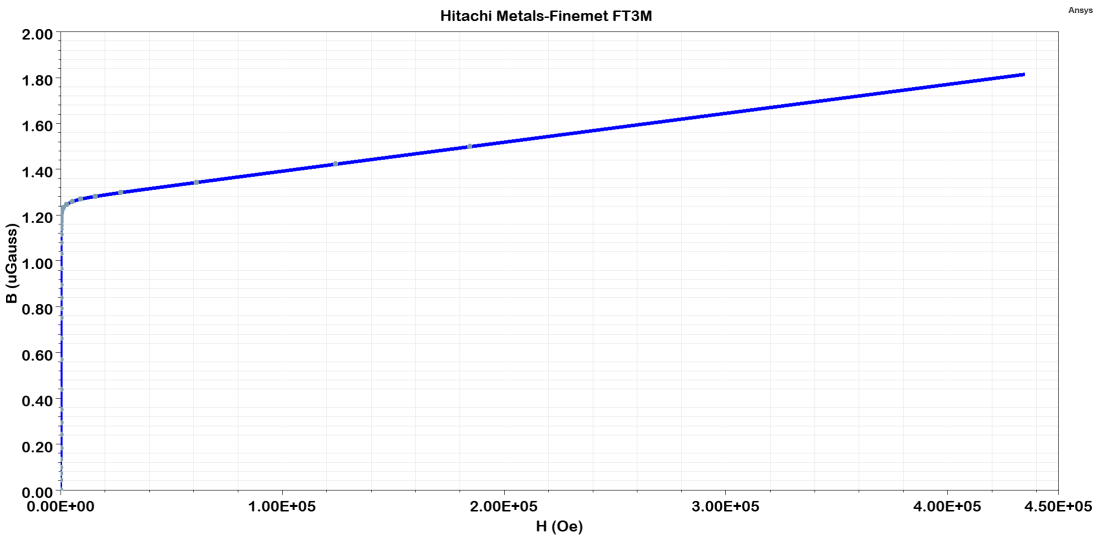


Figure 2.29: BH Curve of the used FT3M Material

avoid crystallization, and maintain the material's workability when creating the ribbon. The material is crystallized in an annealing profile at a temperature at or above 500 C for on the order of one hour after the amorphous ribbon is formed into a tape-wound core. With a maximum operating temperature of 125 C, the final core material has a grain size of roughly 10 nm and a saturation flux density of 1.23 T. Figure 2.29 shows the obtained BH-curve for the selected magnetic material. The reason for choosing this material lies in its magnetic and thermal properties [100]-[98]. Figure 2.30 shows the thermal performance comparison of FINEMET and another popular material (HTX-002) [101]. It can be observed that the thermal performance of the FINEMET is better, which makes it an ideal candidate to be used in EV applications where the operating conditions are harsh and affected by external temperatures. Initially, 15 turns were wounded around each phase.

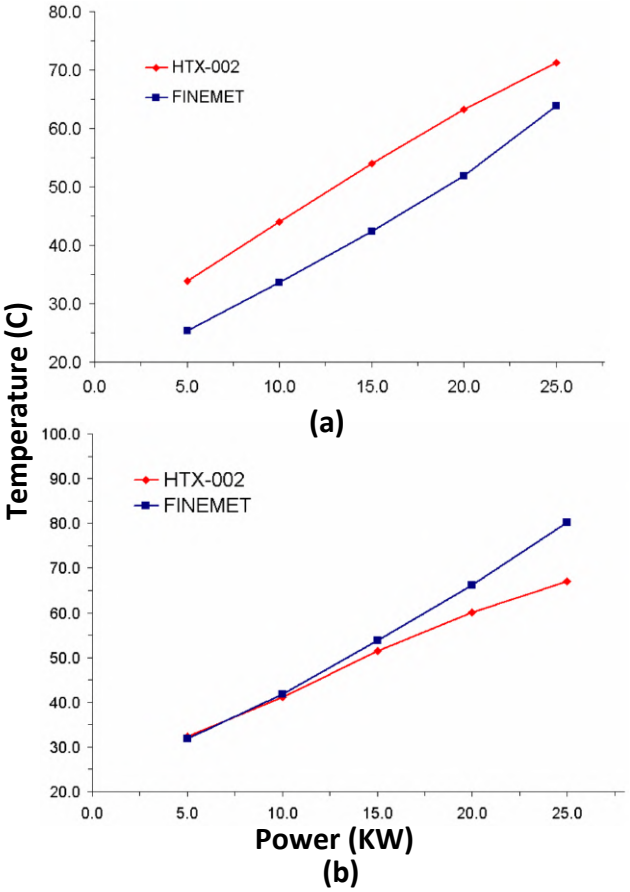


Figure 2.30: Thermal Performance Comparison a) Core b) Winding

The comparison between the proposed model-based projected features and the FEA-based measured characteristics is shown in Figure 7, and it is clear that the suggested model is accurate and closely aligns with the FEA results, whereas it took much less time as compared to the time taken by the FEA analysis with a considerably large mesh size.

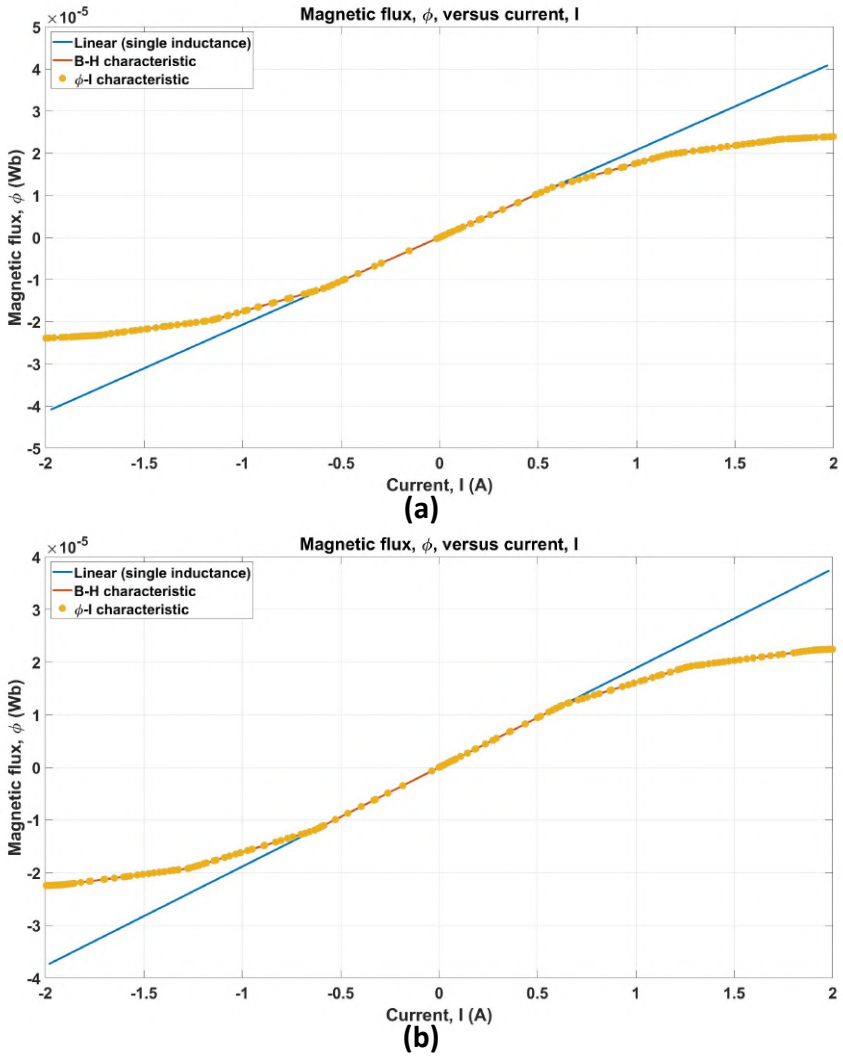


Figure 2.31: Comparison of (a) Measured (b) Predicted , Flux Characteristics

2.2.3 Electromagnetic Analysis

To determine the behavior and performance of the designed inductor geometry, a thorough electrostatic and magnetostatic analysis was performed in the ANSYS-MAXWELL 3D environment. The magnetic analysis is very important here, as this inductor geometry was designed from scratch, so the analysis is an essential step before the manufacturing phase. Considering the operating conditions and input parameters of the interleaved converter for which this inductor geometry is designed, the structure was simulated to confirm its behavior according to the required magnetic field strength and magnetic flux density. Figure 2.32 presents the obtained magnetostatic analysis.

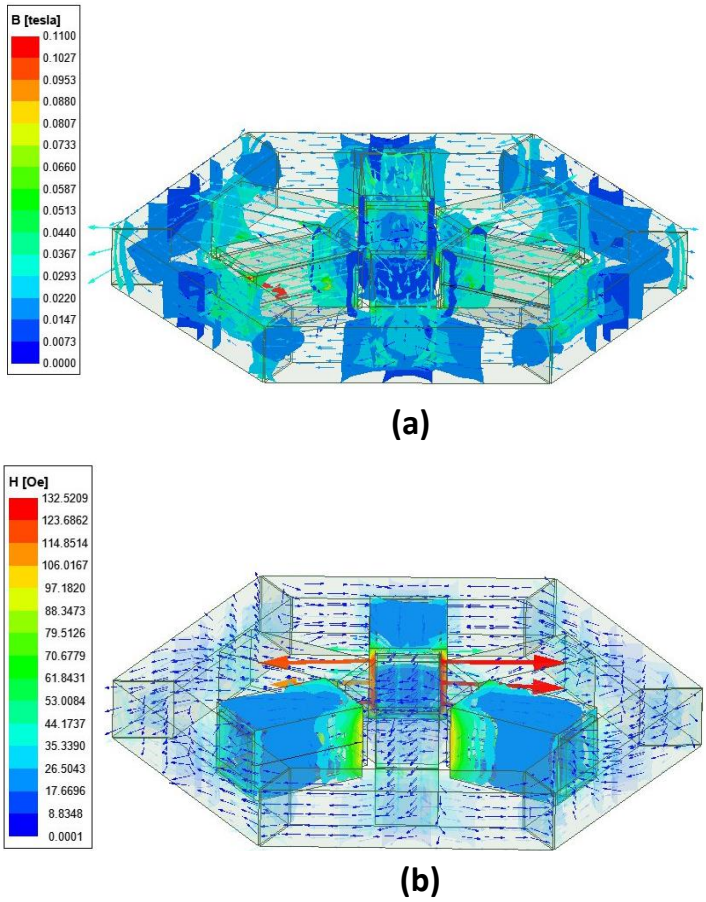


Figure 2.32: Magnetostatic Analysis (a) Magnetic Field Strength (b) Magnetic Flux Density

Moreover, as the operating conditions inside an electric vehicle, especially in a hybrid electric vehicle, are thermally harsh, the thermal analysis to depict the behavior of the designed inductor at various load conditions needs to be determined. However, for the thermal modeling, the power loss information is required, which can be obtained from Fig 2.33. By modeling the power loss relation, the thermal behavior of the inductor was observed at different load conditions. As the inductor is designed to easily operate up to 30KW, in regard to this upper limit, a heat sink is required, however at nominal loads, no heat sink is required as the unique geometry of the inductor enables good airflow access to all the windings, which improve the overall thermal behavior of the designed inductor. Fig 2.34 shows that once the heat sink is attached to the inductor geometry, the temperature of the inductor and the windings is within the acceptable temperature range. The thermal analysis was done in ANSYS-Icepak.

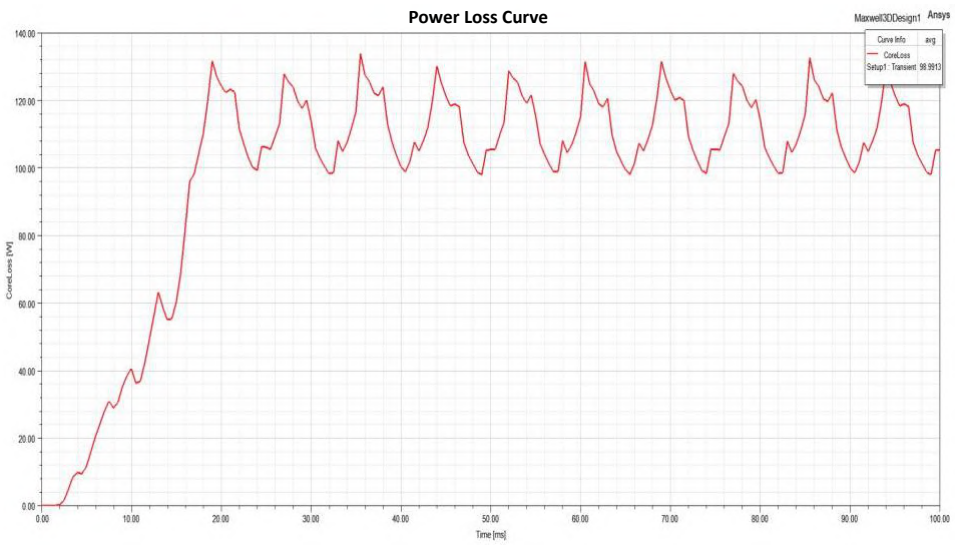


Figure 2.33: Power Loss Curve of Designed Inductor Geometry

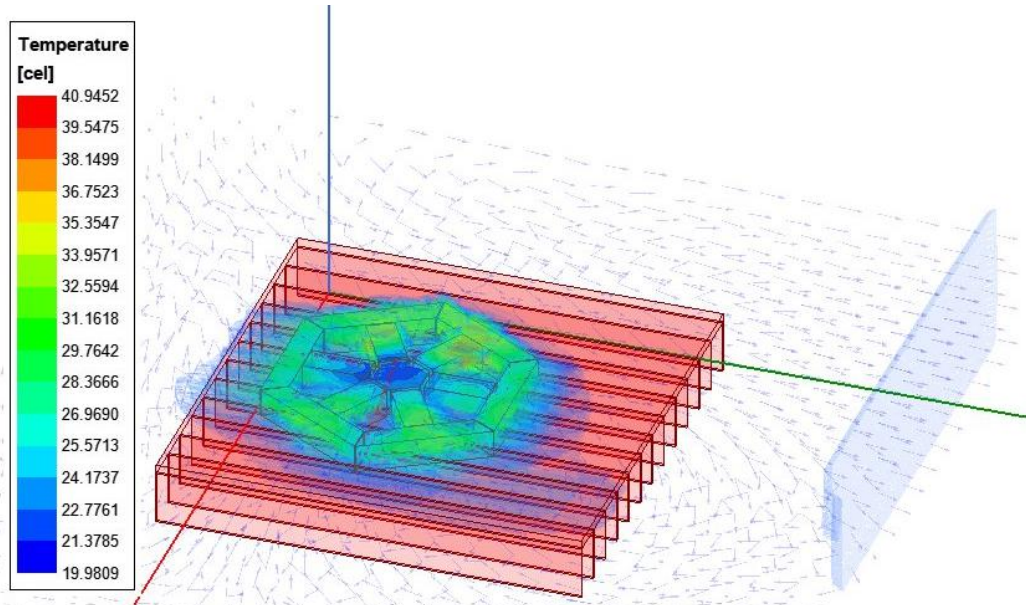


Figure 2.34: Thermal Analysis of Designed Inductor Geometry

2.2.4 Experimental and Simulation Results

For the experimental validation of the designed inductor, a three-phase interleaved converter setup was built, integrated with the designed inductor, and tested at various operating conditions. The fabricated inductor and the overall test bench setup are shown in Fig 2.35 a and Fig2.35b, respectively.

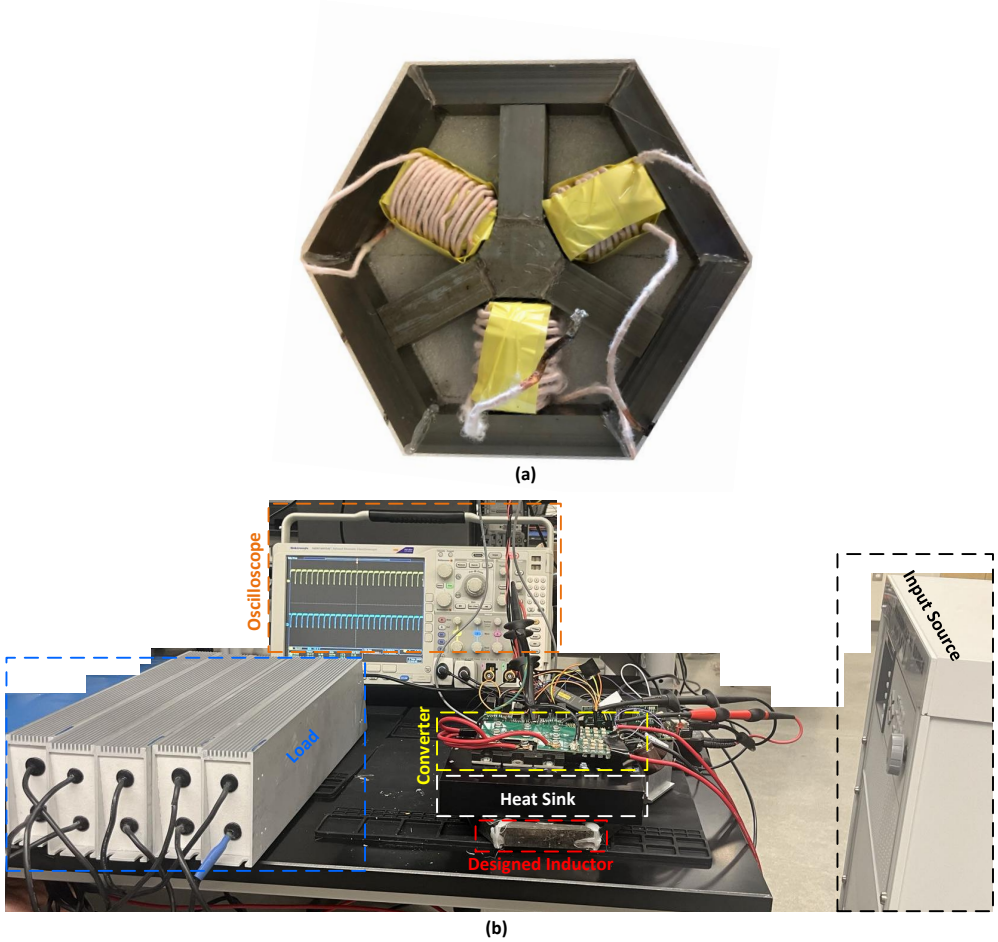


Figure 2.35: (a) Designed Inductor (b) Test Bench

To test the designed inductor, these different modes were achieved by varying the inductance value of the inductor, which is one of the flexibilities this designed geometry offers, as the whole inductor core doesn't need to be disturbed to change the number of windings. Table II depicts the different modes of operation and the corresponding inductance values. Figure 2.36 shows the experimental three-phase current waveforms obtained for the discontinuous current mode, boundary mode, and continuous current mode. It can be observed that the waveforms obtained adhere to the simulation results, as well as all the phase currents are balanced, which highlights the stable structural design of this inductor as the interleaved converter was operated in an open loop control to prove the current balancing property of the proposed inductor geometry. Figure 2.36 shows the experimental three-phase current waveforms obtained for the discontinuous current mode (L= $66uH$, Load(ohms)=15), boundary mode (L= $73uH$, Load(ohms)=15), and continuous current mode (L= $100uH$, Load(ohms)=15). It can be observed that the waveforms obtained adhere to the simulation

results, as well as all the phase currents are balanced, which highlights the stable structural design of this inductor as the interleaved converter was operated in an open loop control to prove the current balancing property of the proposed inductor geometry.

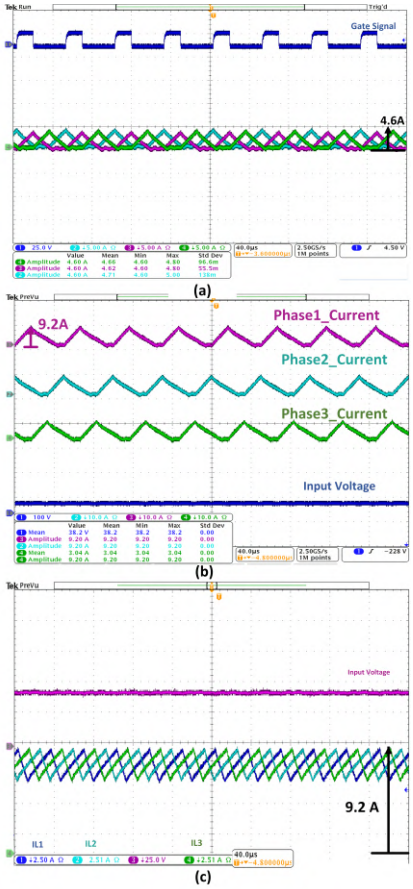


Figure 2.36: Experimental Results (a) DCM Mode-Three Phase Currents (b) Boundary Mode-Three Phase Currents (c) CCM Mode-Three Phase Currents

Another major goal of this research was to increase the power density of the overall interleaved boost converter through this new inductor design, in view of the low vertical space available for power electronics units in the chassis of electric vehicles. This problem of limited vertical space was solved through the designed inductor, as it is only 2 cm high. Compared to the conventional inductors of the same power level, a decrease of 120% in the inductor height was observed, as shown in Fig 2.37, which improved the overall power density too. It is to be noted that the horizontal space in the vehicle power electronics is not as limited as the vertical one therfore this research wa specially focused on reducing the height and maintaining other dimensions accordign to the space available. No significant difference was observed in the weight (around 80 grams).The comparison is based on an 8cm high EE

core-shaped three-phase inductor of the same material and is capable of providing identical inductance values.

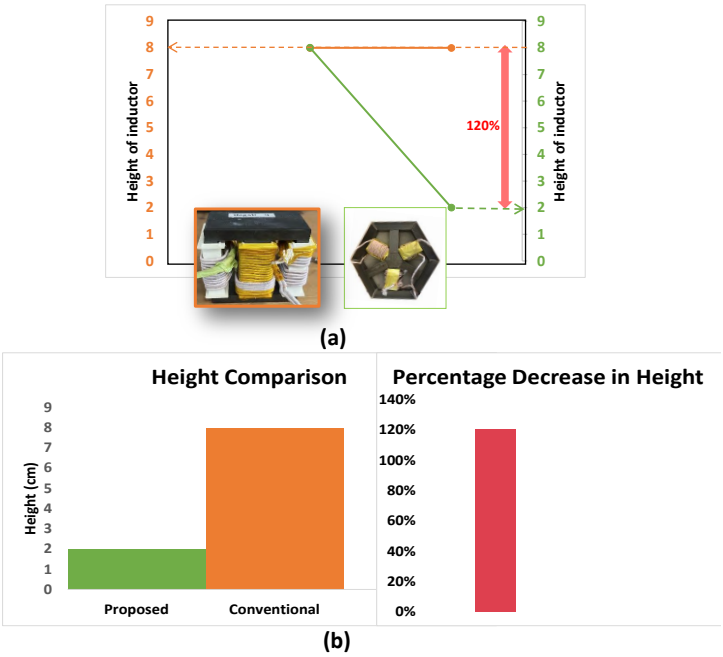


Figure 2.37: (a)Conventional vs Proposed and Design Inductor Geometry (b) Height and Power Density Comparison

In this research, a very high power density three-phase interleaved boost converter was realized by designing a unique geometrical star shape inductor. Moreover, a new high-fidelity modeling approach was presented and validated as an alternative to the FEA analysis, which is a significant step forward in the domain of automated magnetics design.

CHAPTER 3

Bare-Die Embedded PCB Technique for Small Mobility Applications

3.1 Bare-Die Embedded PCB Technique

3.1.1 Introduction

Small mobility vehicles such as electric scooters are becoming an integral part of the transition towards electrified transportation. However, the limited driving range and the lack of onboard charging capability are the major challenges for the widespread adaptation, which arises due to the limited space for power electronics units and batteries on the chassis of small mobility vehicles. This research introduces a new bare-die embedding PCB packaging technology, ensuring a very compact, high power density, and integrated design for the power electronics unit. The design incorporates the bare die of the switching devices into the PCB layers and uses multilayers for routing and cooling purposes. A MOSFET bare-die is embedded into the FR4 layers using the stomach cell approach, electrically connected, and cooled through laser-drilled microvias and copper fills. The electrothermal codesign reduces the parasitic loop inductance by 74%, increases the power density by 113%, and enhances the driving range of the small mobility vehicle by 16.6% compared to the traditional TO-247 packaging approach. Moreover, a new thermal model is also presented and validated for the bare-die embedded board. A high power-density power electronics unit integrating the motor drive and the onboard charger was developed using the proposed bare-die embedding technology, and a benchmark comparison was done to evaluate the effectiveness of the proposed bare-die embedding technique.

Small mobility vehicles such as electric scooters have the ability to decarbonize transportation at the cellular level and have become a popular mode of global micromobility, thus becoming a crucial part of the electric transportation revolution. In particular, the urban centers are the hotspots where mobility needs can be fulfilled by small mobility vehi-

cles; therefore it's now considered as an essential component of the urban mobility planning worldwide. The global E-scooter market was valued at USD 19.96 billion in 2020 and is projected to reach USD 40.3 billion by 2030, which is a compound annual growth rate of 8.1% [102]. The North American e-mobility revolution continues, as 58.5 million trips were recorded on the E-Scooters in the year 2022. The overall shared micro-mobility trips are up by 40% since 2018, which is a 35-fold increase from 2010, according to the National Association of City Transportation Officials (NACTO) [103]. The major challenges in the widespread adoption of small mobility vehicles are the limited driving range and unavailability of onboard charging flexibility [104]. The portable and lightweight design requirement of the e-scooters or small mobility vehicles makes it impossible to increase the driving range and incorporates the onboard charger by increasing the chassis dimension. Traditionally, the power electronics unit inside the e-scooters only contains the motor drive circuitry and a separate off-board charger, which the user needs to carry along the ride or the alternative is to return to the starting point for recharging. In this research work, this problem is solved by increasing the power density of the motor drive, which leads to additional space required for the on-board charging circuitry or battery extension.

The 2025 technical targets published by the US Department of Energy (DOE) aims to reach a power density of 33KW/L for a 100 KW traction drive system, which is an increase by a factor of 5.5 and an 88% volume reduction compared to the state-of-the-art technology. Achieving these goals primarily depends on semiconductor power device improvements in packaging, heat management, losses, and electrical switching performance [105]. Magnetics was the limitation for the power density improvement for a long time, but with the introduction of wide-bandgap devices, enabling high-frequency operation, the size of magnetics can now be reduced significantly [106]. However, today's challenge is the power-switching devices' size and packaging, which also come with fundamental electrical and thermal limitations. Researchers have explored several techniques to address the electrical, thermal, and reliability challenges associated with traditional packaging. Traditionally, ceramics-based modules such as direct bonded copper (DBC) are used due to their properties such as good insulation, high thermal conductivity, and ampacity. Bare dies are attached to the top side copper of DBC [107]. The connections between the power component, substrate, and substrate to the frame are made using Aluminum wire bonds, utilizing several parallel wire connections to ensure the required module ampacity [108]. In spite of the shortcomings and challenges such as lengthy processing, full area DBC substrate soldering, potting, and non-reliable bonding were accepted due to lack of alternatives and due to the fact that the performance was acceptable for the required applications. In the past decade, the requirements for power density, voltage, power, and switching frequency have increased

significantly due to advancements in power electronics and the paradigm shift towards electrified transportation and power-converted dominated power systems [109]. Moreover, due to the increased switching frequency, the parasitic effects of such traditional modules, such as inductance, capacitance, etc., are important to consider. In the current high switching frequency applications, the conduction and switching losses are of great importance and consideration [110]. High switching frequency helps to reduce the size of passive and magnetic components, improving the power density and overall volume. The drawback is that high switching frequency means high switching losses; therefore, minimizing the parasitic at the lowest level is extremely important to reduce the overall losses and increase efficiency. In the currently used power modules, bond wires are the main sources of parasitic inductances directly proportional to their shape, number, and length [111]. In addition, the distance between the gate driver and the gate contact of the power module is a source of parasitic, which is a concerning issue, and it has become more crucial with the introduction of wide band gap electronics whose gates are too sensitive and prone to be damaged by such parasitic effects [112]. The bond wires also add to the non-reliability, considering their delicate structure and soldering. Bond lifting from the Silicon power devices is a major cause of power module failure (difference between the coefficient of thermal expansion between Aluminum and Silicon), which is directly related to temperature; therefore for high-power applications, which leads to extreme operating temperatures, the power module reliability is questionable. Silver sintering as a solder replacement is another technology that is attaining the attention of power module manufacturers due to its improved reliability [113]. However, the expensive DBC substrate is still present there, which is a disadvantage.

In [114], an approach for integrating a decoupling capacitor with a half-bridge switch module is presented using AIN DBC. In [115] and [116], the gate driver ICs were integrated onto the same substrate to improve the parasitic performance further. In [117], a hybrid DBC-PCB approach is presented where the power and gate connections are formed using AIN DBC and PCB, which enables design freedom for the gate driver circuitry. Although the discussed approaches result in increased power density and better parasitic performance compared to the conventional packages, wire bonds are still involved in these solutions, which pose reliability risk, increased inductance, and low current capacity. Furthermore, double-sided cooling is also impossible when wire bonding is used [118]. In [119], a wire bondless approach is adopted by utilizing AIN and Al_2O_3 DBC substrates and using wide planar copper bonds for the die-interconnection. The flip-chip bonding technique, in which the source and gate terminals are directly attached to the substrate, is discussed in [120] and [121] to achieve wire bondless integration. The die is sandwiched between the two PCBs in [122]. Using planar power overlays is another technique reported in the literature to avoid

wire bond-based connections. This technique achieves reduced power loop inductance by placing the bare dies between wide-bus planes [123]. In [124], another approach that uses heat spreaders as a substrate is introduced, where the dies are directly populated on the substrate, which in this case is the heat spreaders. In some industry application modules, the SKiN technique has been used [125], which utilizes a flex-PCB on the die top to achieve low parasitics and high power density. Although these POL and flex-based approaches result in compact packaging and low inductances, but they suffer from high parasitic capacitances due to the large overlap and small separation between the planes, and it also makes the intra-module integration challenging. A different approach by using multi-functional components (MFCs) that act as a heat sink and bus bar simultaneously is presented in [126]. In this approach, the heatsinks are directly attached to the dies. In the power-on-chip bus (PCoB) approach the die is connected to the metal substrate on both sides for better thermal dissipation. These techniques no doubt offer better thermal performance, but the close integration of the gate driver circuitry will result in a very small contact area for the heat sinks, which is a design challenge [127]. Table 3.1 provides a detailed overview and a comparative analysis of this work with the other techniques found in the literature.

To address the described shortcomings, in this research, a bare die of a MOSFET is embedded between the second and third layer of the PCB board to develop a high-power density motor drive for small mobility applications, which leads to a significant size reduction of the power electronics unit, allowing the integration of the onboard charger with the motor drive and sparing additional battery space to enhance the driving range. A benchmark comparison in terms of power density, thermal performance, parasitic inductance, and capacitance was carried out, and the benefits of this technique were analyzed from different perspectives. Moreover, this paper also provides the methodology and design rules for bare-die embedded PCB design, which are scarce in the literature and will aid the development of such PCB manufacturing techniques. In addition, a new thermal model is proposed and validated for the bare-die approach, as the traditional thermal models are not applicable here. The overall architectural block diagram of the small mobility vehicles is presented in Fig. 3.1.

3.1.2 Bare-Die Embedded Design

Bare-Die embedded design refers to embedding the power semiconductor switching devices such as MOSFET's into the layers of the printed circuit board (PCB), which is a new packaging technique and a unique philosophy for power electronics systems design. The aim is to achieve a compact design, high power density, good parasitic performance, high depth

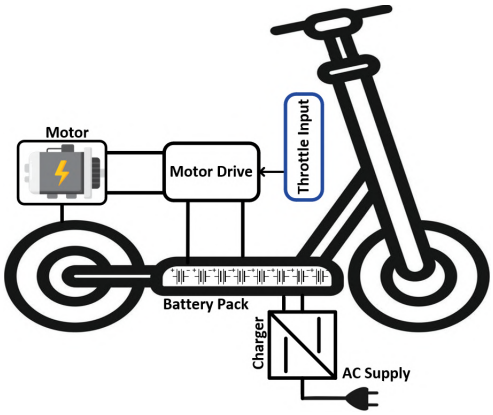


Figure 3.1: Small Mobility Vehicles Architectural Block Diagram.

Table 3.1: A Comparison of the existing techniques with the proposed one

Ref	Bond	Bondless	L_g	L_p	Cooling	Substrate	Thermal	C_{oss}
[114]	✓		3	2.4	Single Sided	AIN DBC	Low	Low
[115]	✓		N/A	7.3	Single Sided	Al_2O_3 DBC	Medium	Low
[117]	✓		N/A	3.38	Single Sided	AIN DBC	Low	Low
[116]	✓		N/A	3.4	Single Sided	Al_2O_3 DBC	Medium	Low
[128]		✓	4.3	4.5	Single Sided	AIN DBC	Low	Low
[129]		✓	6	1.6	Single Sided	Al_2O_3 DBC	Low	Low
[130]		✓	N/A	2	Double Sided	FR4-PCB	High	High
[131]		✓	N/A	0.86	Single Sided	FR4 and Al_2O_3 DBC	Medium	High
[125]		✓	20	1.4	Single Sided	Flexible Board	Low	High
[120]		✓	0.25*	4.88*	Single Sided	FR4-PCB	Low	Low
[121]		✓	N/A	1.5	Double Sided	Epoxy Resin	High	Low
[123]		✓	N/A	5	Double Sided	DBC/AMB	High	High
[132]	✓		N/A	7.5	Double Sided	Resin-Molded Heat Spreader	High	High
[133]	✓		N/A	1.63	Double Sided	AIN DBC	High	High
[126]	✓		4	8	Double Sided	PCoB	High	High
[127]	✓		N/A	N/A	Double Sided	PCoB	High	Low

*Values not considering placement of corresponding components

of integration, and low cost at the system level.

3.1.2.1 Stomach Cell Approach

The essential step to manufacture a bare-die embedded board starts with the creation of a cellular structure that contains the bare-die of the power semiconductor attached to a lead frame through transient liquid phase bonding (TLPB). The power device's die structures are impregnated into the stomach or cavities of a lead frame. In this research, a MOSFET bare die (IAUE303N08S5N009) was attached to the lead frame to form a cellular structure that can be embedded into the core of the PCB [134]-[135]. Special consideration is required for the footprint construction as it needs to be according to the dimensions of the die and allow the required spacing from the S-cell contour, which will be discussed in the design rules section. Figure 3.2a shows the constructed footprint, and Figure 3.2b presents the lead frame with cavities where the bare dies can be placed to form a planar surface. Figure 3.2c shows the formed cellular structure of a bare die attached to the lead frame, ready to be embedded into the PCB layers. The front side of the structure contains the isolated gate pad and the source terminal and also provides access to the drain side. The back side of the frame is connected to the drain for ease of thermal dissipation. While designing the footprint, a minimum cutout distance needs to be considered between the gate, source, and drain regions. Access to the gate, source, and drain will be achieved by drilling the laser vias.

3.1.2.2 Design Rules for Bare-Die Embedded PCB

Unlike the traditional PCB design and manufacturing, the process for the proposed bare-die technique is symmetrical and starts from the middle layer. As in the case considered here, the goal is to design a 4-layered PCB board embedding the MOSFET bare-die between the second and third layers. The process of the bare-die cellular structure integration starts with the deposition of thick copper layers above and below. For this purpose, thick copper layers are formed above and below the FR4 material. After milling, the cellular structure is placed or embedded between the second and third layers. Then, the remaining two layers, i.e., the first and fourth layers, are formed. The process of laser-drilled vias is carried out to form an electrical connection between the embedded bare die and the first layer. The same approach is used to connect the drain of the buried MOSFET to the bottom layer. A thermal interface material can attach a cold plate or heat sink to the bottom layer. Figure 3.3 presents the manufacturing process of the bare-die embedded PCB.

This approach of embedding the bare die provides the flexibility to merge and combine

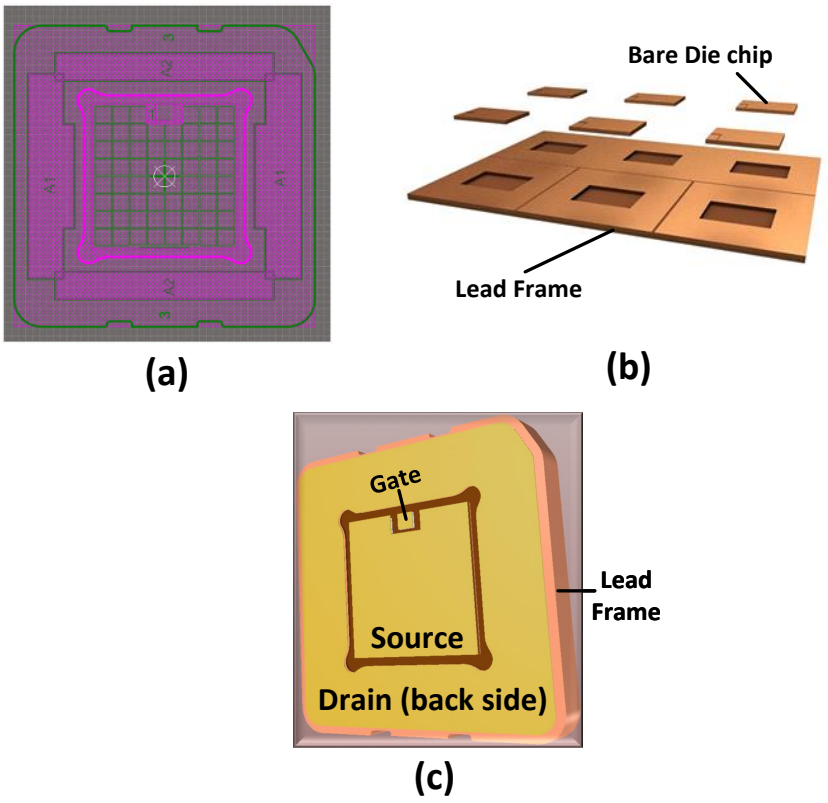


Figure 3.2: (a) Constructed Footprint (b) Lead frame cavities for bare-die (c) Bare-Die attached to the frame forming a cellular structure

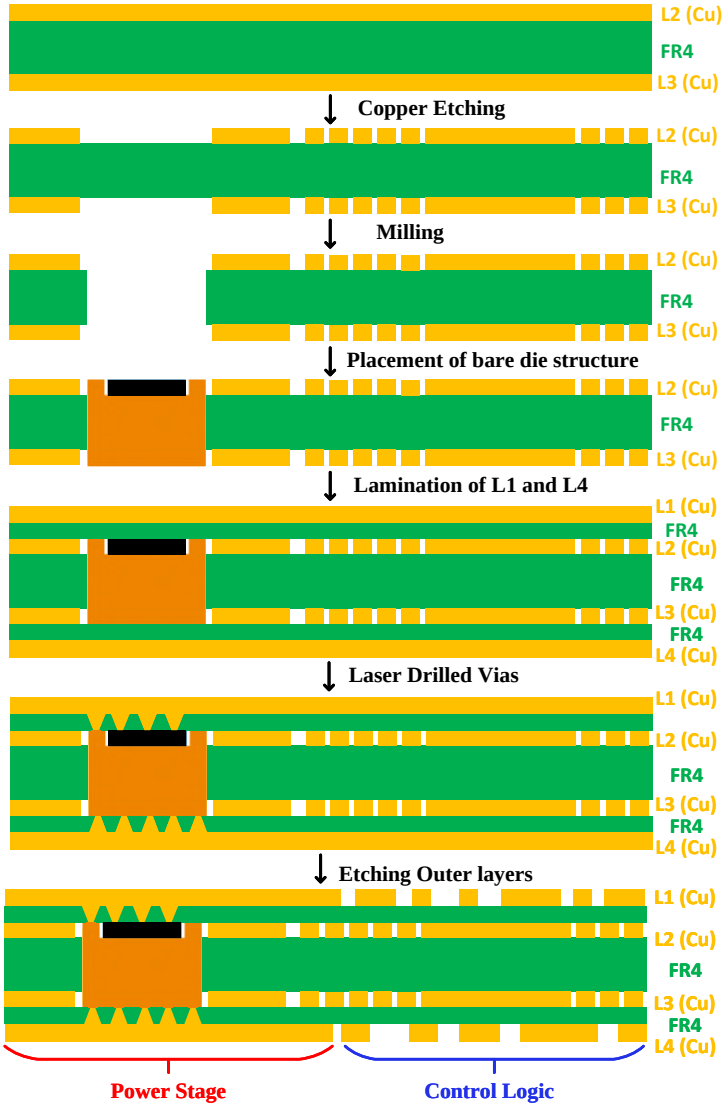
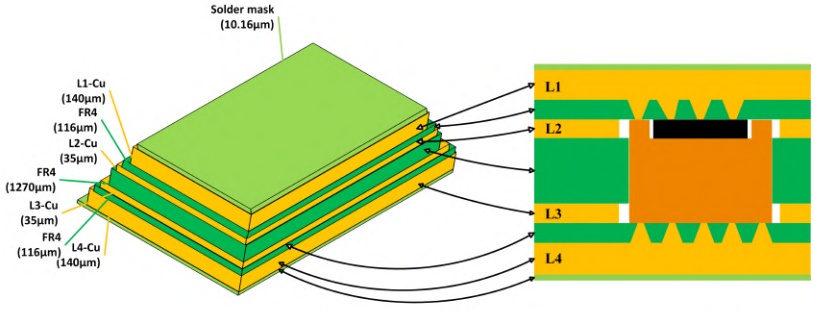


Figure 3.3: Bare-Die Embedding PCB Process

power electronics of the power stage and logic control in one single PCB without the need for additional connectors between logic and power board, which yields benefits in terms of power density, parasitic performance, reliability, and efficiency. The thickness of all copper and prepreg layers are not similar, which calls for careful consideration during the layer stack design. Generally, the dielectric layer used for embedding is much thicker than other prepreg layers. Similarly, the copper layers above and below are thicker than other copper layers to carry a high current. The added advantage of this technique is that despite the thick copper and di-electric layers, the thickness of the overall bare-die embedded board can vary between $1.2mm$ to $1.7mm$. Figure 3.4 presents the designed layer stack of the bare-die embedded PCB.



(a)

Name	Type	Thickness
Top Solder	Solder Mask	10.16µm
Top Layer (L1)	Copper (Cu)	140µm
Dielectric 1	FR4 material	116µm
Layer2 (L2)	Copper (Cu)	35µm
Dielectric 2	FR4 material	1270µm
Layer 3 (L3)	Copper (Cu)	35µm
Dielectric 3	FR4 material	116µm
Layer 4 (L4)	Copper (Cu)	140µm
Bottom Solder	Solder Mask	10.16µm

(b)

Figure 3.4: (a) Bare-Die Embedding PCB Layers (b) Designed Layer Stack

Once the layer stack is set up, the routing can be done to form electrical connections to the embedded MOSFET's gate, drain and source. The gate terminal should be accessed vertically by designing blinded laser drilled vias to minimize the gate loop inductance, which is one benefit of this technique. The source pad of the bare-die can be accessed using multiple blinded laser drilled vias, as multiple vias improve the current conduction capability. The drain can be accessed from the top as well as the bottom side of the bare die. In this design, the electrical connections to the drain were established from the top layer, and then the bottom layer was connected to the drain for thermal dissipation purposes. Because of its symmetrical design, thermal interface material that is directly mounted to a heat sink experiences less pump-out effects due to reduced warp and twist during thermal cycling.

In fact, the power device cools on both sides thanks to the thick copper layers that are positioned above and below the lead frame, which maximize heat distribution across each layer. A heat sink connected from the bottom receives up to one-third of the heat transported to the top layer and then through the entire package. For this kind of design while routing and pouring copper, it must be considered that for the thick top and bottom layers, the distance between the copper structures must be $300\mu m$. To avoid twisting or wrapping of the inner layer during the production phase, the cellular structure should get a copper cutout of $500\mu m$ from the cell contour, as shown in Fig 3.5, along with the designed layers. Another important factor in designing such bare-die embedded PCB is the size of annular rings required for the laser vias drilling. For this design, the size of the annular rings was set at $450\mu m$ as shown.

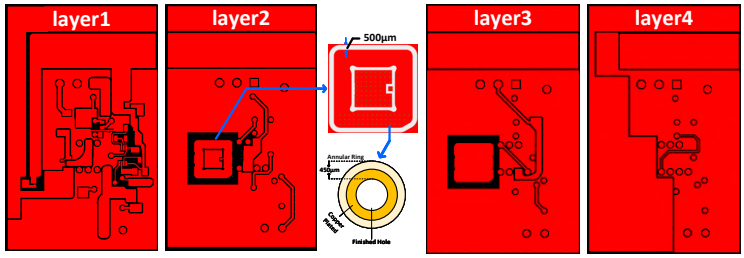


Figure 3.5: Designed Bare-Die Embedding PCB Layers and Structure Stack

The 3D view of the designed bare-die embedded PCB is shown in Fig 3.6, where the position of the bare-die can be seen. Moreover, thermal and copper-filled vias were constructed for thermal dissipation purposes, and copper-filled regions were poured on the outer layers. The detailed thermal analysis is presented in the respective section.

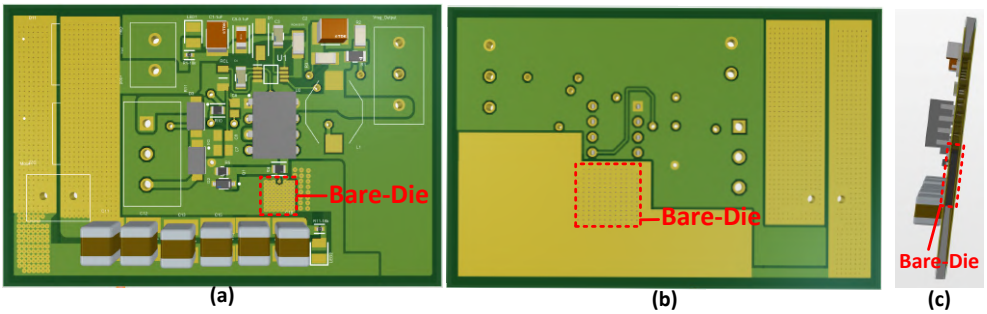


Figure 3.6: 3D View of Designed Embedded Bare-Die PCB(a)Top View(b)Bottom View(c) Side View

A summary of the design rules, specifically regarding the layer type, thickness and laser

drill vias diameter, is presented in Table 3.1.2.2.

Table 3.2.Layers and Laser Drilling Specifications

Layer and Thickness	**Line Width** (μm)	**Line Spacing** (μm)	**Plated Hole Annular Ring** (ϕ) $0.35 \leq 0.50mm$ (μm)
Layer 1 ($150\mu m$)	400	300	200
Layer 2 ($35\mu m$)	100	100	125
Layer 3 ($35\mu m$)	100	100	125
Layer 4 ($150\mu m$)	400	300	200

3.1.3 Thermal Estimation and Parasitic Analysis

Thermal performance is an important aspect to consider for power electronics packaging techniques. For the proposed bare-die embedding approach, thermal dissipation is a challenge. As the structure of the embedded die differs from the traditional packages thus, a new thermal equivalent circuit model was proposed and validated. Unlike the traditional packages in the bare-die approach, there is no junction to case $R_{th(J-C)}$ and case to ambient $R_{th(C-A)}$ resistance. Hence, the total thermal resistance is lower, which calls for better thermal performance. A traditional and proposed model comparison is presented in Fig 3.7.

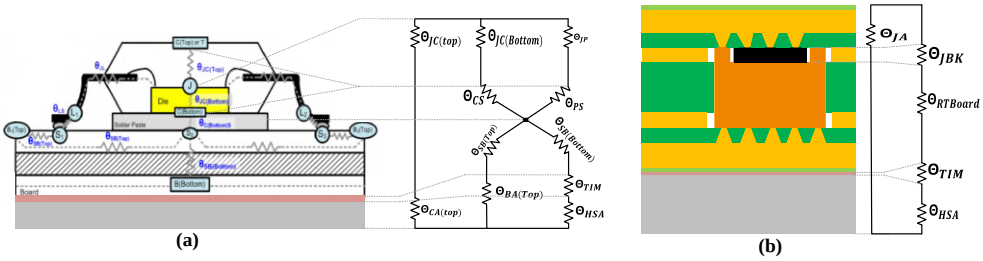


Figure 3.7: (a) Conventional Package Thermal Modeling(b)Embedded Bare Die Package Thermal Modeling

Based on the proposed model, the equivalent thermal resistance of the bare die embedded into the PCB can be modeled as

$$\Theta_{RTH} = \frac{\Theta_{JA}(\Theta_{JBK}+\Theta_{RTBoard}+\Theta_{TIM}+\Theta_{HSA})}{\Theta_{JBK}+\Theta_{RTBoard}+\Theta_{TIM}+\Theta_{HSA}+\Theta_{JA}} \tag{3.1}$$

where Θ_{JBK} refers to the thermal resistance from the bare-die junction to the back side of the attached substrate, which was known by the PCB manufacturer. Θ_{JA} is the junction to

ambient, $\Theta_{RTBoard}$ is the total thermal resistance, including the board and drilled thermal vias, Θ_{TIM} is the thermal resistance of the thermal interface material and Θ_{HSA} is the heatsink to ambient thermal resistance.

Thermal vias were used for the heat transfer, which is the most effective method for an improved vertical heat transfer. As the thermal conductivity of the FR4 material is very low, plated through hole vias between the conductive layers was used in this research. Here the temperature measurements were taken using a thermal camera. Hence the relationship between the junction of the bare die and the board can be formed through a junction-to-board characterization parameter Ψ_{JB}. If T_{board} is the temperature measured on the board surface above the bare-die location, then

$$\Psi_{JB} = (T_J - T_{board})/P_D \tag{3.2}$$

Where T_J and P_D represent the junction temperature and dissipated power, respectively. Once the board temperature is known, the junction temperature is calculated by

$$T_J = (T_{board}) + P_D\Psi_{JB} \tag{3.3}$$

Moreover, for such PCB-embedded techniques, other factors such as the size of vias, pad size, and copper fill size become very important in estimating thermal performance. The vertical structure of the multi-layered PCB vias of the plated hole nature have three paths i.e. via filler (Θ_{filler}), via barrel (Θ_{barrel}) and cooper and FR4 layers (Θ_{cu}+Θ_{FR4}). If the thermal conductivity of each material is presented by $k(W/(m^2K))$, then each of the thermal resistances can be written as Eq (3.4)-(3.6),

$$\Theta_{filler} = \frac{t_{PCB}}{k_{filler}\pi(\phi/2-t_{PTH})^2} \tag{3.4}$$

t_{PCB} is the thickness of the PCB, t_{PTH} is the plated hole thickness, t_{Cu} is the copper layer thickness, s is the inter via spacing and ϕ is the via diameter.

$$\Theta_{barrel} = \frac{t_{PCB}}{k_{Cu}\pi t_{PTH}(\phi/2-t_{PTH})} \tag{3.5}$$

$$\Theta_{Cu} + \Theta_{FR4} = [\frac{t_{Cu}}{K_{Cu}} + \frac{t_{Cu}}{K_{FR4}}][\frac{4}{(\pi+s)^2*-\pi\phi^2/4}] \tag{3.6}$$

The total vertical thermal resistance of the board is computed through Eq 3.7.

$$\Theta_{RTBoard} = \Theta_{filler}||\Theta_{barrel}||(\Theta_{Cu} + \Theta_{FR4}) \tag{3.7}$$

$$\Theta_{RTBoard} = \frac{1}{\frac{k_{filler}\pi(\phi/2-t_{PTH})^2}{t_{PCB}} + \frac{k_{Cu}\pi t_{PTH}(\phi/2-t_{PTH})}{t_{PCB}} + \frac{(\pi+s)^2 * -\pi\phi^2/4}{4t_{Cu}/K_{Cu}+t_{PCB}-4t_{Cu}/K_{FR4}}} \tag{3.8}$$

To validate the proposed thermal model and to observe the thermal performance of the bare-die embedded board, the model was first validated in the Simulink environment and then compared with the experimental results. Figure 3.8a presents the methodology used for the performance comparison that includes both the simulation and experimental data for the result comparison. In Figure 3.8b, it can be seen that the bare-die embedded PCB board performs thermally better than the conventional PCB board with discrete components in both cases, i.e., with and without a heat sink, and the proposed model follows the experimental results curve.

To better understand the difference in thermal performance between the proposed bare-die embedded PCB and the conventional one, a 3D surface plot is presented in Fig.3.9, which highlights the magnitude of the temperature difference with respect to the varying load conditions. In the presented surface plot, the change in the temperature between the two boards, i.e., the traditional benchmark PCB motor drive having discrete components and the bare-die embedded motor drive, can be seen in the corresponding load condition.

Moreover, to further understand the thermal performance and temperature distribution of the design, bare-die embedded PCB was analyzed, and thermal simulations were conducted in the ANSYS-ICEPAK to observe the performance during the design stage. This analysis helps to identify the estimated temperatures and hotspots on the designed board. Figure 3.10a shows the obtained thermal simulation results where it can be seen that the hotspots are at the points where the barer-die is embedded and on the two diodes where the maximum power dissipation occurs. Figure 3.9b shows the thermal images obtained during the experiment, which adhere to the simulation results. The benchmarked motor drive's experimental thermal image is presented in Fig 3.10c, which shows that the temperature at similar load conditions is higher than the bare-die embedded design board, which affirms the fact that the bare-die embedded technique possesses better thermal performance.

The signal integrity analysis, through which the power dissipation at each unit area, along with the current density, can be viewed and analyzed, is essential for an optimized PCB design to identify the hotspots and modify them accordingly in line with the target of having an equal power dissipation pattern and to avoid the saturation of current density points that will affect the thermal behavior of the design. In this study, the power and current density analysis was performed as shown in Fig 3.11 where the color shades represent the power dissipation and the arrows direct to the path of the power flow, which helps in understanding the performance of the design.

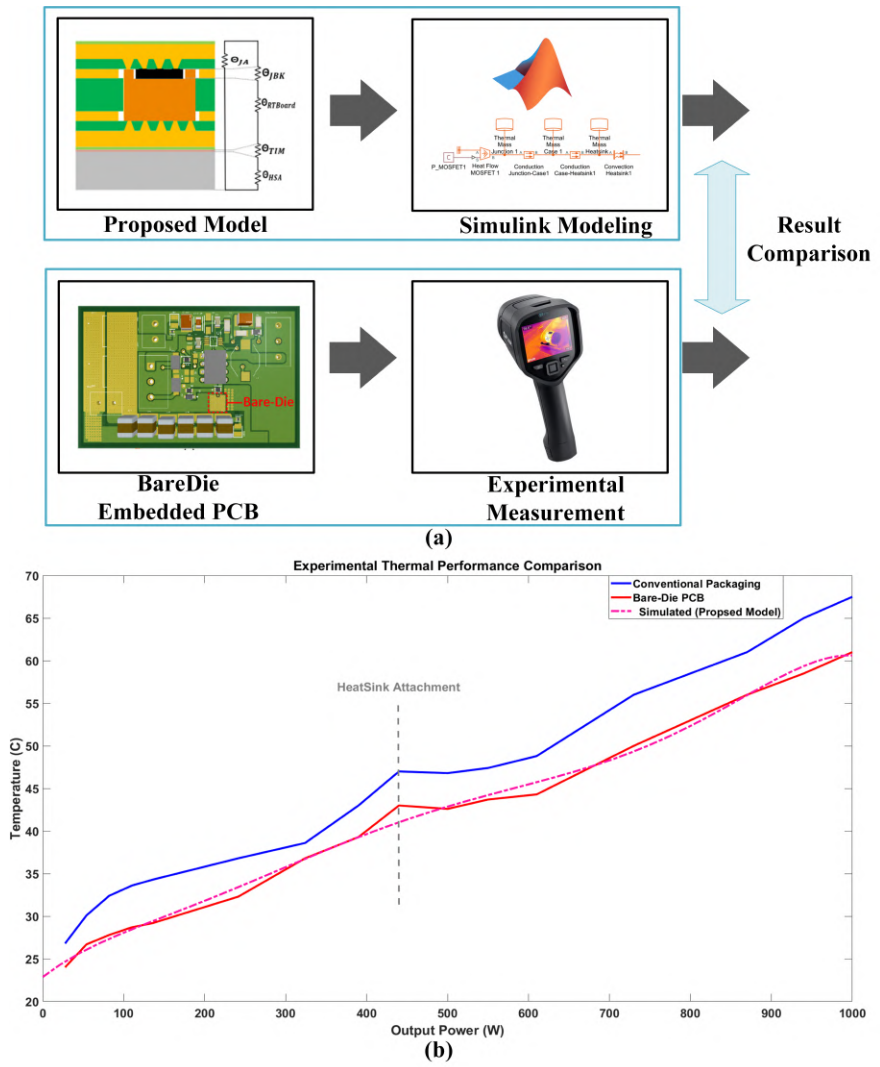


Figure 3.8: (a) Methodology of Thermal Validation (b) Experimental Thermal Performance Comparison

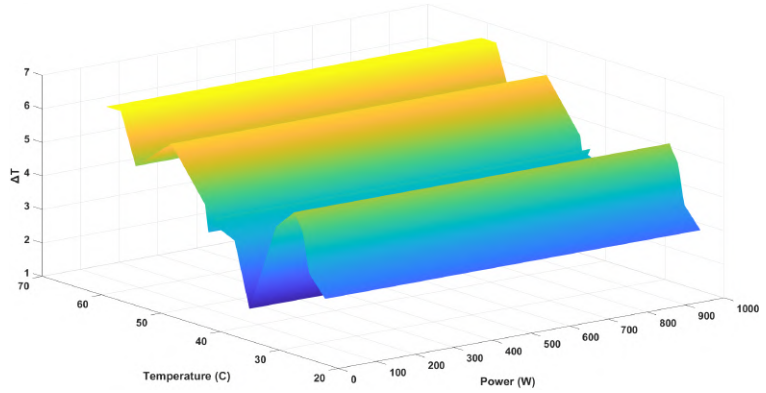


Figure 3.9: Surface Plot- Thermal Performance

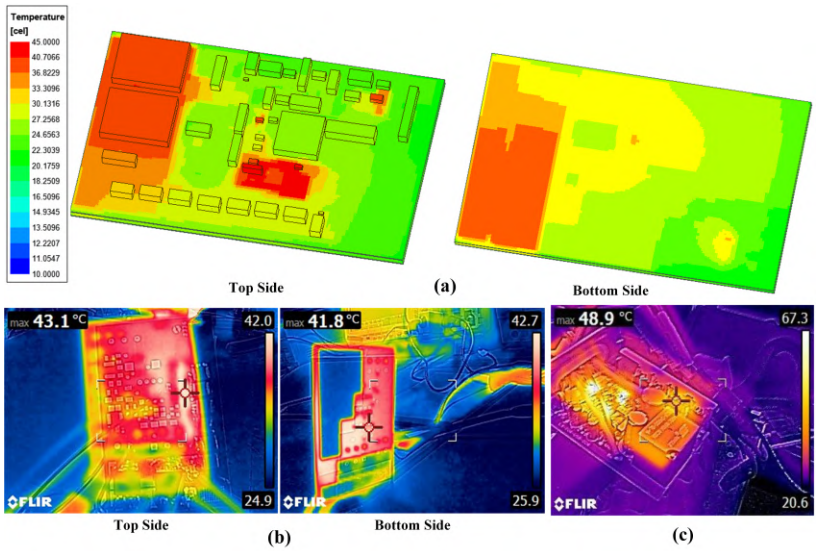


Figure 3.10: (a) ANSYS-ICEPAK Thermal Analysis of Bare-Die Embedded PCB at 600W(b) Experimental Thermal Image of Benchmark Motor Drive at 600W - Top and Bottom side (b) Experimental Thermal Image of Bare-Die Embedded PCB Motor Drive at 600W - Top and Bottom side (c) Benchmarked/Conventional Motor Drive PCB Thermal Image

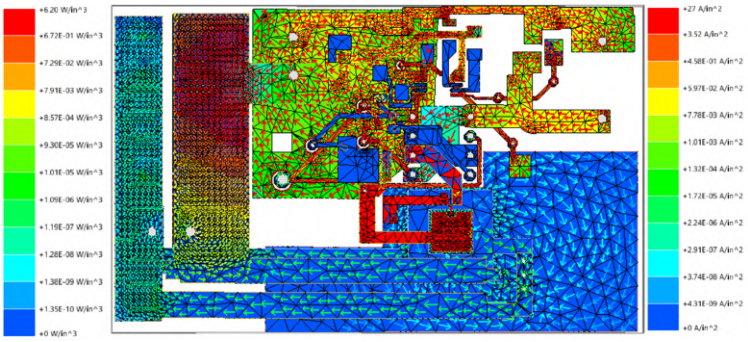


Figure 3.11: Power Distribution and Current Density Analysis-ANSYS-SiWave

An improved parasitic performance is another major goal of this research study. By using the bae-die instead of the packaged die, the R_{DS} of the MOSFET is reduced significantly. As in this case, the bare-die used is IAUE303N085N000 whose $R_{DS(on)}$ is $0.8m\Omega$,$V_{DS} = 80V$ and continuous drain current capability of $460A$ with a die size of $30.25mm^2$ and $100\mu m$ thickness. Compared to the benchmarked E-Scooter motor drive that uses the T-220 package MOSFET(CS55N53) whose $R_{DS(on)}$ is $6.4m\Omega$, and only $100A$ of current carrying capability due to the constraints associated with the traditional packaging. The modern packages such as PD-HDSOP-16-2 (IAU300N08S5N012), which are considered the best available in the market so far with a V_{DS} of $80V$ have an $R_{DS(on)}$ of $1.2m\Omega$ and a current carrying capability of 300A, which when compared to the proposed bare die technique it offers an improvement of 50% in terms of the $R_{DS(on)}$ and 30% in the current carrying capability, which opens up new possibilities for such rated packages to be used in low voltage and high current applications [136]-[137]. This property of high current capability also reduces the number of components required to divide the current stress and voltage drop.

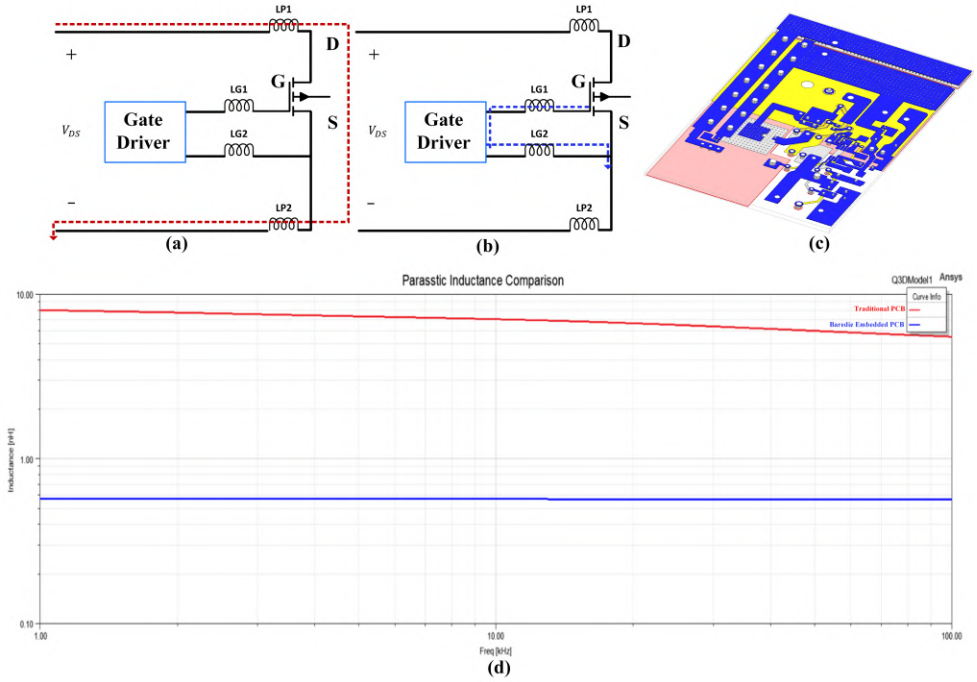


Figure 3.12: (a) Power Loop Parasitic Inductance (b) Gate Driver Loop Parasitic Inductance (c) ANSYS-Q3D Model of BareDie Embedded PCB (d)Parasitic Inductance Comparison

Figure 3.12a and 3.12b shows the parasitic inductance schematics of a DC motor drive MOSFET. L_{p1} and L_{p2} are the respective power loop inductances and L_{G1} and L_{G2} are the gate loop inductance. The designed bare-die embedded PCB was modeled in the ANSYS-Q3D simulation tool as shown in Fig 3.12c to extract the parasitic parameters and induc-

tances. Table 3.3 presents a comparison between the benchmark motor drive PCB using a TO-220 device and the designed motor drive PCB having an embedded bare-die power device. It can be clearly seen that due to the vertical direct connections possible through laser drill vias to the gate of the bare die, the gate parasitics have been improved by 74%, as depicted in Fig 3.12d.

Table 3.3.Parasitic Performance Comparison of Proposed Bare-Die Technique and Conventional Benchmarked Discreet Packaging

	V_{DS} **(V)**	I_{Dmax} **(A)**	$Inductance$ **(nH)**	R_{DSon} **(mΩ)**
Benchmarked Motor Drive	80	100	1.96	6.4
BareDie Embedded Technique	80	460	0.56	0.8

3.1.4 Experimental Results and Analysis

To evaluate the effectiveness of the proposed technique, the designed bare-die embedded motor drive was tested and compared with a benchmark e-scooter motor drive from the market. The bare-die embedded motor drive was designed with the same power level and circuit topology for a fair comparison. Apart from the demonstrated thermal and parasitic benefits offered by the proposed technique, which are discussed in the previous sections, the increase in the power density was a major goal for this research work. The manufactured bare-die embedded motor drive is shown in Fig 3.13a and Fig 3.13b, having dimensions of $(2.87L \times 1.77W \times 0.7H)$ inches, including the attached cold plate to the bottom layer, which compared to the benchmarked motor drive is an increase of 113% in the power density as depicted in the Fig 3.14b which shows the power density comparison.

Due to such significant improvement in the power density, the motor drive can now be easily integrated into a single case with the planar transformer design-based onboard charger; the design of the onboard charger is out of scope for this paper. The bare-die embedded motor drive, and the OBC are now incorporated into the case, having similar dimensions previously occupied by the benchmark motor drive as shown in Fig14a, solving the challenge of lack of onboard changing capabilities for small mobility vehicles.

The bare die technique is expected to have better efficiency than the benchmarked motor drive using discreet packaging, as the bare die has low parasitic associated with its packaging, resulting in low power losses. An efficiency comparison at different load conditions between the designed bare-die motor drive and the benchmarked motor drive is presented in Fig 15a, where it can be concluded that the proposed technique has higher efficiency. To

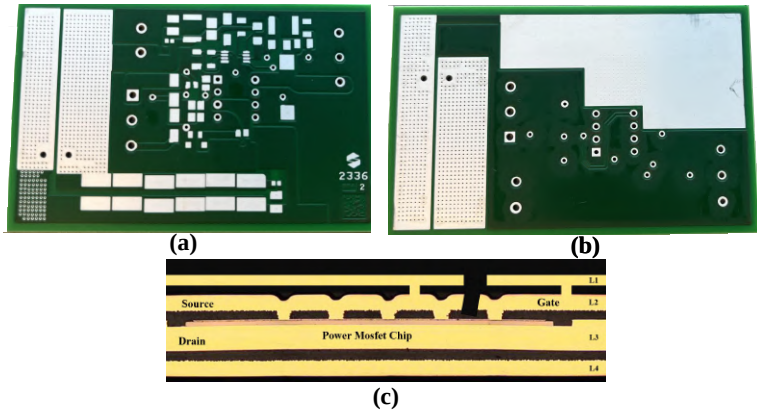


Figure 3.13: Manufactured BareDie Embedded Motor Drive PCB(a) Top View(b) Bottom View(c) Cross-Sectional View - adapted from [131] with permission from Wiley and Sons, Copy right (2019)

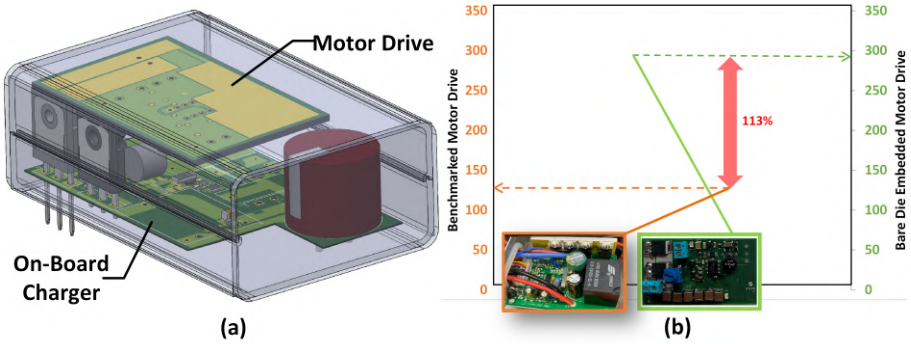


Figure 3.14: (a) Developed Integrated Module Containing Motor Drive and OBC (b) Power Density Comparison

better represent and understand the relation between the efficiency, load, and change in the efficiency, a surface 3D plot is presented in Fig 3.15b. The experimental setup used for all the experimental results is shown in Fig15c. The waveforms of the designed DC motor drive are shown in Fig 15d. The benefits of the proposed bare-die embedded technique can be

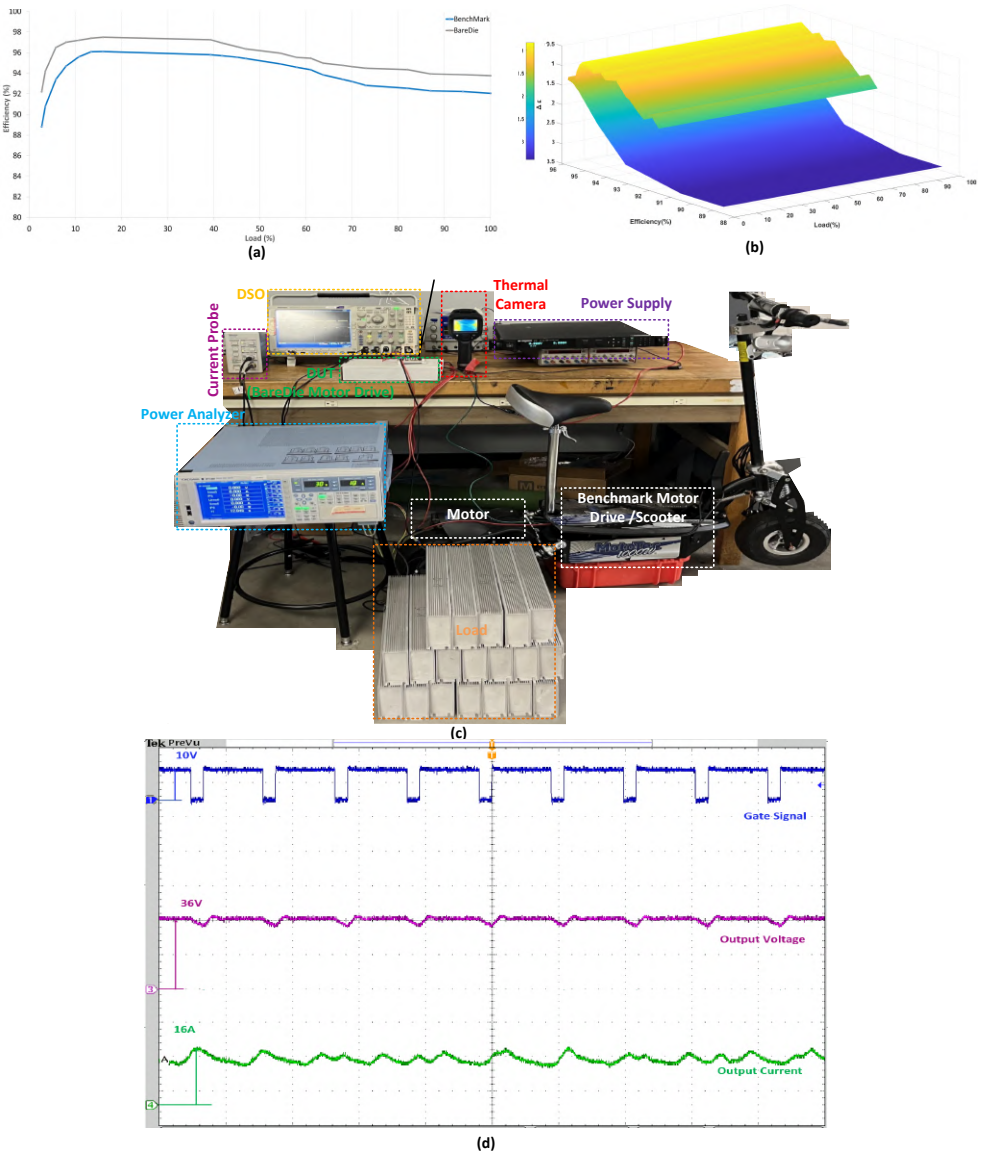


Figure 3.15: (a) Experimental Efficiency Comparison (b) Efficiency Surface Graph (c) Experimental Setup (d) Experimental Waveforms

analyzed from two perspectives, i.e., the development of the integrated module resulted in the onboard charging capability for small mobility vehicles, and from another perspective, the space saved due to the high power density offered by the bare-die embedded technique, the battery pack can be extended which will extend the driving range of the vehicle reducing

the range anxiety.

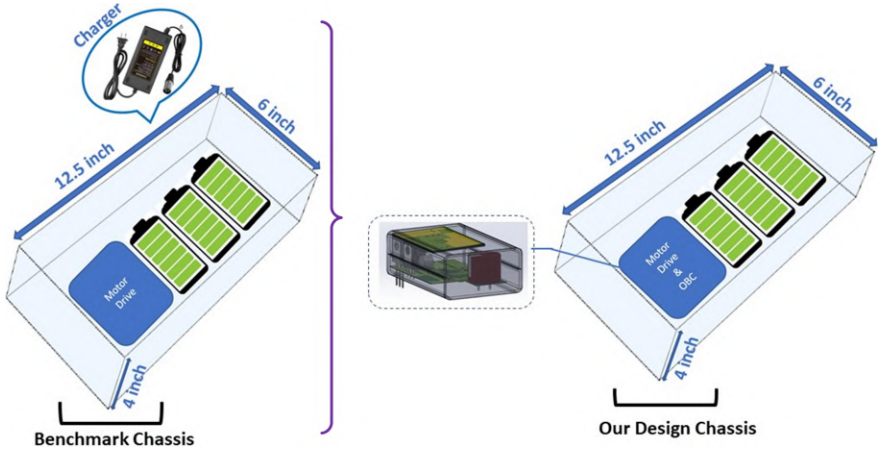


Figure 3.16: Off Board to On Board Conversion with Integrated Motor Drive

3.1.4.1 Perspective 1

The small mobility vehicles come with an offboard charger, which is a disadvantage. So, due to the high power density achieved through the bare-die embedded technique, an integrated module containing both the motor drive and OBC can be placed into the chassis of the vehicle, which offers an onboard charging capability to the small mobility vehicle. The aluminum casing that previously in the benchmark vehicle only contained a motor drive now incorporates both the motor drive and OBC without any increase in the chassis dimension, as shown in Fig 3.16.

3.1.4.2 Perspective 2

From another perspective, the space saved by adopting the high power density bare-die embedded technique can be used to extend the battery pack shown in Fig 17a, which will increase the vehicle's driving range and solve the challenge of range anxiety. In this case, the driving range was increased by16%. The improvement in the driving range is shown in Fig 17b.

This research presented a bare die embedded packaging technique, along with the design rules, methodology, and manufacturing framework, which proved the superior performance and advantages. A thermal model for the proposed technique was presented and validated, along with the experimental results. A motor drive was designed using the proposed technique and compared with the benchmark motor drive to justify better performance in terms of high power density, better thermal performance, low parasitics, higher efficiency, increased

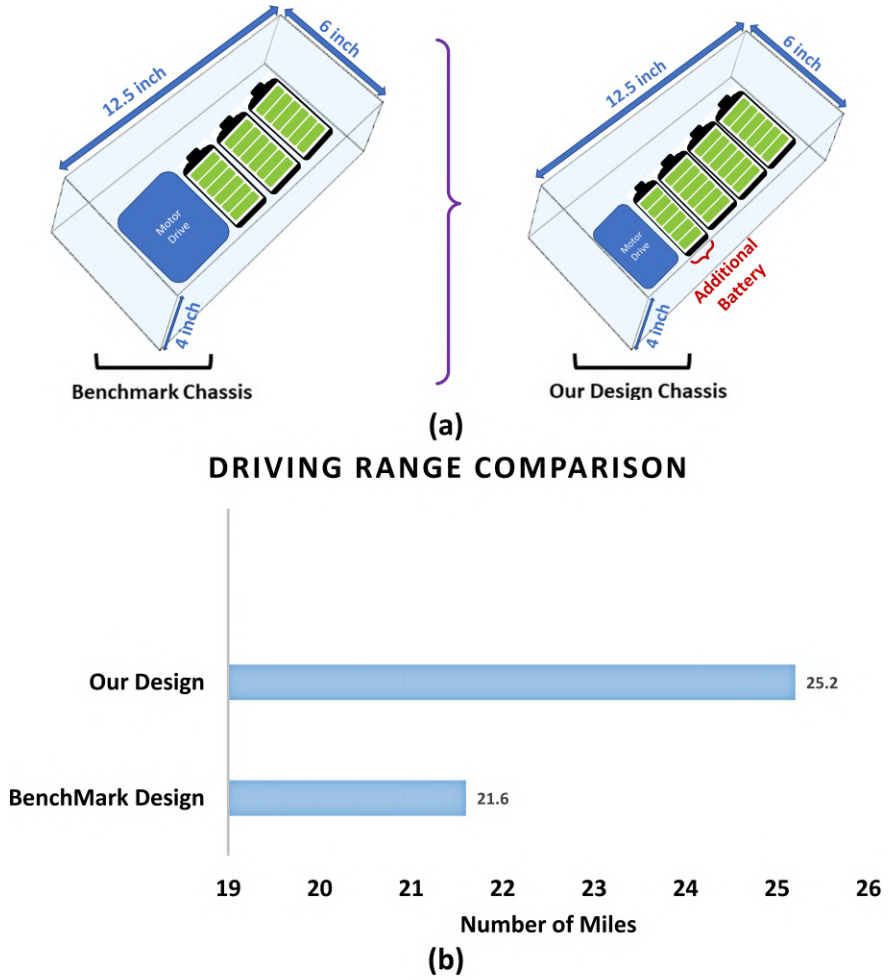


Figure 3.17: (a) Battery Pack Extension (b) Driving Range Extension

depth of integration, and extended driving range. Parasitic extraction, signal integrity analysis, and experimental comparison were done to illustrate the performance of the proposed technique. This work is the foundation to illustrate the potential of the newly proposed bare-die embedding technique, whose applications can be extended beyond small mobility and to high power level applications to accelerate the electrification revolution.

3.2 Bare-Die Embedded PCB Technique: An EMI Perspective

3.2.1 Introduction

The key goals in developing power electronics converters for today's demanding applications and industry are achieving high power density, high efficiency, and low cost. However, as power electronics become more integrated and closely packaged, they become more susceptible to the disruptive effects of electromagnetic interference (EMI), which is a challenge for embedded and integrated designs. This research focuses on the signal integrity and EMI performance evaluation of a new bare-die embedded PCB packaging technology, ensuring a very compact, high power density, and integrated design for the power electronics unit. The design incorporates the bare die of the switching devices into the PCB layers and uses multilayers for routing and cooling purposes. A Silicon (Si) MOSFET bare-die is embedded into the FR4 layers using the stomach cell approach, electrically connected, and cooled through laser-drilled micro vias and copper fills. The electrothermal codesign reduces the parasitic loop inductance by 74% and increases the power density by 113%. This research, through analysis and experimental results, evaluates the signal integrity and EMI performance, including conductive emissions, radiated emissions, insertion loss, reflective loss, cross talk, and susceptibility analysis, according to industry standards (CISPR25) to establish the superior performance of the proposed bare-die embedding technique through a benchmark comparison with the traditional PCB design. To the best of the author's knowledge, this is the first paper to explore the EMI perspective on a system level for bare-die or active components embedded PCB design.

advancements in semiconductors and packaging technologies have led to the emergence of high-speed switching transistors that ensure high efficiency from KHz to MHz range. Power electronics, which is a key enabling technology for modern applications, necessitate advancement and exploration on the packaging side along with the semiconductor devices, control, and new topologies [138]. Today's power electronic systems aim for high power density, maximum efficiency, and low-profile packaging to meet the demand for modern

electric vehicles (EV), aerospace, and energy systems applications [139, 140, 141]. The wide-bandgap (WBG) materials have enabled high speed and high voltage operation while offering low on-state resistance and compact design freedom. However, these characteristics come with their own set of challenges, particularly regarding electromagnetic interference (EMI) and electromagnetic compatibility (EMC) [142, 143, 144, 145, 146]. Moreover, the incorporated advanced cooling approaches, integrated passive devices, and 3D packaging increase circuit complexity and adversely affect the EMI performance[147]. Various standards such as CISPR 25, CISPR 32, DO-160, and MIL-STG-461G are being adopted globally to regulate EMI/EMC levels[148, 149]. The literature presents multiple methods, such as EMI filtering, EMI shielding, soft switching, random modulation, chaotic PWM control, etc., to reduce EMI and pass the required EMC standards[150]. However, the scope of this research is to determine the impact of bare-die embedded PCB technique on EMI performance.

Active components are the ones switching at high frequencies and are the dominant source of EMI emissions due to the increased switching noise harmonics at high frequencies. The integration or embedding of these active switches (such as MOSFETs) within the PCB layers, switching at higher frequencies proposed in this research, offers significant benefits in terms of power density and low parasitic inductance, but the EMI impact of such an approach is unknown and is explored in this research.

The need to embed the bare die of the switching devices into the PCB arises from the fact that magnetic components are no longer bottlenecks in high-power density design due to the high switching frequency enabled WBG devices, which significantly reduce the size of passive components [151]. Hence, the challenge at hand is the size and packaging of the switching devices themselves. In literature, multiple packaging techniques can be found; however, most of them use bond wires, which are a source of parasitic, for the connections between the power component and substrate. The drawback of the high switching frequency operation is the increased switching losses; therefore, reducing the parasitic at the lowest level in packaging is essential to harvest the true benefits of high switching frequency and achieve low power loss, better thermal performance, and increased system efficiency[152, 153, 154]. The detailed literature review and design comparison of the proposed bare-die embedded technique is given in [] by the authors, which is focused on the design and performance of the proposed technique.

In this research, a detailed signal integrity and EMC analysis, including radiated emissions, conductive emissions, and electromagnetic susceptibility (EMS) analysis, of the newly proposed bare-die embedded PCB technique is conducted to prove the superior EMC performance of the die-embedding approach. This research contribution helped identify the previously unexplored superior EMC performance benefit of the chip embedding approach,

which sets a foundation for its adaption and advancing power electronics packaging technology. The paper is organized as follows:

The introduction section provides an in-depth overview of the problem statement to highlight the significance and need for this research, aided by the literature survey, and presents a comparative analysis of the existing techniques. Section II provides insights into the bare-die embedding technology from the footprint construction to the embedded PCB design. Section III focuses on the analysis, mathematical background, and tests that are required to validate the EMC performance. The Results and Analysis section provides an overview of the hardware setup and simulation environment and analyses the results obtained to translate them into the performance explanation with the help of pre-compliance experimental results.

3.2.2 Signal Integrity and EMC Analysis

Signal Integrity (SI) and Electromagnetic Compatibility (EMC) modeling are essential to design optimized high-speed electronics, especially in power electronics-based systems. SI analysis determines the signal quality throughout the system in terms of losses, interference, or timing errors, which can be assessed by modeling the impedance, cross talks, and noise. The S-parameter extracting and time domain reflectometry technique is used in this research for the determination of the SI analysis. The S parameter sweep technique helps to analyze both the time and frequency domains. The time domain evaluates the transient behavior, while the frequency domain evaluates the steady state and resonance effects.

EMC modeling and analysis are essential to determine whether the designed system can operate within the standardized EMI limits and is immune to disturbances from its surroundings. EMC analysis can be classified into electromagnetic interference (EMI) and electromagnetic susceptibility (EMS) analysis. EMI is further classified into conductive emissions and radiated emissions as shown in Fig.3.18.

Conducted EMI is the noise that propagates through physical connections like wires, connectors etc., while the radiated EMI is the emissions in the free space. Conducted EMI can be simulated by circuit-based tools such as LTspice, which is used in this research. However, an electromagnetic solver, such as ANSYS in this research, is required for radiated EMI. Moreover, in this research, the electromagnetic solver is coupled with the circuit solver to improve the accuracy of determining the conducted EMI. The EMC analysis of the proposed bare-die embedded PCB technique is done and the performance is compared with a traditional PCB design using discrete MOSFET.In contrast to the benchmarked E-Scooter motor drive, which employs the T-220 package MOSFET (CS55N53), which has an RDS (on) of

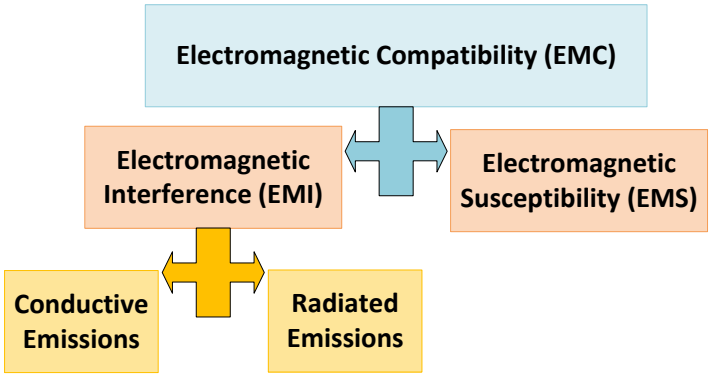


Figure 3.18: EMC Classification

6.4m and a current carrying capacity of only 100A because of the limitations of the conventional packaging. When compared to the suggested bare die technique, the modern packages like PD-HDSOP-16-2 (IAU300N08S5N012), which are thought to be the best on the market at this time with a VD S of 80V, offer an improvement of 50% in terms of $RDS(on)$ and 30% in terms of current carrying capability. This creates new opportunities for such rated packages to be used in low-voltage and high-current applications [155, 156]. Figure 3.12 shows the power stage schematics of the DC motor drive in consideration. L_{p1} and L_{p2} are the respective power loop inductances and L_{G1} and L_{G2} are the gate loop inductance.Extraction of the parasitic is essential before moving onwards to the EMC analysis stage. The parasitic extraction of the proposed bare-die embedded design and traditional design was done in ANSYS-Q3D; the summary of the extracted parameters is shown in Table 3.1.3 where it can be observed that the gate loop parasitic are reduced by 74% as the bare-die embedded PCB resulted in 0.56nH of gate loop inductance as compared to 1.96nH for the traditional PCB design.

Signal Integrity (SI) and Power Integrity (PI) analysis is the way forward toward an optimized design and EMC performance evaluation. The signal integrity analysis helps identify the hotspots for power dissipation and current density, using which the layout can modified to obtain an acceptable and optimized design with the goal of equal power dissipation pattern and to avoid current saturation at a single point in the design. The power, current, voltage density, and distribution analysis were performed as shown in Fig.3.19.

3.2.2.1 Signal Integrity Analysis

Signal integrity analysis and comparison are essential as they gauge the integrity of signals transmitted through interconnects, traces, cables, etc. It also identifies signal degradation or

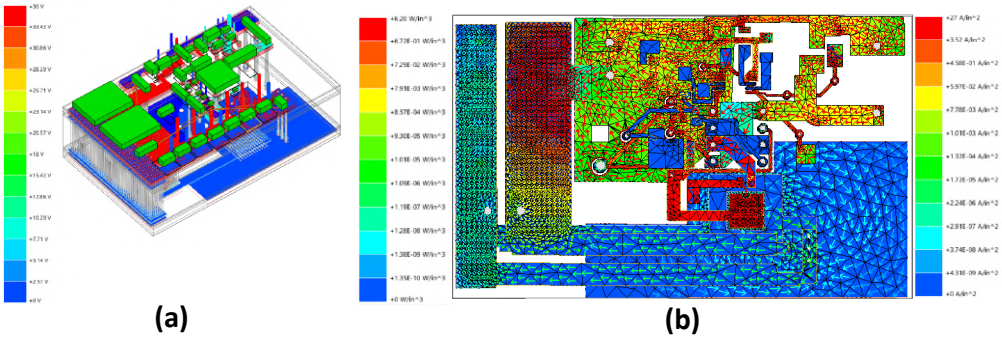


Figure 3.19: (a) Bare-Die Design Signal Integrity Model(b) Power Distribution and Current Density Analysis

distortion due to insertion loss, reflective loss, and cross-talk. In this research, the insertion loss was quantified by simulating the S-parameters of the design to identify the frequency-dependent losses. Insertion loss can also be understood as the ratio of the incident power to transmitted power. High insertion loss causes the transmission signal to be too weak for active equipment interpretation. Return loss refers to the signal power loss due to reflection or discontinuity in the line. A high return loss is favorable, and it correlates to a low insertion loss. Figure 3.20 shows the insertion and return loss comparison for the proposed bare-die embedded design and the traditional design for the crucial traces. It can be concluded that the bare-die embedded PCB design offers low insertion loss; most of the nets are around zero or converging to zero, and the maximum loss peak is at 2.5dB, while the traditional design has a very high and non-desirable insertion loss with the peaks reaching up to 25dB. All the traces are not close to the zero line. Similarly, the return loss for the bare-die embedded design is high (which is desirable), and most of the traces range from 50 to 100dB marks. However, for the traditional design, a poor return loss pattern is recorded where most traces are near the zero line, and the maximum peak is at 22dB, which will negatively impact the system and signal integrity performance.

Cross talk can be understood as the coupling between the adjacent traces or lines that leads to signal interference. Cross talk is of great concern in high-power density PCBs with closely packed traces. The cross-talk behavior is simulated by electromagnetic field solvers such as ANSYS-SiWave by modeling the coupling effects and identifying potential issues near the design phase to ensure EMC compliance. Figure 3.20e and 3.20f shows a cross-talk comparison of the bare-die embedded design and the traditional design, where it can be seen that the traditional design experiences 36% higher cross-talk magnitude than the bare-die embedded design.

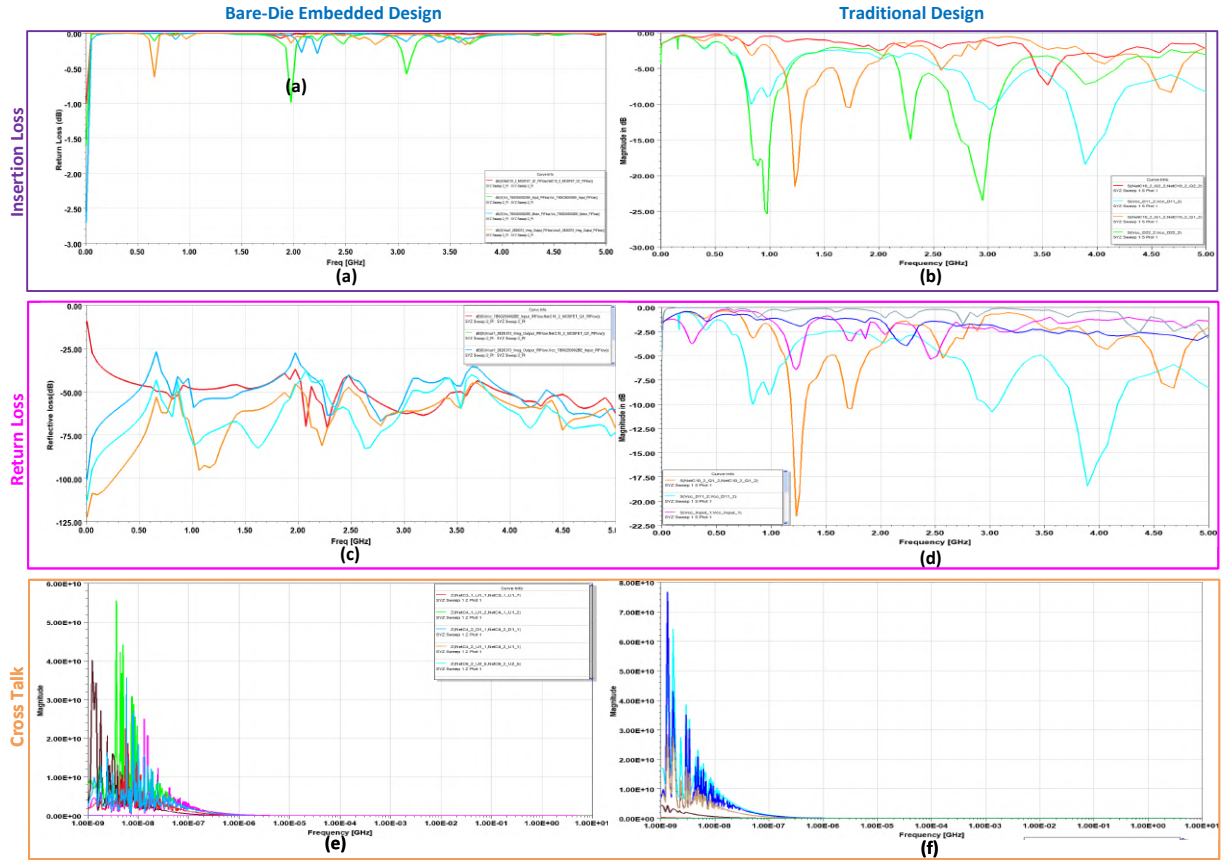


Figure 3.20: Bare-Die Design (a) Insertion Loss (c) Return Loss (e) Cross Talk Traditional Design (b) Insertion Loss (d)Return Loss (f) Cross Talk

3.2.2.2 Electromagnetic Susceptibility Analysis (EMS)

A voltage-induced test can analyse the design's susceptibility to external electromagnetic fields. It evaluates the effect of induced voltages and external field disturbances on the design regarding performance, safety, and EMC compliance. EMS analysis is crucial for high-reliability applications such as automotive, aerospace, and other industrial electronics where the environment contains electromagnetic disturbances. This analysis focuses on quantifying the voltage induced in critical areas of the design, such as signal traces, power traces, etc. This analysis considers the field interactions and coupling mechanisms, including material properties, frequency dependency and design geometry. The EMS analysis is of significant importance as it potential failure areas or performance degradation caused by induced voltages, which can lead to circuit malfunction and permanent component damage.

Moreover, it ensures the product's compliance with EMC standards. Figures 3.22a and 3.22b present the EMS analysis of the bare-die embedded PCB and the traditional PCB, respectively in terms of insertion loss, return loss and cross talk. The analysis identifies the

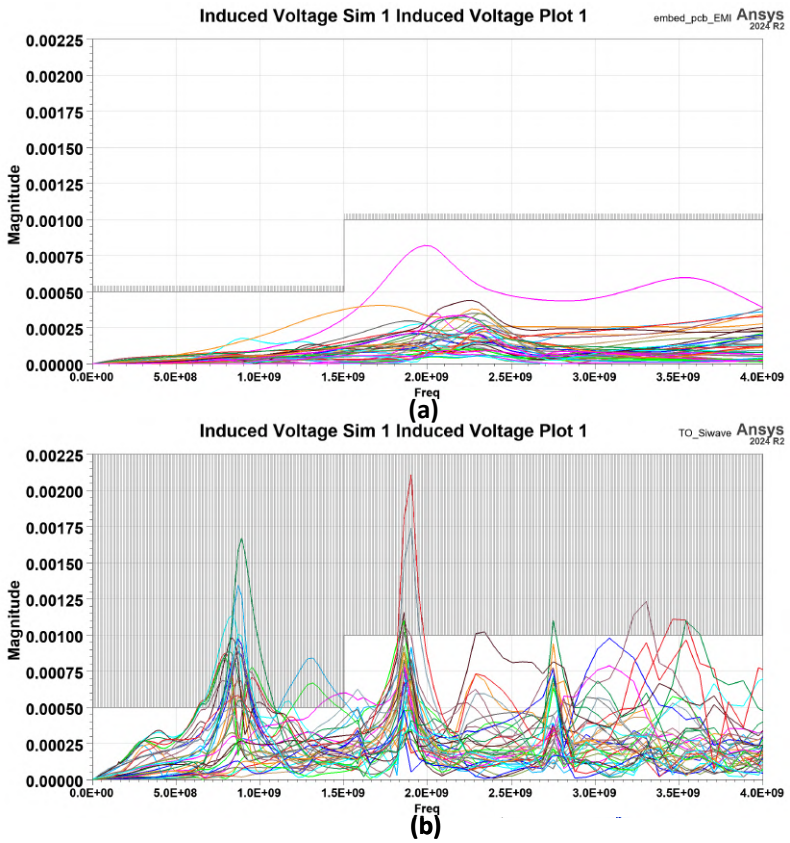


Figure 3.21: Electromagnetic Susceptibility Analysis (a) Bare-Die Embedded Design (b) Traditional Design

effect of induced voltage on the selected and critical nets in the design. It can be observed that the proposed bare-die embedded PCB performs much better as its traces have a low magnitude overshoot compared to the traditional one. A limit line on the $4Mhz$frequency range helps to understand better and quantify behaviour, as the overshoots in the proposed design stay below the reference limit line compared to the overshoot in the traditional design, which results in a greyed region when the trace crosses the limit line. This analysis establishes that the bare-die embedding technique proves useful and performs better than the traditional PCB design approach, making the design more susceptible to external electromagnetic disturbance and preserving performance, safety, and EMC compliance.

3.2.2.3 Electromagnetic Interference(EMI) Analysis-Radiated Emissions

Radiated emission is the mid-to-high frequency noise produced by a device while operating under normal conditions and can interfere with nearby devices; therefore, it must comply with regulatory standards. The analysis in this research compares both the near and far field

radiated emissions through detailed and standard simulations to evaluate the performance of the proposed and traditional design. Near filed region is the one located close to the PCB or emitting source and is dominated by reactive field and provides insights into the local coupling between the components. In this analysis, the near field region is the standard 3mm distance from the board on all sides. The far-field region is located at a distance of 1 meter in this analysis, where the wavefronts behave like plane waves. Figure 3.22a and 3.22b shows the nearfield comparison of the bare-die embedded design and the traditional design respectively, which depicts that the bare-die design emits less radiations in both electric field (E-field) and magnetic field (H-field) perspective.

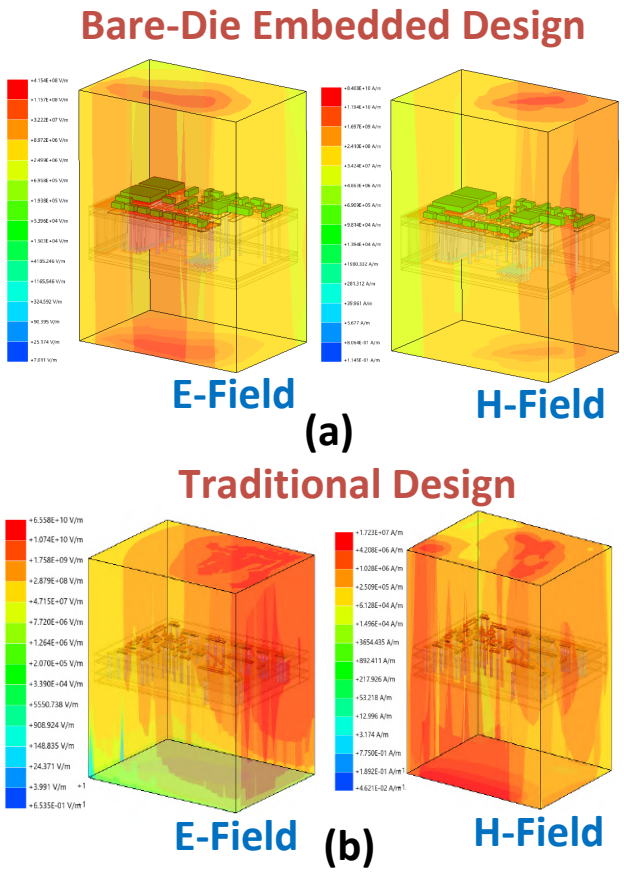


Figure 3.22: Near-Field Analysis (a) Bare-Die Embedded Design (b) Traditional Design

Similarly, the far-field analysis and comparison are shown in fig 3.23 where graph of the maximum total energy in the far-field region is shown in Fig.3.23 a and Fig.3.23 b for the bare-die and traditional design respectively, which shows that the magnitude of radiations in the traditional design are higher compared to the proposed bare-die design, which makes the proposed technique more suitable for developing high power density and integrated products

that ensure EMC compliance in harsh environment. The same is also shown in a 3D plot in Fig.3.23 c and Fig.3.23 d where it can be seen that the bare-de design ensures more symmetrical behavior with less intense emissions compared to its counterpart, which makes it a superior choice for high power density and complex designs.

3.2.2.4 Electromagnetic Interference(EMI) Analysis-Conductive Emissions

Conductive emissions are the EMI transmitted through a conductive path, such as power or signal lines, which can lead to system degradation, failure, and EMC non-compliance. These emissions can be generated due to various reasons, such as high-frequency switching of devices, voltage and current ripples, etc. In this research the CISPR25 standard is used to analyse and test the conductive EMI. The conductive emissions workflow is presented in Fig.3.24a, which depicts different stages and analyses needed to evaluate the conductive emissions. Following the signal integrity analysis of the design, its parasitics are extracted in ANSYS-Q3D, and those parasitics are modeled in the system-level simulation that needs to be carried out to obtain the conductive emissions. This research designed the required line impedance stabilization network (LISN) according to the adopted CISPR 25 standard specification. The constructed setup for conductive emissions in LTSPICE is shown in Fig.3.24b; the hardware setup will be discussed in the experimental section of this paper.

Figure 3.25a shows the obtained total noise of the proposed bare-die embedded PCB design at the 4Mhz range on the x-axis, while the magnitude in μdB on y-axis. However, total noise is not enough to determine the causes and mitigation of noise, so it needs to be split into common mode (CM) and differential mode (DM) noise as shown in Fig.3.25b. Compared with the traditional PCB conductive emissions presented in Fig 3.25c and 3.25d, the emissions peaks are higher both on the upper and lower side, especially from the start to the center frequency range, which establishes the superior performance of the bare-de embedding technique.

3.2.3 EMC Experimental Results and Analysis

The designed bare-die embedded motor drive was tested on and compared with a benchmarked electric scooter drive from the market as shown in Fig.3.26a. The motor drive is rated at 1KW with a battery voltage of 36V. Significant benefits in power density, efficiency, and thermal performance were observed. However, this paper is focused on exploring the benefits in the EMC/EMI performance for which a pre-compliance setup was built to evaluate the conductive emissions, as shown in fig.fig:fig3.26b.

For the experimental setup of conductive emissions, according to the CISPR 25 standards,

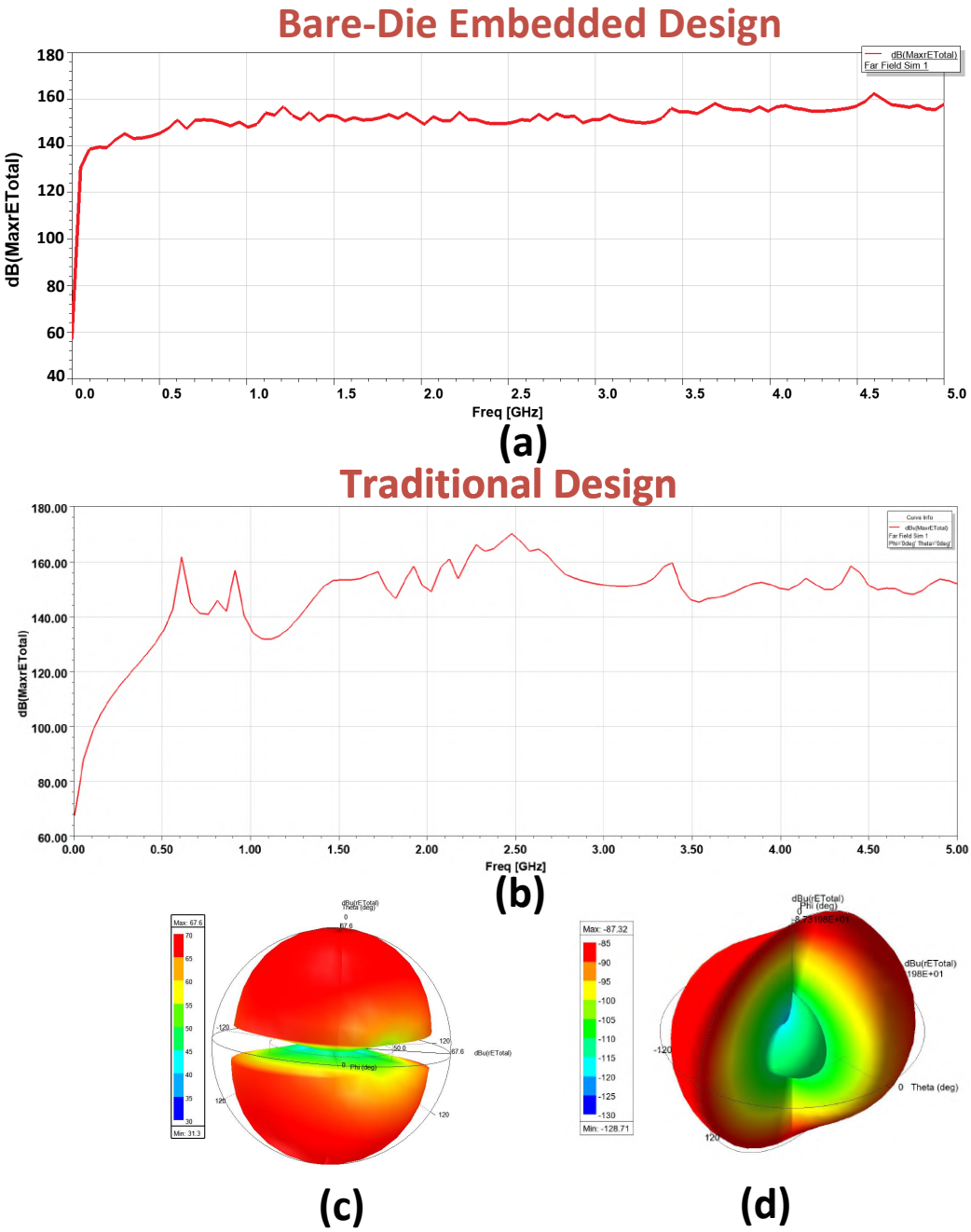


Figure 3.23: Far-Field Analysis Rectangular Plot (a) Bare-Die Embedded Design (b) Traditional Design, Far-Field Analysis 3D Plot (c) Bare-Die Embedded Design (d) Traditional Design

LISN TBOH01 from tekbox was used, which has the impedance of $5\mu H/50\Omega$ and a frequency range of $150KHzto108MHz$. A sepeate LISN was used for both positive and negative supply wire and a LISN mate(TBLM2) was used to split and record the CM and DM noise from

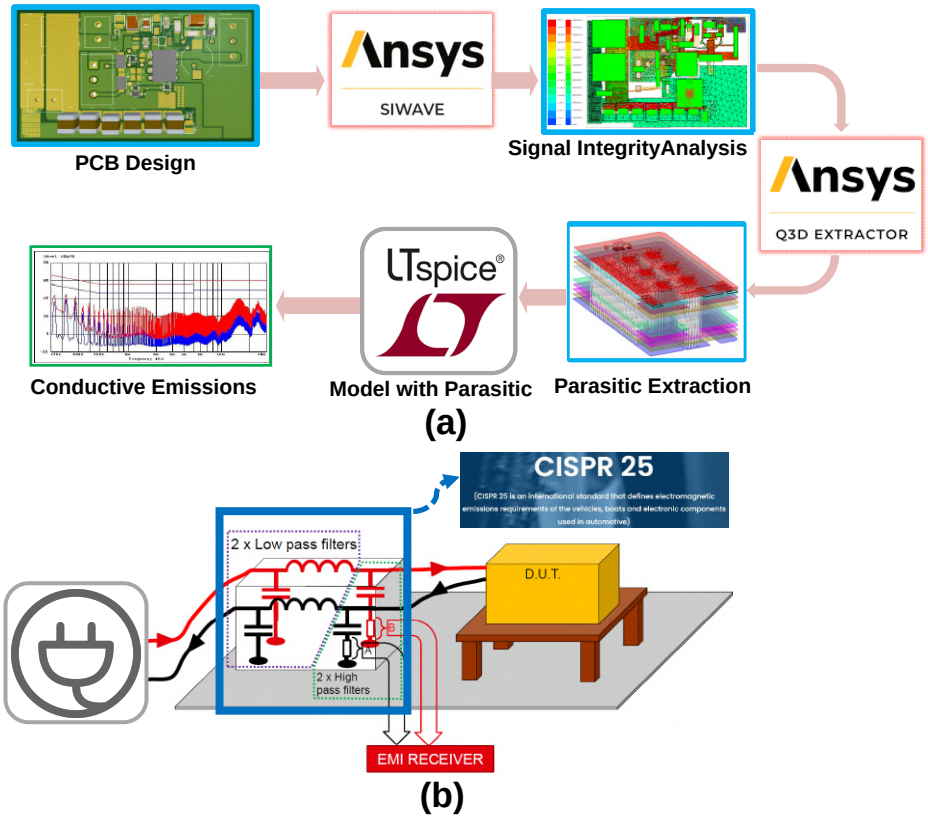


Figure 3.24: (a) Conductive Emissions Workflow (b) Conductive Emission Setup-LTSpice

the total noise as shown in Fig.3.26c from TekBox. Fig3.27 shows the total noise comparison of the traditional PCB and the bare-die embedded PCB, which has a frequency range of 4MHz on the x-axis and magnitude in (μdB on the y-axis. It can be observed that there is a significant difference, and the traditional PCB design has more noise peaks before and after the center frequency. For better understanding, the DM and CM noise comparison is presented in Fig.3.27c,d and Fig.3.27e,f respectively. The performance difference is more clear in this comparison as the traditional design results in significant magnitude noise peaks as compared to the bare-die design, which has fewer noise peaks for both CM and DM noise under the same ambient noise and operating conditions. These experimental results shows that the bare-die PCB embedding design offers significant advantages from an EMC/EMI perspective, making it vital for developing high power density and integrated designs.

This research presented a unique perspective and benefit of the newly proposed bare die embedded packaging technique and established its superior performance through signal integrity analysis, electromagnetic susceptibility analysis, and EMI analysis aided by experimental results and compared with traditional PCB design. A motor drive was designed using the proposed technique, and its EMC performance was compared with that of the bench-

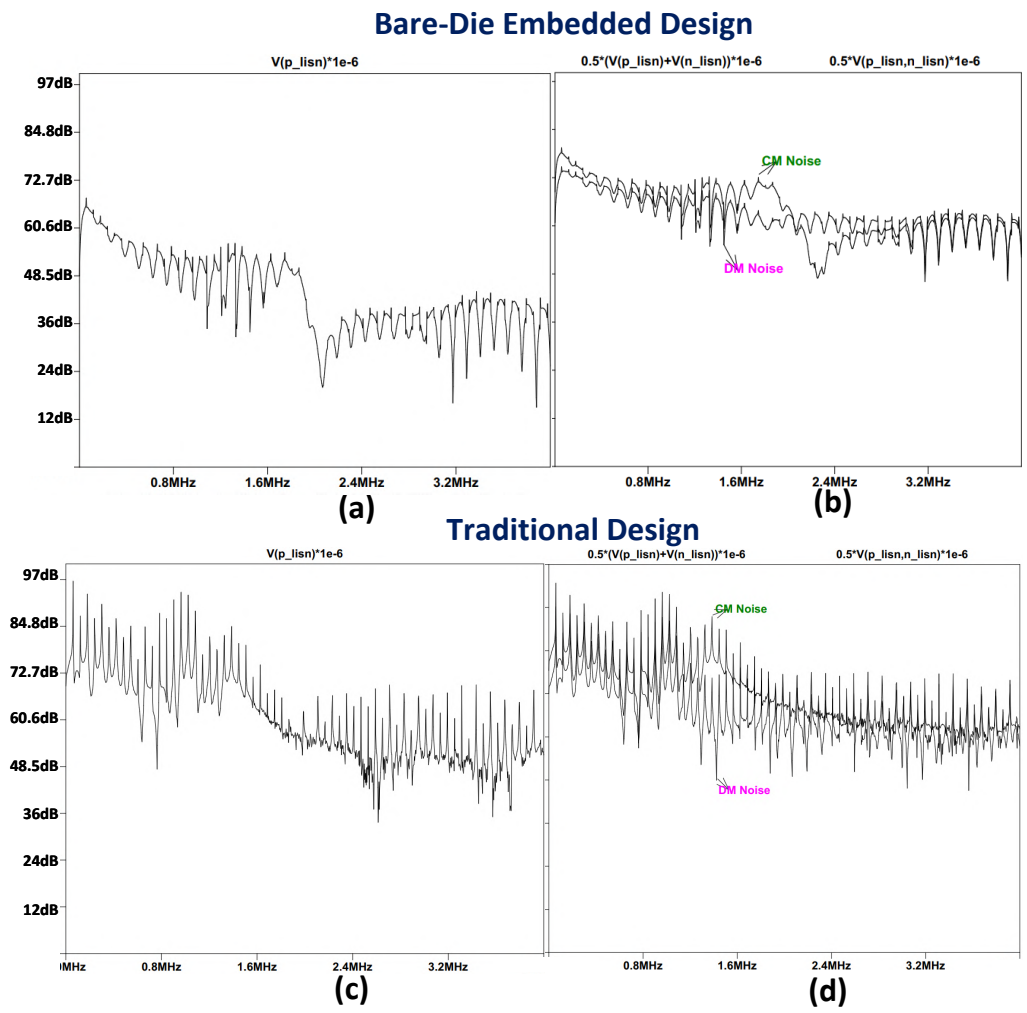
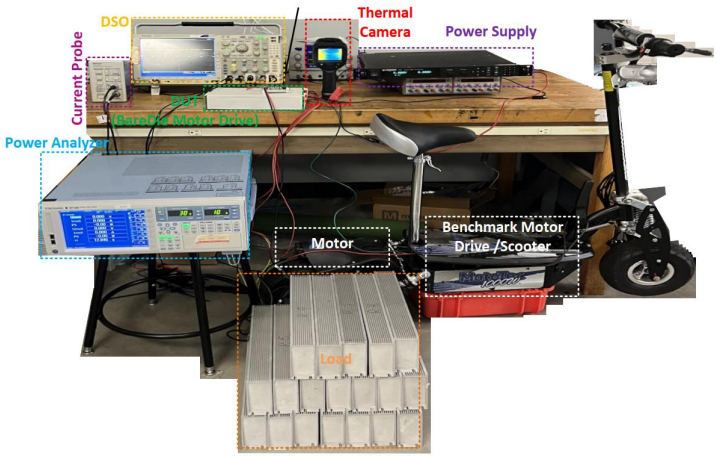
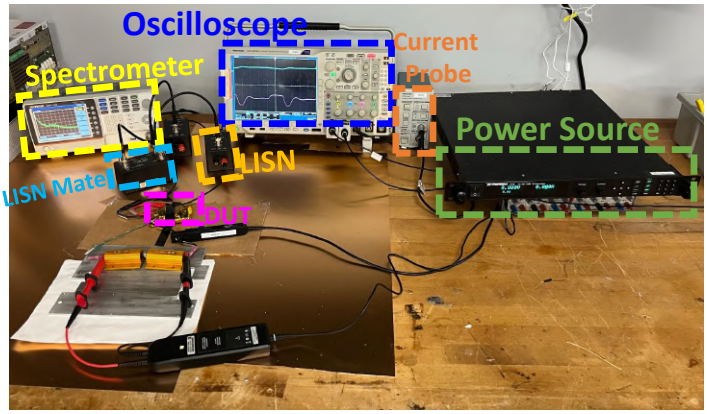


Figure 3.25: (a)Total Noise-Bare-Die Design (b) CM and DM Noise-Bare-Die Design

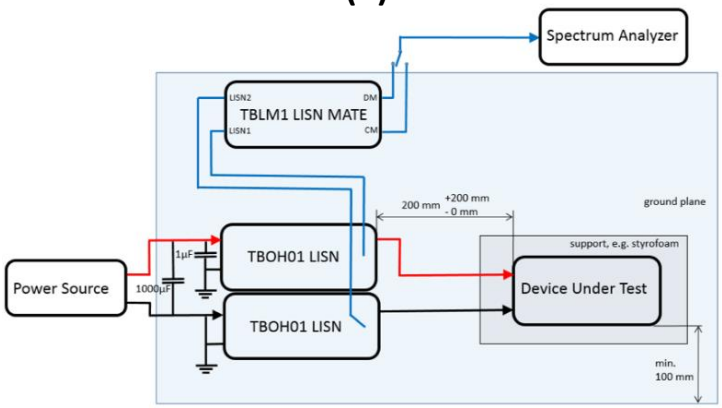
mark motor drive to justify better performance. This work is the foundation to illustrate the potential of the newly proposed bare-die embedding technique and discover its benefits from the EMC/EMI perspective, which will pave the way for its widespread adaptions to accelerate the electrification revolution.



(a)



(b)



(c)

Figure 3.26: Experimental Setup(a) Motor Drive Operation (b) Conductive EMI (c) LISN Connection Setup [from TekBox Datasheet]

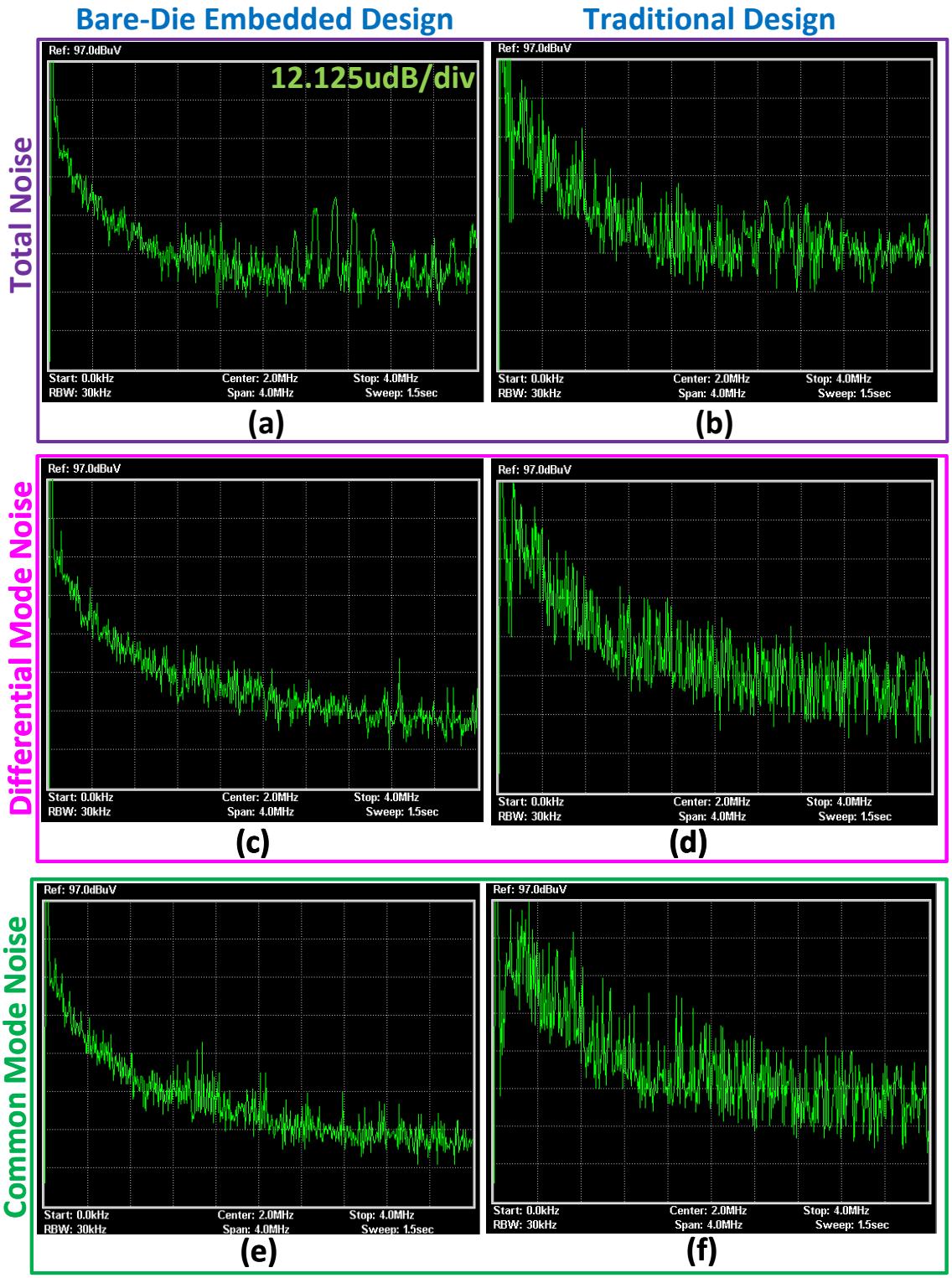


Figure 3.27: Experimental Setup(a) Motor Drive Operation (b) Conductive EMI

CHAPTER 4

On-board Charger (OBC) Development for Small Mobility Application

4.1 Introduction

The lack of onboard charging capability is one of the major challenges for the widespread adaptation of small mobility vehicles such as electric scooters, which arises due to the limited space for power electronics units on the chassis of the e-scooters. Magnetics design is the bottleneck for increasing the power density, and it's also the reason that the e-scooters come with a separate off-board charger as an off-the-shelf planar flyback transformer with the required center airgap and power rating is readily not available in the market. This research solves this problem by designing a very low-footprint multi-winding flyback planar transformer, operating in discontinuous conduction mode with an interleaved arrangement of windings, resulting in a height of only 12mm and improved current density distribution. This led to the realization of a high power-density power electronics unit integrating both the onboard charger and motor drive. A benchmark comparison in terms of power density was made to evaluate the achieved benefits. This enables the user to charge anywhere without carrying a separate off-board charger, contributing to the rapid adaption of electrified transportation. The paper explains the design process, key parametric calculations and considerations, and electrostatic and magnetostatic analysis.

Electric Scooters have the ability to decarbonize transportation at the cellular level and have become a popular mode of global micromobility, thus becoming a crucial part of the electric transportation revolution. The adaptation of electric scooters in urban centers is crucial, and it's now becoming an integral part of urban mobility planning. The global E-scooter market was valued at USD 19.96 billion in 2020 and is projected to reach USD 40.3 billion by 2030, which is a compound annual growth rate of 8.1% [157]. The North American e-mobility revolution continues, as 58.5 million trips were recorded on the E-Scooters in the year 2022. The overall shared micro-mobility trips are up by 40% since 2018, which is a

35-fold increase from 2010, according to the National Association of City Transportation Officials (NACTO) [158].However, some major challenges need to be solved to increase this continuous growth. The charging flexibility is one of the major hurdles in this aspect, as the user has to carry a separate off-board charger or return to the starting point for charging purposes, which limits the range, reliability, and flexibility of e-scooters. EV adoption would rise with the usage of onboard chargers, especially for lightweight EVs intended for urban use. Actually, the amount of space available for housing the propulsion battery pack is limited in scooters and three-wheeled vehicles; as a result, traditional battery solutions can only provide autonomy of 20–30 miles [159].In actuality, onboard chargers greatly increase the range of EVs and may be used with any domestic outlet. Therefore, installing a battery charger on a lightweight electric vehicle is desirable. It should be mentioned that the power demand for a potential fast charge system is not essential for the power converter design due to the propulsion system's relatively small size [160]. No mature technique can be found in the literature for the onboard charging approach of small mobility vehicles. In [161], a wireless charging approach for e-scooters is presented; however, due to the required infrastructure, it's not a feasible approach ready for commercialization. Another approach that can be found in the literature is based on the integration and utilization of the motor windings and used for charging with the help of some additional components and contactor switches that need to be adjusted to select the required operation mode, but this approach still needs a lot of space and is a good fit for heavy electric bikes or electric cars which only uses brushless motors and provides sufficient space on the chassis to get connected with the windings [162]-[163]. Because it may be used in a wide range of electronic systems, the flyback converter architecture is very important in current power electronics research. Its special qualities—such as voltage regulation, galvanic isolation, and straightforward design—make it a top option for a wide range of uses, from high-power industrial systems to low-power gadgets like cell phone chargers. It is essential to power supply design because of its effective voltage stepping capabilities and ability to maintain isolation between input and output circuits. Its performance has also been improved by advances in control techniques, which makes it a perfect fit for electric cars, portable devices, and renewable energy systems. Consequently, in order to advance power electronics technology and create more dependable and energy-efficient electronic systems, it is essential to comprehend and optimize the flyback converter architecture.The contrast between planar and conventional transformer design is a key area of research in power electronics since it clarifies the special benefits that planar transformer design offers. Traditional transformer designs are characterized by wound cores that have toroidal or cylindrical geometries, whereas planar transformers have a flat, stacked construction. The increased power density and efficiency of planar transformer

design is one of its main benefits. Higher power density and more compact integration into power electronic systems are made possible by the planar geometry's more effective cooling and heat dissipation capabilities. Because of their interleaved winding construction, planar transformers also have lower leakage inductance and better magnetic coupling between windings, which reduces switching losses and enhance transient response. Additionally, the planar design provides more control over parasitic components like leakage inductance and stray capacitance, enabling more precise transformer modeling and control. Moreover, planar transformers are more suited for automated manufacturing processes by nature, which results in reduced production costs and increased dependability. Planar transformer design is becoming the preferred option for a wide range of power electronics applications, from renewable energy systems to electric vehicles and beyond. This is because of its significant performance advantages and potential for innovation, as highlighted by the literature comparison between planar transformer design and conventional transformer design.

This work tackles this problem by leveraging the proven flyback topology shown in Fig4.1a that is readily used in the e-scooter off-board chargers by designing an application-specific multi-winding planar transformer for the flyback converter with interleaved PCB windings and discontinuous conduction mode (DCM) operation to achieve enhance power density and efficiency, which reduces the overall converter size and can easily fit and work as an onboard charger on the space available on the chassis of the e-scooters.

4.2 Multi-Winding Planar Transformer Design

The continuous conduction mode (CCM) and dis-continuous conduction mode (DCM) have associated advantages and disadvantages but for our goal of increased power density, DCM offers suitable switching conditions as the diodes operate at zero current before becoming reverse biased, and since the average energy storage is small compared to CCM, the size of flyback transformer can be reduced by operating in DCM mode [164]-[165]. As the benchmark e-scooter is of 1KW and fixed with 36V battery system so considering that the design specifications of the multi-winding transformer can be shown in Table 4.1.

When operating in Discontinuous Conduction Mode (DCM) as opposed to Continuous Conduction Mode (CCM), the flyback converter exhibits different characteristics. The primary winding of the transformer in DCM experiences a zero-current drop prior to the subsequent switching event during each switching cycle. This happens because the primary winding's current flow stops as a result of the transformer's leakage inductance's energy being completely transferred to the secondary side. As a result, DCM's energy transfer process is sporadic, producing a discontinuous current waveform. Benefits of this mode of operation

Table 4.1: Designed Planar Transformer Specifications

Parameters	Value
Input Voltage	90 Vac to 240 Vac
Output Voltage (Secondary)	36 Vdc
Output Voltage (Auxiliary)	18 Vdc
Primary Inductance	313 uH
Leakage Inductance	1.6 uH
Switching Frequency	65 KHz

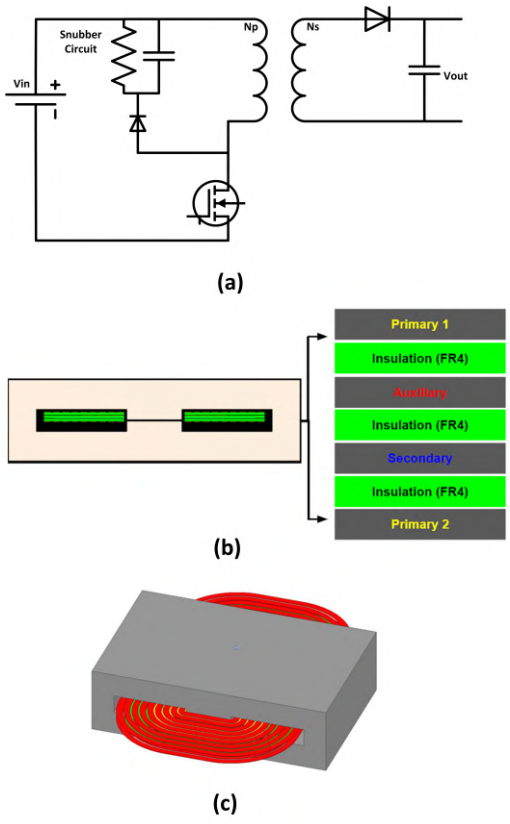


Figure 4.1: a) FlyBack Topology b) Winding Layer Stack c) Designed Planar Transformer Geometry

include lower switching losses, easier control systems, and increased efficiency under light load situations. To avoid problems like voltage spikes and subharmonic oscillations, operating parameters must be carefully considered. Optimizing the flyback converter's DCM mode operation is essential to maximize performance and efficiency in a range of power electronics applications. The power handling capacity of the transformer is determined by the window area product $W_a A_C$, where W_a is the available core window area and A_c is the effective core cross-sectional area. For this scenario, the window area product comes out to be $2.2157 cm^4$. However, none of the available off-the-shelf planar cores can meet the required core area and power handling capability of $75W$, which implies that a customized core design was needed. MnZn Ferrite material was selected for the core, which offers low core loss and high saturation flux density, making it a good candidate for planar designs. The calculation for the required number of turns is accomplished once the core material is chosen and the initial structure and windings layer stack of the transformer was designed as shown in Fig. 4.1b and the constructed transformer geometry in MAXWELL-3D is presented in Fig.4.1c.Understanding a transformer's core and winding losses is critical to power electronics research, especially when it comes to designing and optimizing flyback converters. The transformer's magnetic core material experiences core losses, which are mainly caused by hysteresis and eddy currents. These losses constitute a substantial source of dissipation of energy. Similar to winding losses, which result in additional energy loss as heat, winding losses are caused by the resistance of the wire windings conveying current. These losses have a direct effect on the flyback converter's performance and efficiency, which affects thermal management and total power conversion efficiency. Researchers must minimize core and winding losses through material selection, design optimization, and sophisticated management systems as they work to increase the power density and efficiency of flyback converters. By effectively managing these losses, researchers can unlock the full potential of flyback converters, enabling their widespread adoption in various applications ranging from consumer electronics to renewable energy systems.

Under operational conditions, a transformer's core and copper losses will cause a temperature increase. To prevent harm to the transformer or the remaining circuitry, this rise must remain below a maximum permitted value. Figure 4.2a presents the loss and thermal analysis of the designed transformer. Planar transformers with their interleaved winding structure are a major advancement in power electronics research, providing numerous advantages that improve power converter performance and efficiency. This arrangement enhances the magnetic coupling between the windings and effectively minimizes leakage inductance by splitting the primary and secondary windings into several interleaved layers. Consequently, there are less switching losses, better transient response, and higher power density. Additionally, the

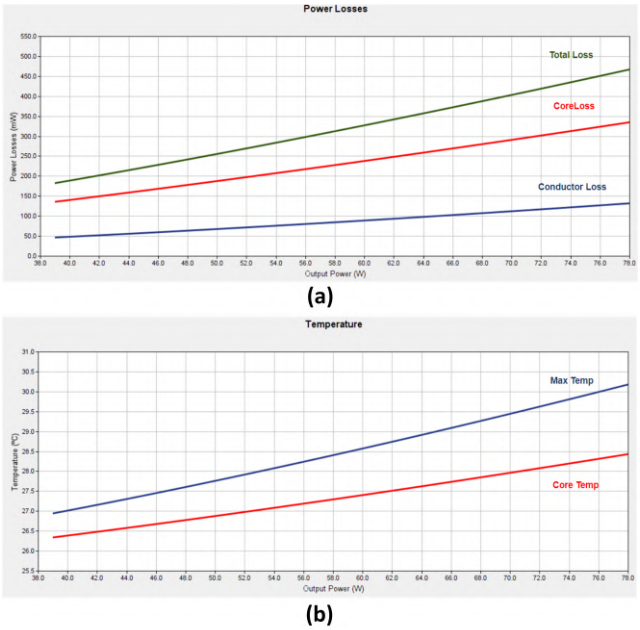


Figure 4.2: a) Power Loss and Output Power b) Temperature and Output Power

transformer's flat shape allows for compact integration into high-density power electronic systems and improved thermal control. Therefore, planar transformers' interleaved winding structure is essential for enhancing power converter performance and making them useful for a wide range of applications. Division of the windings on the PCB layers is an important step with thermal and magnetic consequences. In this work, instead of using the traditional approach to design the required PCB layers, an interleaved approach is adopted, which sandwiched the other layers into the primary layers as shown in the layer stack in Fig. 4.2b, which reduces the proximity effect. The analysis of both conventional and interleaved winding structures was done, and it is concluded from the results shown in Fig. 4.3 that the current density distribution is much better in the interleaved arrangement.

The improved current density distribution translates to better efficiency depicted from the ohmic loss analysis. The magnetostatic analysis performed after the selection of the interleaved winding arrangement confirms the required performance of the designed planar inductor as shown in Fig. 4.4. Within the field of power electronics, a critical measure in guaranteeing the best possible performance and dependability of power conversion systems is the electrostatic and magnetostatic study of planned magnetics. Understanding the distribution of electric fields inside magnetics, especially in components like capacitors and insulating materials, is the main goal of electrostatic analysis. Engineers can find possible high voltage stress locations that could result in insulation breakage or early component failure by ex-

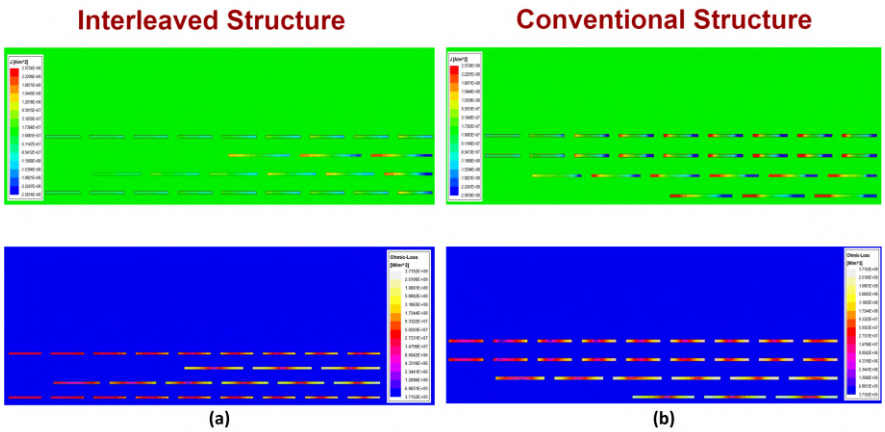


Figure 4.3: a) Interleaved Winding structure b) Conventional Winding Structure

amining the electric field distribution. This study is particularly important in high-voltage applications where dependability and safety depend on meeting strict insulation standards. Conversely, magnetostatic analysis examines the distribution of the magnetic field inside the magnetics, which includes parts like transformers and inductors. Engineers can decrease losses, increase efficiency, and improve overall electromagnetic performance by optimizing magnetic core materials, winding patterns, and geometries with an understanding of the distribution of the magnetic field. Furthermore, the utilization of magnetostatic analysis is imperative in addressing problems like magnetic saturation and core losses, which have the potential to severely impair the efficiency of power conversion systems. Overall, designed magnetics electrostatic and magnetostatic analysis are essential techniques in the design and optimization process that guarantee the performance, dependability, and efficiency of power electronics systems in a variety of applications.

4.3 Experimental Results

A flyback converter hardware's experimental testing process usually consists of multiple crucial procedures to assess the hardware's functionality and verify its design. First, the hardware configuration is done with great care, choosing the right parts such the transformer, switching devices, and control circuitry. After the hardware is put together, it goes through preliminary testing to guarantee correct operation and security. This could entail testing input and output voltages, making sure all connections are made correctly, and looking for any unusual activity. The converter is then put through a battery of testing with varying input voltages, load currents, and switching frequencies, among other working scenarios.

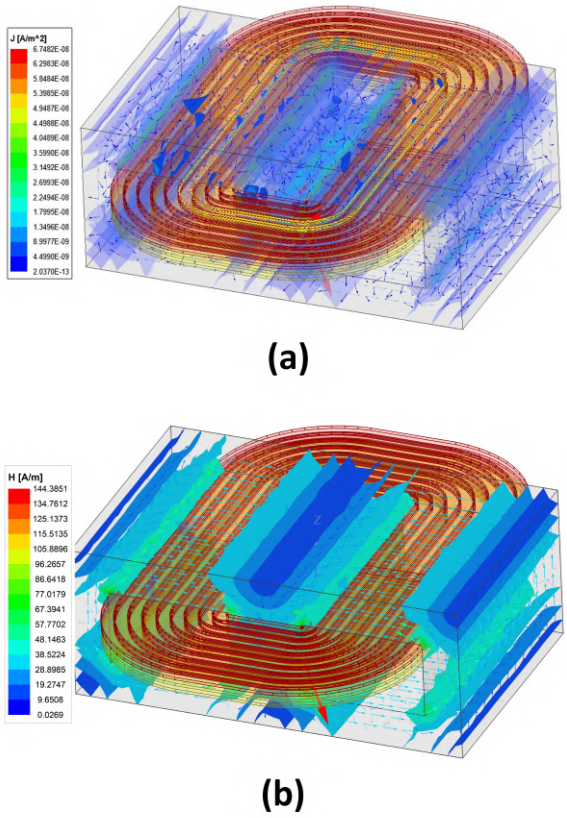


Figure 4.4: a) Magnetic Field Intensity b) Magnetic Field Strength

Meticulously studied and examined are performance factors such output ripple, efficiency, transient responsiveness, and thermal behavior. Furthermore, the resilience and stability of the converter are tested by analyzing its behavior under dynamic conditions, such as load transients. Measurement tools and data collection devices are essential for reliably recording and evaluating the converter's performance indicators during the testing process. Researchers can uncover chances for optimization and enhancement as well as acquire important insights into the behavior of the flyback converter hardware by adhering to a methodical experimental testing strategy.

After the planar transformer and flyback converter were fabricated, the onboard charger board was tested at different load conditions and for universal input range. and placing it within the flyback converter circuit. Figure **??**a shows the flyback planar transformer and the onboard charger converter. The output of the onboard charger can be observed in Fig. 4.5b, which shows the 36V output DC-voltage, and the operation in the DCM mode can be confirmed through the Vds waveform.

To analyze the benefits of the design, the chassis, along with the power electronics unit, is shown in Fig. 4.6a, where it can be observed that no additional space was used when the off-board charger was converted to the on-board charger and packaged within the same case along with the motor drive. The power density comparison compared to the benchmark e-scooter is depicted in Fig. 4.6a, and the overall experimental test bench setup is presented in Fig 4.6b.

In conclusion, this research focuses on developing a very low-footprint planar flyback transformer, which leads to the development of a high power density on-board charger. Due to the achieved high power density, it was integrated and packaged along with the motor drive circuit in the same case without occupying additional space, equipping the e-scooter with the onboard charging capability and contributing to the adaptation of electrified transportation.

4.4 An RMRAC-based Adaptive and Robust Control for a Multi-Winding Flyback Converter in OBC Application

This research presents and evaluates a robust model reference adaptive controller (RMRAC) for a multi-winding flyback converter, which is a compelling choice for the trending small mobility electric vehicles, offering onboard charging capabilities due to the associated advantages of wide input range, isolation, multi-output, low component count, and high efficiency. However, conventional control methods offer loose voltage regulation and poor cross-regulation.

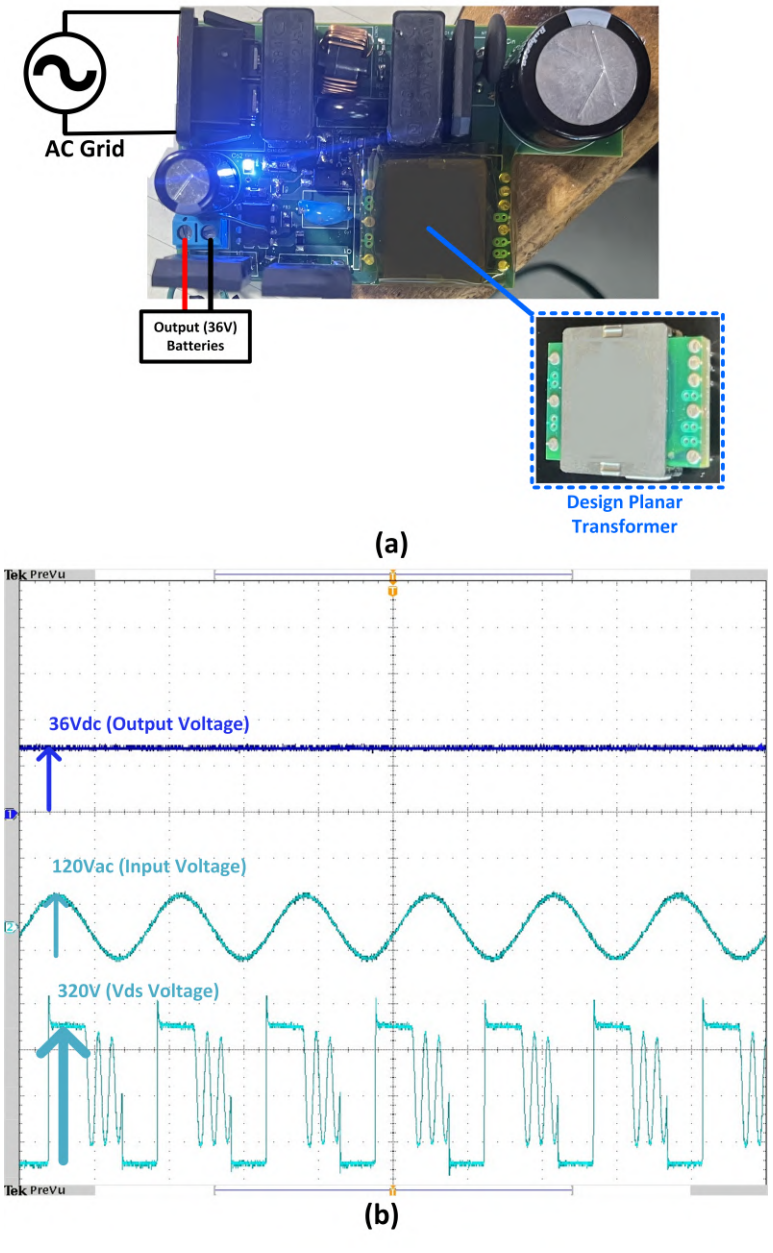


Figure 4.5: a) Designed On bOard Charger b) Experimental Waveforms

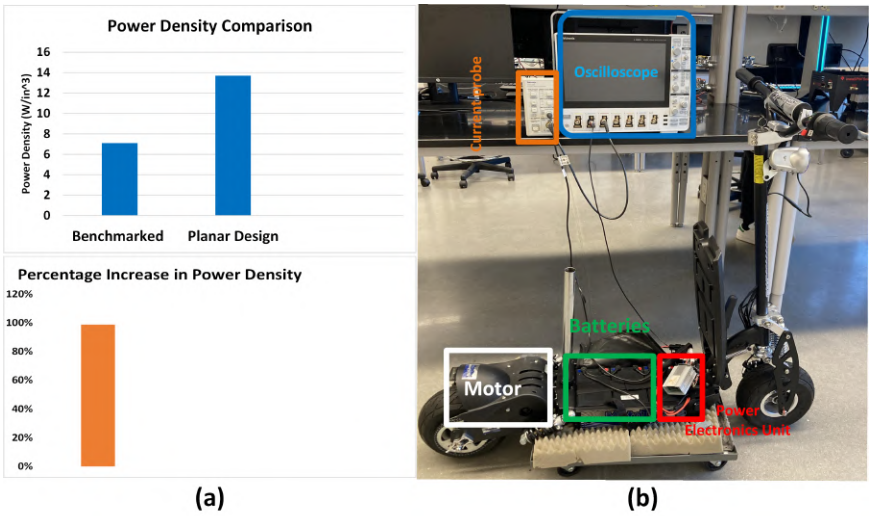


Figure 4.6: a) Power Density Analysis and Comparison b) Experimental Setup

The implemented RMRAC technique proves to be robust and performs better than the classical existing technique in terms of dynamic load conditions and reference tracking. A hardware prototype for a small mobility vehicle, such as an electric scooter's onboard charger (OBC), using the flyback topology, was developed, and the presented control scheme was applied to test and evaluate the performance experimentally.

Small mobility vehicles such as electric scooters contribute to the electrification of transportation at a cellular level and have become a trending mode of transportation in global urban centers. The global E-Scooter market is projected to reach USD 40.3 billion by 2030. The integration of onboard chargers into small mobility vehicles is the most suitable solution to eliminate range anxiety and is implemented in the coming new vehicle models [166]. In electric scooter on-board charger applications, the flyback converter plays a crucial role in enabling the battery systems to be charged effectively and dependably. The flyback converter's ease of use and adaptability make it a great option for electric scooters, where a lightweight and compact design is crucial. In charging systems, its capacity to provide galvanic isolation between input and output circuits and to step up or down voltage levels is especially useful. By doing this, security is maintained and delicate electronics are shielded from possible voltage surges. Moreover, electric scooters can be charged from a variety of power sources, such as home outlets and public charging stations, thanks to the flyback converter's capacity to function over a broad range of input voltages. Its great efficiency also contributes to maximizing the scooter's range and reducing charging times. All things considered, the flyback converter is essential to making electric scooter charging quick and easy, which helps to explain why these vehicles are becoming more and more popular as

environmentally friendly urban transportation choices.

Control design is greatly hampered by the nonlinearities, time-varying dynamics, and parameter uncertainties of flyback converters. Inadequate attention to these aspects can result in inferior performance or instability when using conventional control procedures. Strong control strategies offer a methodical framework for addressing these difficulties and guarantee dependable performance in a variety of operational environments.In order to adapt to shifting operating conditions, adaptive control methods dynamically modify controller parameters based on system identification. Adaptive control approaches provide better performance for flyback converters by continuously adjusting control settings to account for changes in load, input voltage, and component properties. These methods improve efficiency and stability by adaptively modifying control operations, which makes them ideal for real-world settings where operational conditions fluctuate. In order to achieve high-performance regulation in the face of uncertainties, robust model reference adaptive control, or RMRAC, combines the advantages of robust control with adaptive control. To track planned system performance and simultaneously adjust to disturbances and parameter alterations, RMRAC uses a reference model. RMRAC algorithms can improve transient response and stability in flyback converters by dynamically modifying control settings in response to real-time feedback and reference model tracking. RMRAC guarantees dependable operation and excellent performance under a range of operational circumstances by robustly managing uncertainties and disturbances.

For a flyback converter control architecture, good output voltage regulation is required to be robust against changes in load and inputs. Most of the control solutions available currently are based on the classical PID control due to its ease of implementation and acceptable suitable transient and steady-state response [167]-[168]. However, with the advancement in electrified transportation and new incoming industry standards, there is a need for a more robust control architecture that is free from the problem of finding optimal gain setpoints. The setpoints and gains under uncertainties and dynamic operating conditions are still challenging and not mature [169] - [170].

The presented RMRAC control can be a suitable choice for the upcoming advanced applications involving flyback converters, due to the adaptability, robustness, and stability it offers.

4.4.1 RMRAC Converter Control Mathematical Development

The control law can be described as [171]

$$\theta^T(k)\omega(k) + r(k) = 0, \tag{4.1}$$

where $r(k)$ is the reference, $\theta(k)$ is the adaptive gains vector and $\omega(k)$ is the regressor vector. Furthermore, $\omega(k)$ can be written as $\omega(k) = [\ \omega_1(k)\ \omega_2(k)\ y(k)\ u(k)\ ]^T$, in which

$$\begin{aligned} \omega_1(k+1) &= (I + FT_s)\omega_1(k) + qu(k), \\ \omega_2(k+1) &= (I + FT_s)\omega_2(k) + qy(k), \end{aligned} \tag{4.2}$$

where I is a $n \times n$ identity matrix and (F, q) is controllable and with a stable matrix F and a controllable vector q, beign $n_p - 1 \times n - 1$ and $n - 1$, respectively [172]. Also, T_s is the sampling time, u is the control action, and y is the plant output.

The system plant is second order, but a first-order simplified nominal plant is considered for the RMRAC design. In this sense, there is no ω_1 and ω_2. Thus, $\omega(k) = [\ u(k)\ y(k)\ ]^T$. So, $\theta(k) = [\ \theta_u(k)\ \ \theta_y(k)\ ]^T$. Expanding (4.1), and considering a first-order reference model, it follows

$$u(k) = \frac{-\theta_y(k)y(k) - r(k)}{\theta_u(k)}. \tag{4.3}$$

The parameters adaptation algorithm is a modified gradient as

$$\theta(k+1) = \theta(k) - T_s\sigma(k)\Gamma\theta(k) - T_s\ \frac{\Gamma\kappa\zeta(k)\epsilon(k)}{m^2(k)}, \tag{4.4}$$

and the augmented error is $\epsilon(k) = e_1(k) + \theta^T(k)\zeta(k) - y_m(k)$, as well as $\zeta = W_m(z)\omega$. Note that Γ is the adaptive gains matrix, and κ is an additional scalar implemented for accelerated gains convergence. The majorant signal is given by

$$\bar{m}^2(k) = m^2(k) + \zeta^T(k)\Gamma\zeta(k), \tag{4.5}$$

and a σ-modification function is employed to avoid parameters drifting, according to [172]. More details about the RMRAC design can be found in [169, 172].

4.4.2 Hardware in Loop (HIL) Results and Analysis

To evaluate the performance of the RMRAC structure in the steady state and considering dynamic conditions, the power converter was implemented considering a Typhoon HIL 604 device. Moreover, the control algorithm was implemented in a TMS320F28335 DSP. The RMRAC tuning gains were: $\Gamma = 1$, $\kappa = 100$, $\theta_0^{T(k)} = [\ -1\ \ -0.2\ ]$. The designed reference model can be written as

$$W_m(z) = \frac{0.7351}{(z - 0.2648)}\ , \tag{4.6}$$

obtained with $T_s = 1/20$ kHz and zero-order holder (ZOH) method.

A standard PI controller was tuned for comparison with the adaptive controller. The PI controller equation is as follows:

$$C_{PI}(z) = \frac{3.7929z - 3.731}{(z-1)}, \tag{4.7}$$

also discretized considering $T_s = 1/20$ kHz and ZOH method. Fig.2 and 3 present the

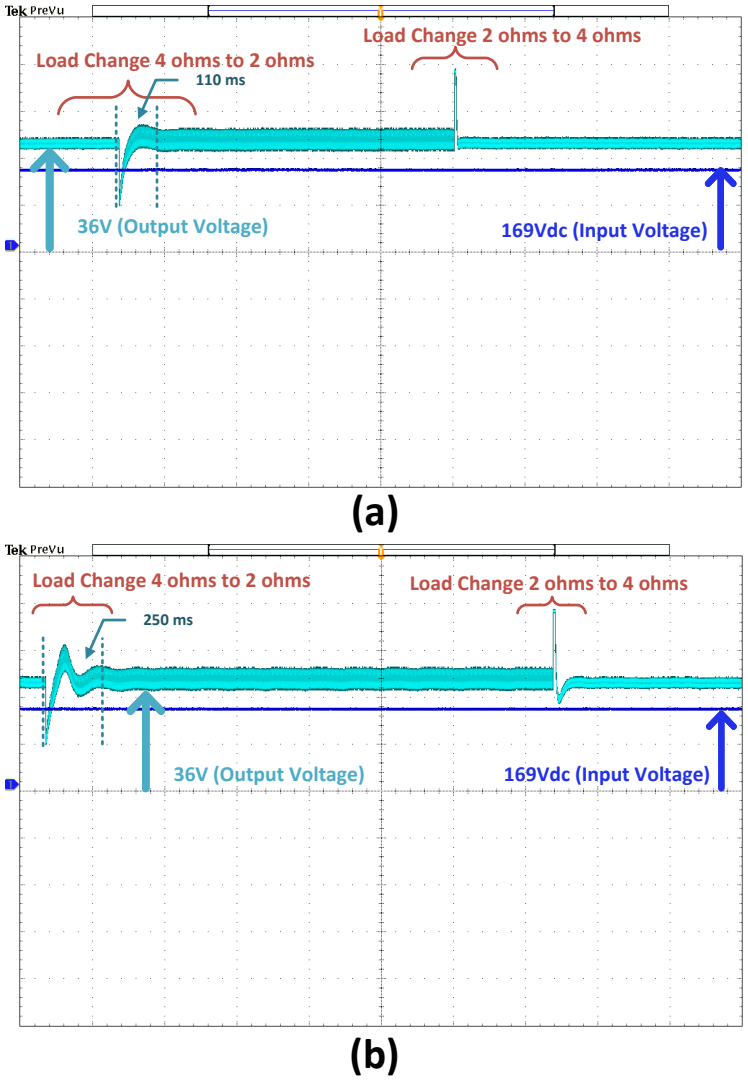


Figure 4.7: Experimental Results. (a) RMRAC Dynamic Load Changing Performance; (b) Traditional Controller Dynamic Load Changing Performance.

regulated flyback converter with both adaptive and classical controllers. For checking the controller performance and robustness, the regulated voltage was changed (Fig.2(a)-(b)) and

load steps were performed (Fig.3(a)-(b)). It is possible to observe that when the reference voltage was changed from 36 to 30 V, the RMRAC controller adjusted itself and tracked the reference within 30 milliseconds as compared to the 40 milliseconds taken by the traditional controller, which is a 25% improvement. Similarly, during the test scenario of sudden load changes from 4 ohms to 2 ohms, the RMRAC controller achieves a steady state in 110 milliseconds as compared to the 250 milliseconds taken by the traditional controller, which is a 56% improvement. For the graphs in Figures 2 and 3, the X-axis has time, and the output voltage in volts is depicted on the Y-axis, which is also highlighted by the annotated marker.

The regulated output voltage tracking error is presented in Fig 4.8. It is possible to observe that the RMRAC structure exhibits superior performance in terms of regulation for both under load-varying conditions (Fig. 4.8(a)) and under steady-state conditions (Fig. 4.8(b)). Under load-varying conditions, the RMRAC control attains a root mean squared (RMS) value of 0.1405 V, compared to the RMS value of 0.1643 V for the conventional controller, which is a 14.5% improvement. Similarly, for the steady state conditions, the RMRAC attains the RMS value of 0.0871 V as compared to the RMS value of 0.1566 V for the traditional controller, which translates to 44.4% improvement.

The controller performance evaluation set up, along with the developed prototype of the flyback converter, is shown in Fig 4.9(a). Fig. 4.9(b) shows the discontinuous mode operation (DCM) of the developed flyback converter prototype where the V_{ds} waveform proves that the converter is operating in the DCM mode and provides a stable output voltage.

In this research, an RMRAC control architecture for a multi-winding flyback converter for small mobility OBC applications was implemented and evaluated. Hardware results prove that the presented control scheme performs better in terms of tracking errors, load changes, and reference changes, ensuring high-quality voltage regulation and minimum cross-regulation.

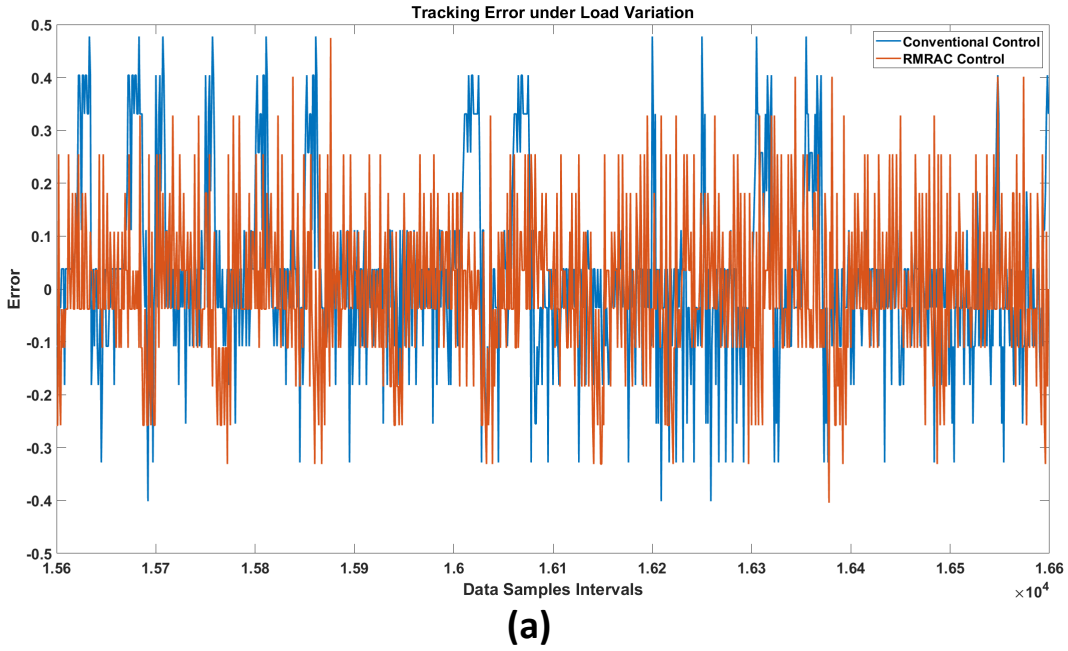
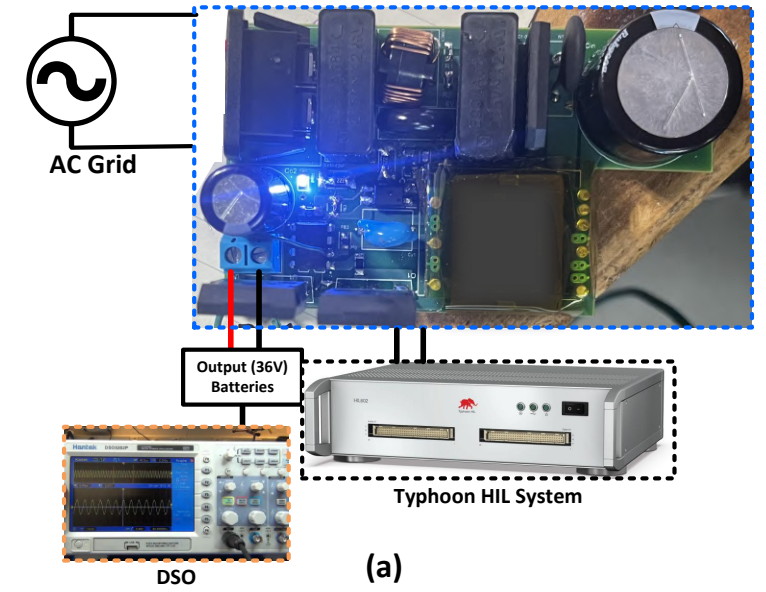


Figure 4.8: Tracking Error Comparison. (a) Dynamic Load Condition; (b) Steady-state Condition.



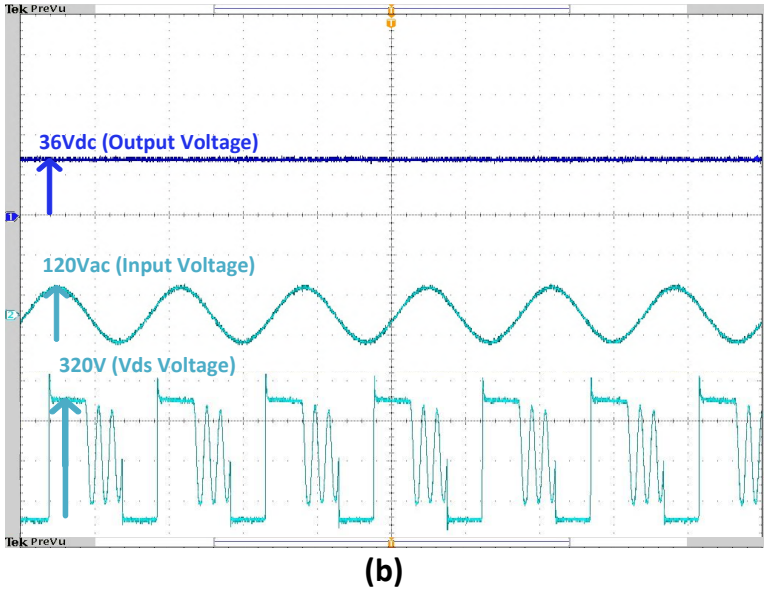


Figure 4.9: Setup and DCM operation. (a) Experimental and HIL Setup; (b) DCM mode Experimental results of the flyback.

CHAPTER 5

GaN based High Power Density and High-Efficiency Motor Drive for eVTOL Applications

5.1 Introduction

The growing interest and investment in urban air mobility (UAM) solutions such as the electric vertical take-off and landing (eVTOL) aircraft with electric motors-based distributed propulsion driven by a power electronics converter is aimed at solving the road congestion and carbon footprint problem. However, these systems demand highly efficient, reliable and compact power trains which can be enabled through the wide band gap (WBG) semiconductor technology such as Gallium Nitride (GaN). Despite GaN's promising characteristics and superior performance its adoption in high power commercial applications has been limited by its low current handling capability and high sensitivity to the parasitic effects, that maps to un-reliability. This paper solves these challenges by presenting the design and optimisation framework for a multi-parallel GaN based motor drive, for low-voltage and high-current eVTOL applications. The proposed approach specifically focuses on the key challenges including parasitic minimization, electromagnetic interference (EMI) mitigation at the board level and an optimized PCB layout. A comprehensive design framework is introduced, enabling the development of a high power density GaN-based motor drive capable of lifting 50 kg of payload, in addition to the vehicle's 47 kg structure weight. By leveraging the benefits of GaN through multi-paralleld architecture the developed system demonstrates significant improvement in power density, and efficiency was achieved compared to the benchmark designs.

The global trend of urbanization has created challenges such as traffic congestion, longer commute times, and increased carbon emissions especially in urban centers. As a solution, the concept of urban air mobility (UAM) has gained significant traction recently. The UAM

vision is to transform the traditional transportation system through aerial transportation that operates above the ground level traffic by utilizing electrical vertical take off and landing (eVTOL) aircraft. This will ensure fast commutes, quite operation, low emissions, and flexibility of take off and landing in an urban space. Data projections show that 68% of the global population will reside in urban centres by 2030 [173], which calls for the need to develop efficient transportation solutions such as eVTOL aircraft that don't contribute to traditional road congestion.The National Aeronautics and Space Administration (NASA) along with other industry leaders have placed UAM as a critical pillar for future smart cities. NASA's UAM Grand Challenge [174] and similar initiatives in Europe [175] and Asia [176] are accelerating the development of certification standards, air traffic management strategies, and infrastructure requirements for aerial mobility. The major aircraft and aerospace companies, such as Airbus, Boeing, etc., have also conducted various studies to demonstrate that electric propulsion-based aircraft with distributed propulsion enhances the safety, reliability, redundancy and controllability in their Concept of Operations (ConOps) for Uncrewed Urban Air Mobility release [177]. Aditionally public and private investments in such startups and ventures have significantly increases with companies like Archer Aviation [2], Volocopter [178], and Vertical Aerospace [179] demonstrating their products and securing billions in funding to develop scalable air taxi platforms. According to market projections, the global UAM market is expected to exceed USD 45 billion by 2030, underscoring its economic and technological importance [180].

Table 5.1: Tale 5.1. Power Density Comparison

Sr. No	**Manufacturer**	**Specs**	**Power Density**
1	Spectrum Firma [181]	36V/160A (3-8S)	$7.17W/cm^3$
2	Flipsky [182]	22.8V/100A (3-6S)	$11.23W/cm^3$
3	Castle Edge [183]	24V/80A (3-12S)	$11.6W/cm^3$
4	Flipsky[182]	45V/50A (5-12S)	$23.9W/cm^3$ (Liquid Cooled)
5	Hobby Wing [184]	22.2V/32A (3-6S)	$21.7W/cm^3$
6	Flipsky [182]	75V/100A (4-20S)	$20.7W/cm^3$
7	AMPX [185]	36V/30A (12S)	$22.4W/cm^3$
8	Tiger Motors [186]	22V/42A (6S)	$22.8W/cm^3$
9	Hobby Wing X13 [184]	76V/36A (18S)	$13.08W/cm^3$
10	**This Research**	**76V/2.5KW (18S)**	$52.6W/cm^3$

The advancement in mechanical and aerodynamics are advancing rapidly however, the electric powertrain is one of the most critical part as it needs to be efficient, light weight, reliable and capable of operating under harsh conditions. The WBG devices such as GaN has the potential to push the boundaries of power density and efficiency in aviation applications however, there are certain challanges with using the GaN devices design for high power

and high current applications that need to be resolved. One of the main design challenges is that GaN devices are more difficult to use for high current applications due to their limited product lines or lower current ratings when compared to Si devices [187]-[188] and the other challenge is the sensitivity of GaN devices to the parasitics. Paralleling several GaN devices can address the low current capability issue, but this approach has drawbacks of its own, including device mismatch, current imbalance, overshoots, switching losses, and parasitic effects that result in device failure and electromagnetic interference (EMI) problems [189]–[190]. Moreover, the GaN paralleing approach makes the other challenge of parasitic sensitive issue even more harder. So there is a need for an optimized PCB layout approach for such devices, which is presented in this paper. GaN devices' fast switching speeds and sensitivity exacerbate these problems [191]. Therefore, a very thorough and optimized PCB layout, power loop design, and gate loop circuits are necessary for a dependable and effective GaN-based design. This research aims to develop an optimum design.

The current literature focuses more on the GaN half bridge modules development for low current applications. In [192] and [193] the gate drive part of the GaN circuits were studied and the circuit simulation model was proposed in [194]. In [195] a low power boost converter operating at 1MHz was presented. In [196] and [197] the authors demonstrates the parasitic performance comparison and its effect on the converter performance along with the Si and GaN comparison. In regards to the GaN devices most of the research is focused on developing the GaN modules and their characterization. A few examples of GaN based converters can be found but they are all for low power applications. Moreover, some evaluation boards are being presented by GaN manufacturers such as from Transphorm in [198] where a single phase converter has been developed to test the performance. In [199] a GaN based Quazi Source converter was presented in [200] which was developed for renewable energy applications. The abnormal behaviour of GaN at high frequencies was reported in [201], which focuses on the impedance network reduction. In [202] a grid connected GaN based inverter was developed. A hybrid switching cell consisting of Si and GaN was developed in [203] to be used in full bridge converter applications. In all of the mentioned literature, there is no focus or solution presented on the design of multi-paralleled GaN devices, which is presented ion this research and is essential to realize a system level GaN based design and utilize the benefits it offers. This research covers the research gap including the preposition of a framework for designing a multi-paralled GaN design, while minimizing the gate and power loop inductances to realize high current operation. For Si devices there is good design literature where multi-paralld Si devices have resulted in high current and high power operation[204, 205, 206, 207, 208], and some design optimization approach for Si designs has been suggested [209] and [210], however considering the different nature of the Si and GaN devices, those design approaches

are not applicable to the WBG or GaN devices that are too sensitive to parasitic and EMI effects.

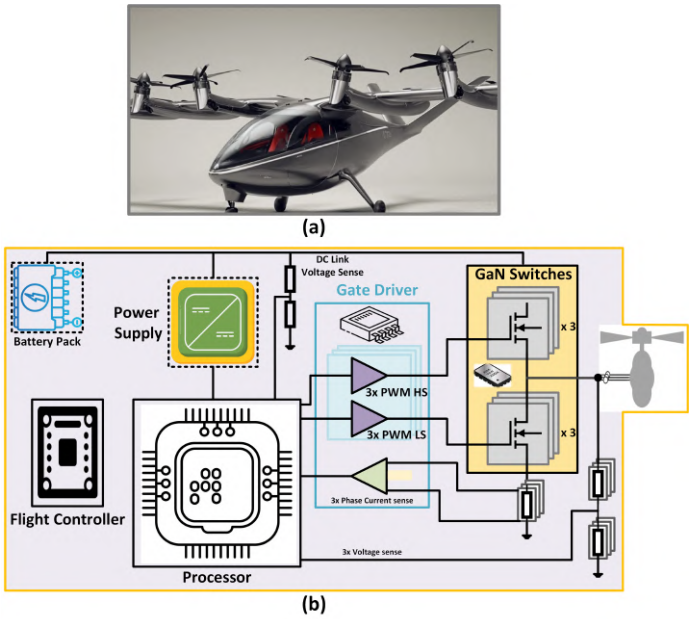


Figure 5.1: (a) eVTOL Aircraft-Archer [2] (b) eVTOL Motor Drive Architecture

In this research an eVTOL architecture comprising of four individual motors, each powered by a dedicated motor drive is considered.The concept diagram of the eVTOL aircraft from Archer [2] is shown in Figure 5.1a. The objective was to develop a muti-paralled GaN based motor drive capable of enhancing current-handling capacity through effective current sharing among parallel-connected devices. The research contribution lies in the proposed optimization framework, which enables the design of a high power density motor drive with minimized parasitics and improved electromagnetic interference (EMI) performance. This paper presents a comprehensive design methodology, covering everything from PCB layer stack-up selection to the strategic placement of GaN devices, gate drivers, DC-link capacitors, and other critical components. It also details the parasitic extraction, analysis, and reduction strategies that were employed to minimize voltage overshoots and mitigate EMI-related issues, ultimately resulting in a high-efficiency and compact power converter. Following the proposed framework the developed GaN based motor drive power density was compared against the benchmark and existing state of the art designs available for aerial vehicles. The comparison is shown in Table 5.1, which depicts superior power density performance of $52.6W/cm^3$, which is essential for the stringent constraints for aerial vehicle applications.

The paper is organized as follows: The introduction section provides a detailed overview

of the challenges that led to this research, and then an in-depth literature review to provide a comparative analysis of the existing solutions. Section II provides insights into the GaN based Multi-paralled Design and consideration. Section III provides the layout optimization process, parasitic extraction and analysis. The Experimental Analysis section provides the hardware design overview, experimental setup, and the results achieved to justify the superiority and significance of this research.

5.2 Multi-Parallel Design Optimization Framework

To enable the high current and high power operation using GaN devices, three paralleled GaN devices were used on the high and low side in each phase. As this is an aerial vehicle application so four electric motors are power through four motor drives, centrally controlled through a flight controller. The architecture of the vehicle is shown in figure 5.1b.

The PCB layout is the critical aspect in this GaN based high speed and high power design, where power density and EMI are of paramount importance. ANSYS Siwave and Q3D was used to extract, analyse andoptimiza the PCB layout following the proposed framework shown in figure 5.5. The designed PCB is imported to ANSYS Siwave for signal and power integrity analysis and after verification and validation of the stack up its forwarded to Q3D to extract the gate and power loop parasitic. Once the parasitics are extracted, the parasitic parameters are modelled in simulation to analyse the overshoots in the design. If the overshoots are high due to the high pararitics, the loop is repeated and the design is modified for layout optimisation.

The challenge here is to layout the parallel GaN devices in a way to ensure equal current distribution among them. Moreover, dividing the current stress also translates to low conduction losses per device and low thermal requirements enhancing the overall power density. So there is a need to design optimal and identical paths for all the gate drive signals. The placement of the gate driver IC itself is very crucial as in general in needs to be physically as close to the devices as possible to reduce the parasitic, but here since we have odd number of devices so its not possible to place it at an equal distance from all devices. The placement axis and exact position of the gate driver IC were finalised by repetitive optimisation of the design using ANSYS-Q3D to achieve the lowest gate loop parasitic possible. A half bridge gate driver IC STDRIVEG600 from STM-electronics y, bootstrap management, and narrow pulse width capability. Amonst many possible configuration for the gate driver IC, the two configurations shown in 5.2 are the most convincing i.e. on the X-axis (orthogonal to the GaN switches-5.2c) shown in 5.2a and along the Y-axis as shown in Fig. 5.2b.

For GaN devices, the EPC 2305 was used, which offers the voltage rating of 150V and 101A

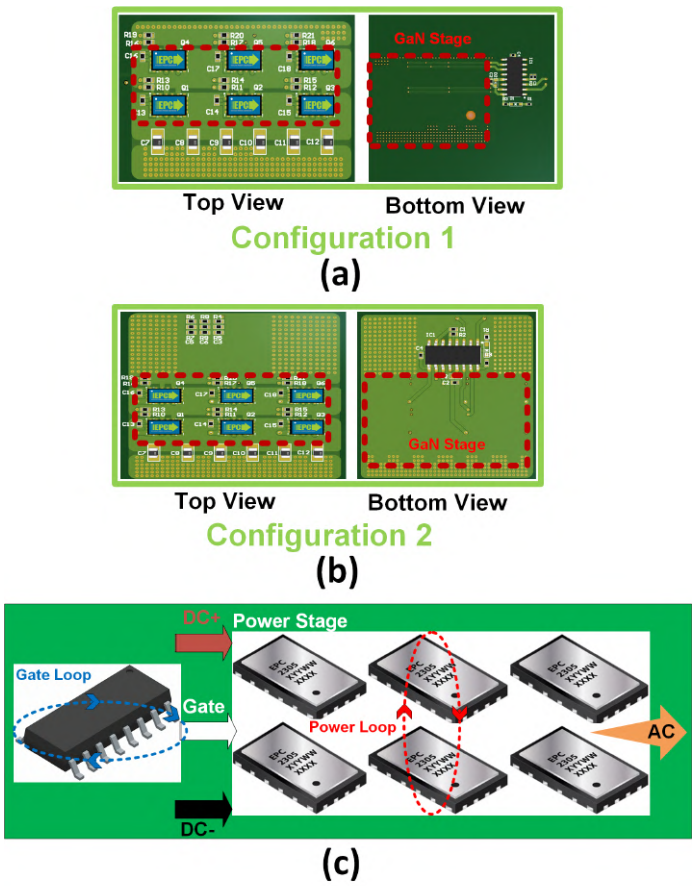


Figure 5.2: Gate Driver IC Placement (a) along X-axis(b) along Y-axis (c) Orthogonal gate and power loop

with the minimal R_{ds} of $3m\Omega$. Following the parasitic extraction and analysis, configuration 1 was found better, and it also has the benefit that the gate and power loop are orthogonal to each other, which helps in suppression and cancellation of EMI noise. The common gate driver appeaoch here allows for 100-300ns deadtime, which needs small turnoff, and large turn-on resistance to prevent Miller turn-on. Based on the analysis and repetitive optimization, the high fidelity model of the extracted parsitics is shown in Fig. 5.3 and the achieved gate and power loop parasitic are presented in Table 5.2.

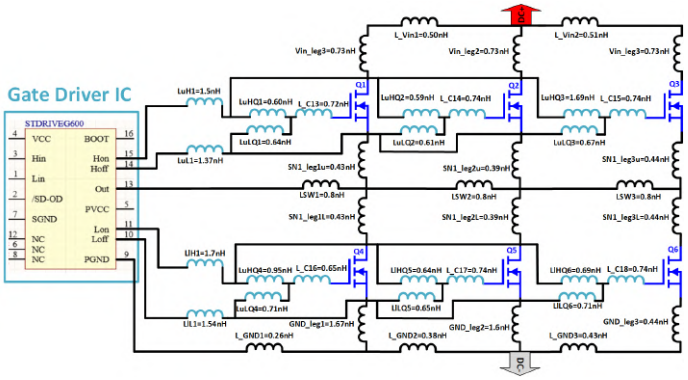


Figure 5.3: High Fidelity parasitic Model based on optimised and extracted parasitics for Phase A

Table 5.2. Designed and Extracted parasitics

	Inductance (nH)
High-side Power Loop	1.66
Low-side Power Loop	2.48
Total Power Loop	4.14
Gate Turn ON Loop	2.82
Gate Turn OFF Loop	2.73
Gate Return Path	0.82

To analyse and verify the obtained parasitic, and to gauge the effectiveness of the proposed optimization framework, the double pulse test (DPT) analysis was done. DPT is the best way to observe the influence of layout parasitics on losses, overshoots, and overall performance. A phase current of $33A_{rms}$ is required for the rated power of 2.5KW with the battery voltage of 76V.

The low on-state resistance of GaN helps to reduce conduction losses, quick switching times reduce conduction losses, and the intrinsic feature of no reverse recovery phenomena completely removes reverse recovery losses. Together, these benefits greatly increase efficiency, decrease the need for thermal management, and minimize the device's overall power

loss.The double pulse result confirms that the turn-on energy (E_{on}) is 17.8μJ and the turn-off energy (E_{off}) is 2.3μJ which is significantly lower compared to the traditional Si devices used currently. The DPT results and analysis is presented in Fig.5.4.

5.3 GaN-based Motor Drive Design

The design consists of a ten layer stackup consisting of signal, power and ground layers. The thickness of the copper for outer layers are 2oz and 3oz for inner layers to ensure high current carrying capability. Moreover, the high speed and low-voltage signals needed to be isolated from the high power signals to avoid interference, crosstalk talk and potential EMI issues. The signals are also laid out vertically and horizontally on alternate layers to help with EMI mitigation through field cancellation. The designed layer stack is shown in Fig.5.6, which resulted in the overall board thickness of 2mm. Every layer is specifically configured for logic, high-frequency, ground plane, and high-power signals. The arrangement of these layers is calculated to guarantee interference reduction and flux cancellation. Beside the same planes, further orthogonal signal routing was carried out. To lessen the return current discontinuity, decoupling capacitors were positioned during the signal interlayer transition. The layer stack is set up so that the ground planes are positioned correctly to shield the signal layers. To improve heat conduction and thermal performance, all of the vias were filled and capped.

The ANSYS analysis was used to optimize the distance and placement of the GaN devices and the gate driver circuitry, which are positioned on the top side and bottom side of the PCB respectively. To make the placement of heatsink possible on the top layer, any other components in the gate drive and power stage that has more height than the GaN chips are positioned on the bottom side or away from the GaN devices. The DC link capacitors are placed adjacent to the power devices so that they are in close proximity without interfering with the heatsink's placement. Figure 5.7 shows the labelled designed PCB.

The thermal dissipation of the designed board is very important as its the deciding factor in determining the power density. In this case the top cooled GaN devices are used so the heatsink will be attached to the top side. In this research the thermal simulations were done for the design board under various conditionsi.e. with heatsink, without heatsink, with forced convection (air) and under varying air speed, as this is an aerial vehicle applications and we can take the advantage of the surrounding air to cool down the motor drive. This will help us to downsize the heatsink requirements, increasing the overall power density and weight, which is crucial for aerial vehicles. For thermal simulation purposes, a two-way coupled thermal simulation approach was adopted that simulates the dependency of power

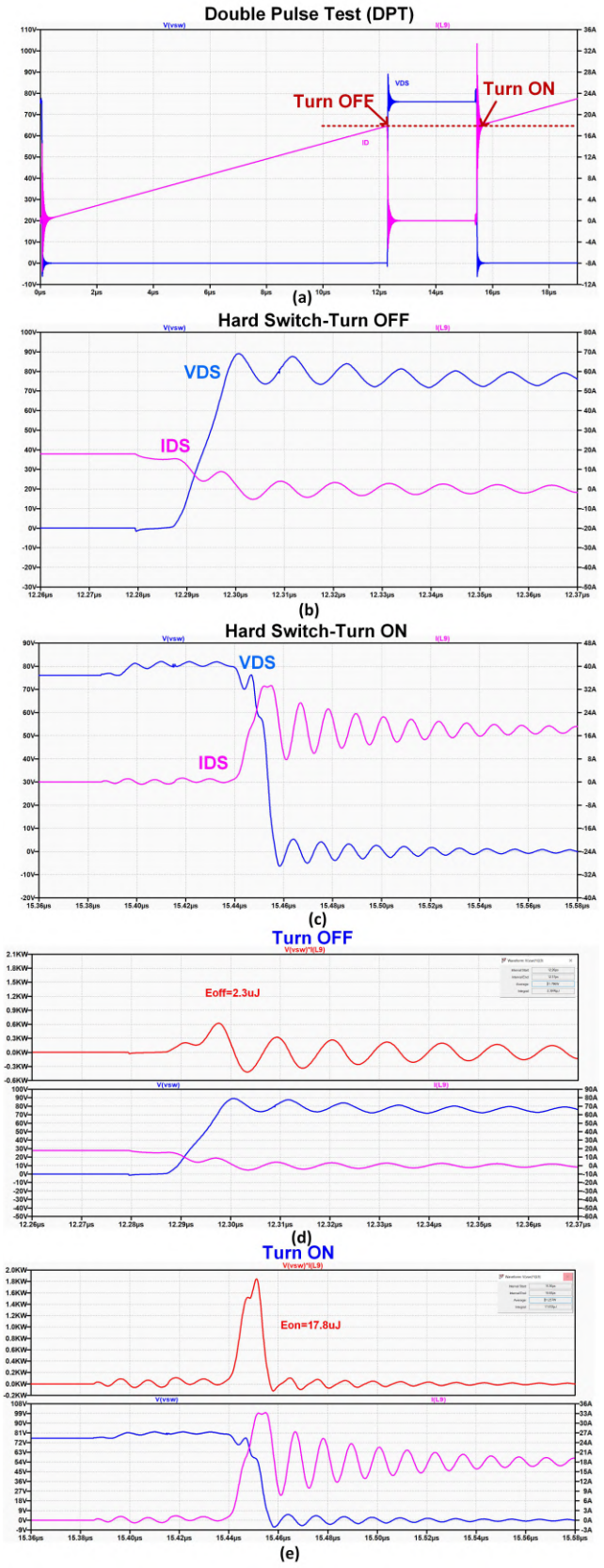


Figure 5.4: (a) Double Pulse Test (b) Hard Switch Turn ON (c) Hard Switch Turn OFF (d)Double Pulse Test-Switching Characteristics Analysis - Turn Off time (e) Double Pulse Test-Switching Characteristics Analysis - Turn On time

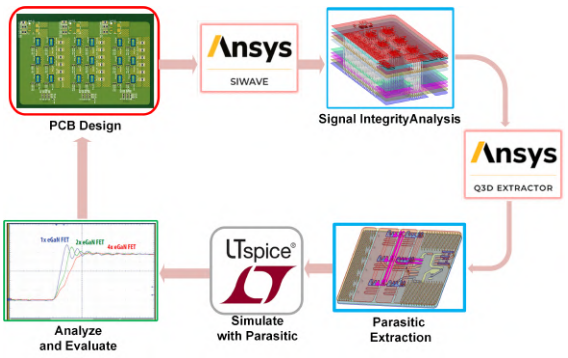


Figure 5.5: Proposed Optimization Workflow

loss and temperature, which are dependent on each other. It's computationally heavy, but results in more accurate thermal estimation.

Table 5.3 presents the thermal analysis under varying air speed and various heatsink options. Based on the analysis it is concluded that a $10mm$ high heatsink is enough for this application, as the airspeed is more than 6/s when the vehicle is in the air, which means the board temperature will be even lower. Figure 5.8 shows the thermal simulation cases where it can be seen that in Fig.5.8a with a $10mm$ high heatsink and natural convection, the estimated temperature is $122C$ the surrounding air is 6m/s and the estimated temperature is $42C$ as shown in Fig.5.8b.

Table 5.3.Thermal analysis under varying conditions

	Analysis Case	**Heat Sink Height**	**Air Speed**	**Temperature**
No Air	1	×	×	$169C$
	2	$10mm$		$122C$
	3	$30mm$		$111C$
Air Speed 2 m/s	4	×	$2m/s$	$134C$
	5	$10mm$		$75.8C$
	6	$30mm$		$71.9C$
Air Speed 4 m/s	7	×	$4m/s$	$104.3C$
	8	$10mm$		$61.1C$
	9	$30mm$		$56.3C$
Air Speed 6 m/s	10	×	$6m/s$	$91.9C$
	11	$10mm$		$44.3C$
	12	$30mm$		$42.1C$

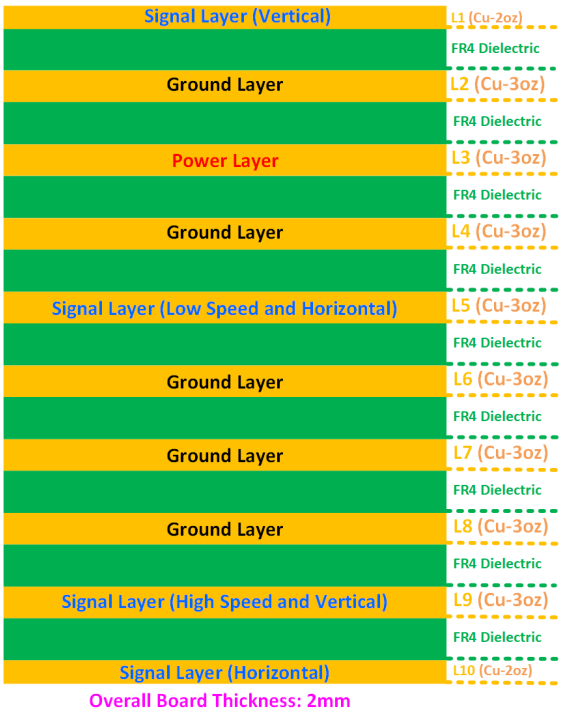


Figure 5.6: Designed GaN Motor Drive Layer Stack

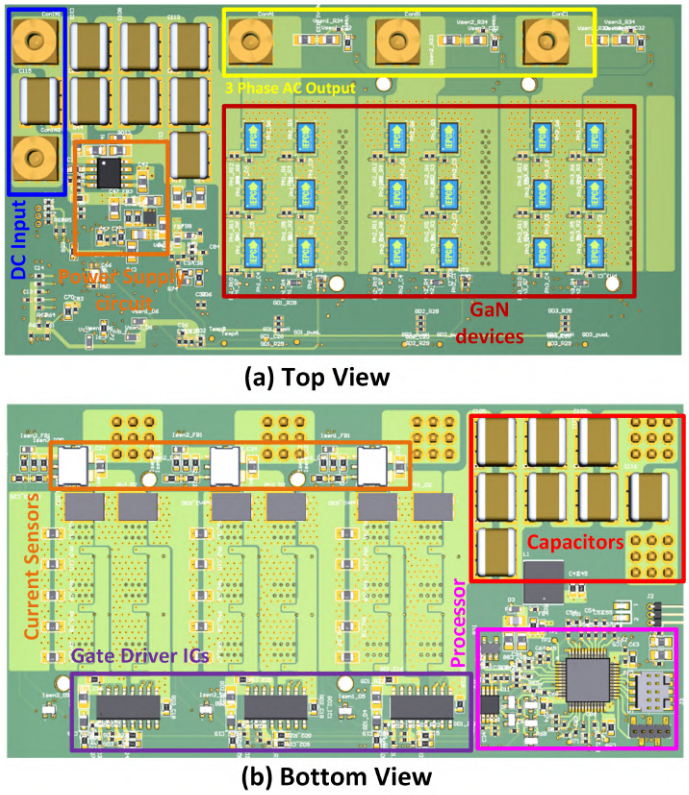


Figure 5.7: (a) Designed PCB-Top View (b) Designed PCB-Bottom View

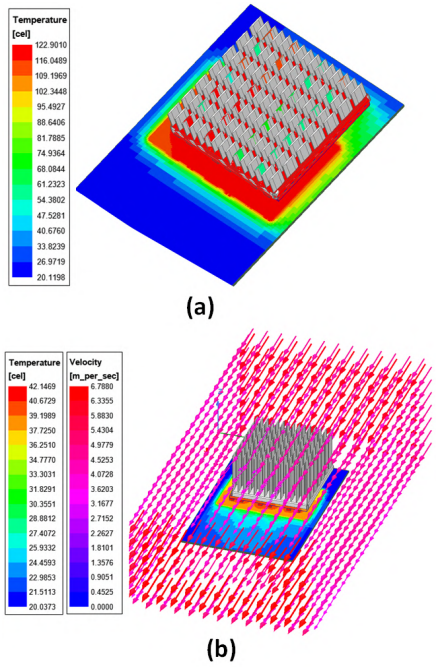


Figure 5.8: (a) 10 mm Heat Sink-Natural Convection (b) 30 mm Heat Sink-6 m/s forced air convection

5.4 Experimental Results and Analysis

For the experiential validation the designed board was populated with the GaN dies and other components and then tested at both RL load and with a BLDC Motor. The experimental setup is shown in Fig.5.9a which depicts the design GaN motor drive is connected to the DC power supply which emulate the battery voltage. The designed hardware GaN based motor drive is shown in Fig.5.9b, which also shows the view of GaN dies attached to the PCB beneath the heatsink. On the load side, RL load as well as a BLDC motor is connected that is attached to the frame of the benchmark aerial vehicle. The benchmark motor drive is a state-of-the-art Si-based motor drive, and an efficiency comparison of the proposed GaN-based design with the benchmark design is presented in Fig.5.9c.

For the 2.5 kW power requirement in this application and also for the benchmark comparison at the same power level, the developed design was tested at the required power as shown in Fig.5.10a, where we can see the three-phase current waveforms. Moreover, Fig.5.10b is a validation of our optimized design and extracted parasitics through simulation, as it's the drain-to-source voltage waveform that is affected the most when parasitics are involved in the design. Here, it can be seen that the overshoot on the Vds waveform is within the acceptable range and in coherence with the DPT and simulation results, which proves the effectiveness of the proposed framework.

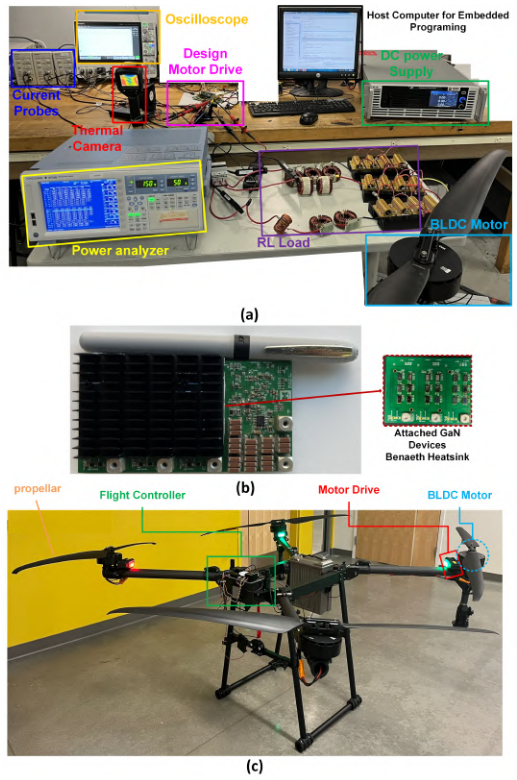


Figure 5.9: (a) Experimental Setup (b)Designed GaN-based Motor Drive (c) Benchmarked aerial vehicle for test setup and performance comparison

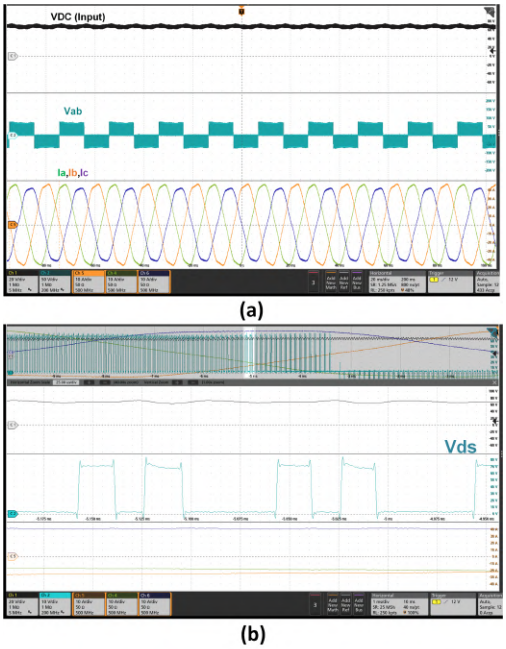


Figure 5.10: (a) Experimental Results- GaN based Motr Drive (b) Drain to Source Voltage Waveform

One of the motivation for using GaN is to benefit from its great efficiency characteristics. To verify the performance efficiency, the developed design was operated at various load levels, and the efficiency was recorded, which was then compared with the benchmark Si-based motor drive, in Fig.5.11 which proves the superiority of the developed design.

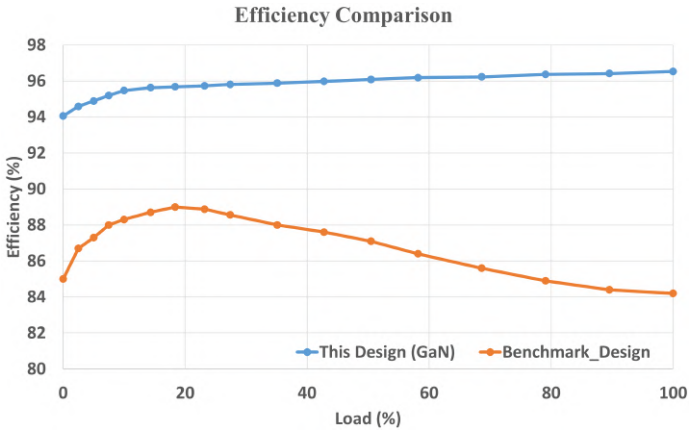


Figure 5.11: Efficiency Performance Comparison

Similarly, thermal performance is another metric that is important for overall power density and performance. In this research, the current stress is divided among paralleled GaN, reducing the conduction loss and eliminating reverse recovery loss due to the inherent characteristics of GaN devices. Figure 5.12 shows the thermal performance under different conditions, such as with no air and no heat sink, air cooled, and the case when both heat sink and air cooling were applied. The experimental results shows that they corresponds closely with the predicted simulation results.

In conclusion, this research introduces a multi-paralleled GaN-based motor drive solution that achieves high power density and efficiency, for aerial vehicle applications. An optimization framework for designing such high-power, sensitive devices based systems is proposed and experimentally validated. The work also includes detailed considerations for layer stack design, EMI mitigation, PCB layout, and thermal management strategies. A method for parasitic parameter extraction is outlined, followed by its optimization using Double Pulse Testing (DPT), with results closely matching experimental data. Additionally, a comparative analysis against current state-of-the-art solutions highlights the proposed design's significant improvements in both power density and efficiency.

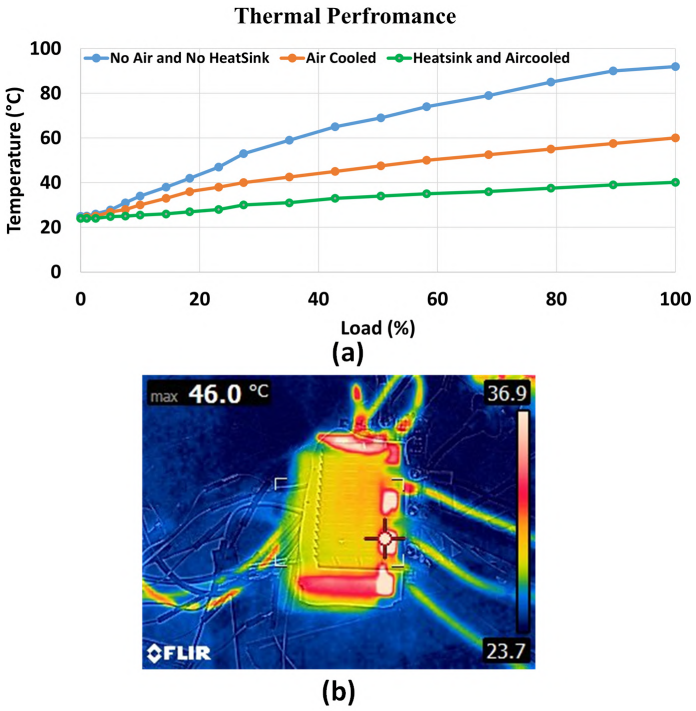


Figure 5.12: (a) Experimental Thermal Performance Under varying conditions(b) Experimental thermal image with heatsink and forced convection (air at 6m/s)

5.5 Integrated Heat Sink Design for Motor and Motor Drive in eVTOL Vehicles

The growing interest and evolution of electric vertical take-off and landing (eVTOL) aircraft demand greater power density, system integration and new thermal management techniques in the propulsion system. This research presents an integrated thermal and mechanical heatsink structure that combines the electric motor and developed Gallium Nitride (GaN) based motor drive into a unified and integrated geometry with a shared heatsink. The proposed co-deign approach significantly enhances the power density, minimizes interconnect parasitics, reduces thermal resistance and improves the electromagnetic compatibility (EMC) at a reduced cost. The integrated heatsink design simultaneously cools both the power electronics and motor, optimized through multiphysics thermal and airflow simulations, to achieve a compact and lightweight form factor, which is critical in eVTOL applications.

5.5.1 Introduction

The growing trend of urban air mobility and electric vertical takeoff and landing (eVTOL) vehicles has resulted in the demand for lightweight, high-power density, highly efficient,

and integrated propulsion systems. The most important parts of the propulsion system are the motor and motor drive. Traditionally, motors and the motor drives are treated as separate and electrically connected through long wires, housed with individual thermal heat sink strategies. This traditional approach results in parasitic losses, electromagnetic interference (EMI) challenges, increased weight, and inefficient thermal dissipation. All of these parameters are very critical for flight or aerial applications where weight, efficiency, and system reliability are significant. The literature review suggests that integration of the motor and motor drive however most of the work is focused on doing the integration on the motor design level[211]-[212].

In this research, these challenges are solved through the design of an integrated heatsink that combines the motor and motor drives. It thermally combines the motor and motor drive, eliminating the need for long interconnecting wires and the need for a separate heatsink, which leads to significant improvements in power density, thermal efficiency, compact structure and weight reduction that increases the overall flight time.

The proposed integrated heatsink dissipates heat from both the motor and the power electronic switches on the motor drive PCB while also acting as a structural interface between them. The integrated geometry enables the use of busbars instead of conventional wires minimising parasitic inductance and enhancing electrical performance. The designed integrated heatsink geometry is carefully optimized using simulation-guided thermal and airflow analysis to leverage the forced convection generated by the propeller's downwash, providing passive cooling enhancement without additional power overhead. The paper provides detailed insights on the modeling, thermal analysis, and drive cycle performance of the proposed integrated geometry to prove the effectiveness and scalability of the proposed solution for aerial vehicle powertrain applications.

5.5.2 Modelling and Design of the Integrated Geometry

The integrated heatsink geometry was designed based on the dimensions of the motor used in this case, but it can be adjusted to any dimensions. The heat is transferred from the motor to the heatsink via the attached designed heatsink geometry from the upper side. The integrated heatsink is attached to the motor via four screws that extends from the designed integrated heatsink geometry to the motor geometry. Similarly on the bottom side, the PCB is attached via small mounting screws. A thermal interface material is used between the heat-producing switches and the designed integrated heatsink geometry. The attachment of Motor and PCB with the designed integrated heatsink is shown in Figure 1b and 1c.

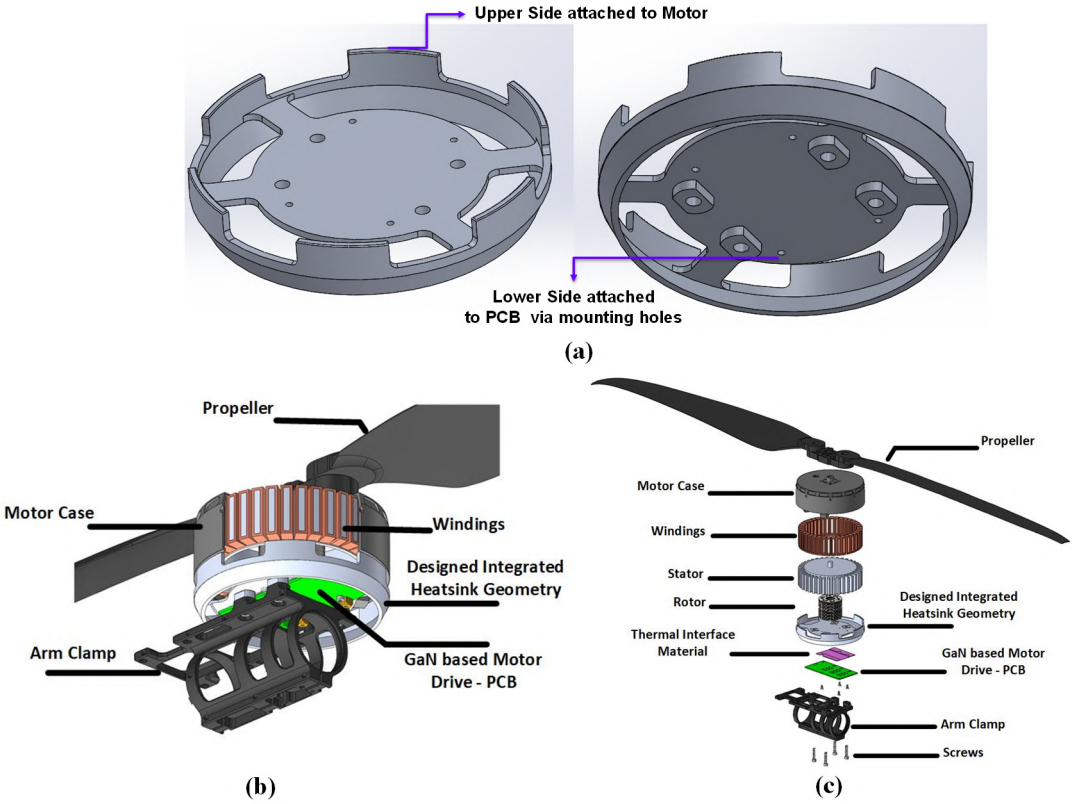


Figure 5.13: (a) Designed Integrated Geometry (b) Compact View- Integrated Motor and Motor Drive System (c) Exploded View- Integrated Motor and Motor Drive System

5.5.3 Thermal Results and Analysis

To evaluate the thermal performance of the designed integrated geometry, the motor drive operation at various load conditions and the full drive cycle under max load was analysed. Figure 2 and Figure 3 shows the results of thermal analysis, which depicts that after integration the design heatsink geometry is capable of cooling down both the motor and motor drive/motor controller. Figure 4 shows the path of airflow being created, as this is an aerial vehicles and the rotating propeller deflects the air downward onto the geometry, in addition to the surrounding atmospheric air, which plays a role in the overall system heat dissipation.

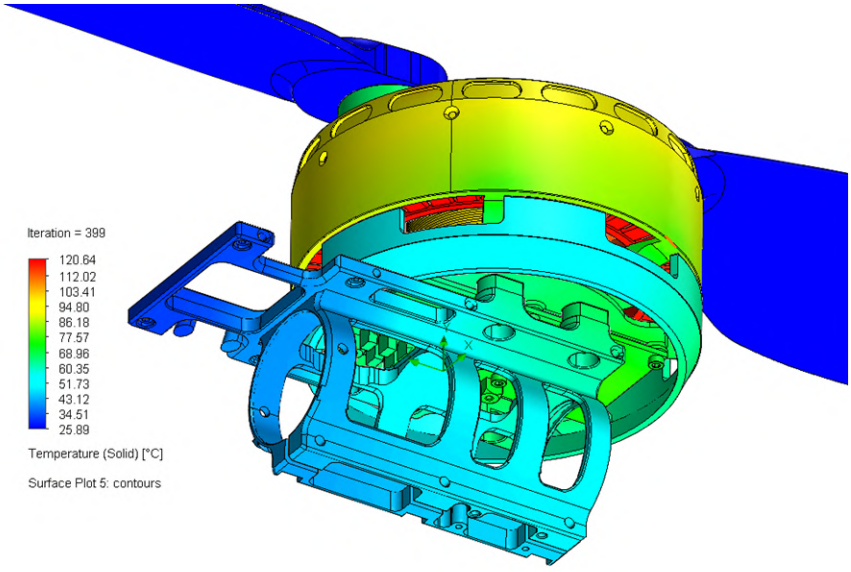


Figure 5.14: Thermal Analysis of the designed Integrated geometry for Motor and Motor Drive System

To analyse the performance of the designed geometry in detail, a full drive cycle simulation of the aerial vehicle was carried out, which includes the idle state, before flight, cruising altitude, and then descending altitude. As the power loss of the motor and motor drive continuously changes, which means the generated heat also keeps varying, the designed geometry must be able to dissipate the heat in all operating conditions.

In conclusion, the designed integrated geometry leads to the cooling of both motor and motor drive, increasing the power density, reducing cost, reducing parasitics, and increasing overall system efficiency. A detailed analysis of the designed geometry, along with the drive cycle operation, is presented to establish the superior performance of the designed geometry.

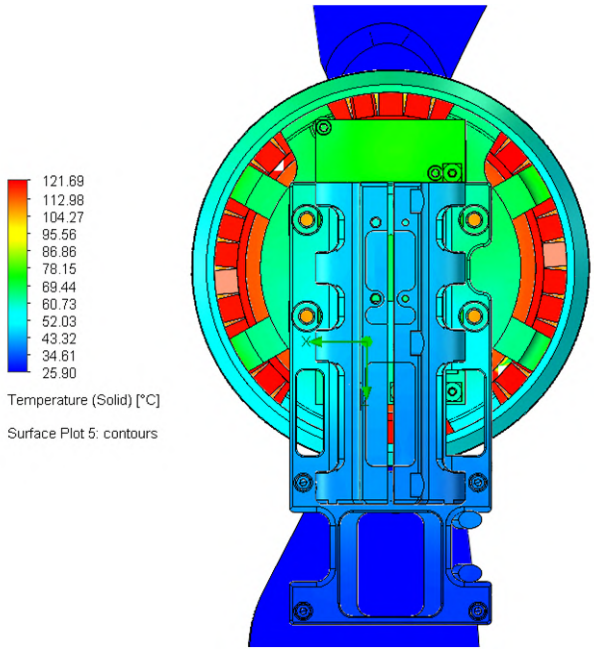


Figure 5.15: Bottom View- Thermal Analysis of the designed Integrated geometry for Motor and Motor Drive System

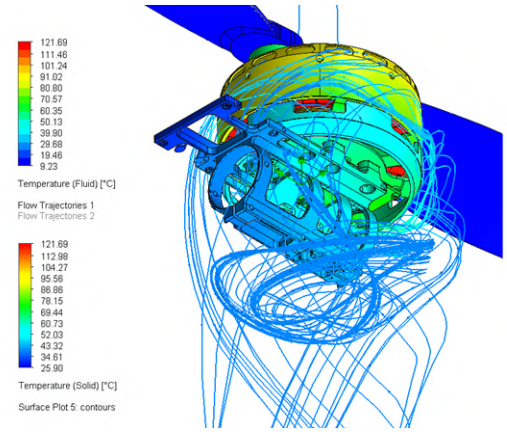


Figure 5.16: Air Profile of the designed Integrated geometry for Motor and Motor Drive System

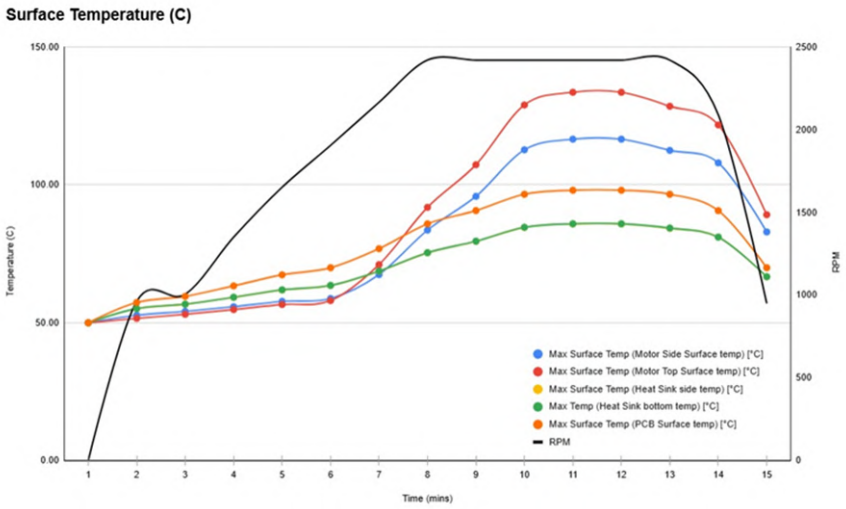


Figure 5.17: Full Drive Cycle Simulation and Thermal Analysis

CHAPTER 6

Conclusion

In conclusion, this dissertation focuses on the power converters optimization for electrified transportation applications through various approaches. At first, the high power density magnetics design which includes two approaches: a distributed magnetics approach and the preposition of a new Star shape three-phase inductor geometry. The distributed approach is especially discussed regarding the hybrid electric vehicles platform and also provides insights into design space optimization and multi-objective optimization. The Star inductor geometry contributes to an increased power density and magnetic performance for an interleaved converter in an electric vehicle. This research solved the problem of limited vertical space on the electric vehicle chassis for WPT power electronics by modeling and designing super planar-distributed magnetics with integrated PCB windings, considering the design space optimization constraints. A novel and more accurate high-fidelity model was derived instead of using the available and traditional magnetic equivalent circuit (MEC) models, which helped to model the magnetic component behavior accurately. Overall, this research treated and solved the power density problem as an optimization problem, considering every constraint involved, resulting in a significant 66% increase in power density. Moreover, the combination of a metal core and FR4 PCB was used based on the test data for optimal thermal performance. This research paves the way for developing a high-power-density WPT power electronics unit. It is also a step forward in distributed magnetics and automated magnetics design, an evolving research area for which the concept of explained design space optimization is essential.n this research, a very high power density three-phase interleaved boost converter was realized by designing a unique geometrical star shape inductor. Moreover, a new high-fidelity modeling approach was presented and validated as an alternative to the FEA analysis, which is a significant step forward in the domain of automated magnetics design.

Chapter 3 includes the new bare-die embedding technique to design highly efficient and high-power-density PCBs for EV applications. It includes the design process, design rules, design framework, and detailed analysis of the proposed technique which includes parasitic

analysis, power density comparison, thermal modeling and analysis, and efficiency comparison with the benchmark product. This proposed technique offers promising results and is a good candidate for designing future high-power power electronics for transportation applications. This research presented a bare die embedded packaging technique, along with the design rules, methodology, and manufacturing framework, which proved the superior performance and advantages. A thermal model for the proposed technique was presented and validated, along with the experimental results. A motor drive was designed using the proposed tech- nique and compared with the benchmark motor drive to justify better performance in terms of high power density, better thermal performance, low parasitics, higher efficiency, increased depth of integration, and extended driving range. Parasitic extraction, signal integrity anal ysis, and experimental comparison were done to illustrate the performance of the proposed technique. This work is the foundation to illustrate the potential of the newly proposed bare-die embedding technique, whose applications can be extended beyond small mobility and to high power level applications to accelerate the electrification revolution.This research presented a unique perspective and benefit of the newly proposed bare die embedded packaging technique and established its superior performance through signal integrity analysis, electromagnetic susceptibility analysis, and EMI analysis aided by experi- mental results and compared with traditional PCB design. A motor drive was designed using the proposed technique, and its EMC performance was compared with that of the bench- mark motor drive to justify better performance. This work is the foundation to illustrate the potential of the newly proposed bare-die embedding technique and discover its benefits from the EMC/EMI perspective, which will pave the way for its widespread adaptions to accelerate the electrification revolution.

Chapter 4 focuses on the development of a very compact and high power density on board charger for small mobility applications using a custom-designed planar flyback transformer having interleaved winding arrangements for low power loss profile ensuring better thermal performance. The integration of the OBC in the vehicle solves the problem of range anxiety and contributes towards the adoption of electric vehicles. In conclusion, this research focuses on developing a very low-footprint planar flyback transformer, which leads to the development of a high power density on-board charger. Due to the achieved high power density, it was integrated and packaged along with the motor drive circuit in the same case without occupying additional space, equipping the e-scooter with the onboard charging capability and contributing to the adaptation of electrified transportation.n this research, an RMRAC control architecture for a multi-winding flyback converter for small mobility OBC applications was implemented and evaluated. Hardware results prove that the presented control scheme performs better in terms of tracking errors, load changes, and reference changes,

ensuring high-quality voltage regulation and minimum cross- regulation.

In Chapter 5, a multi-paralleled GaN-based motor drive solution that achieves high power density and efficiency, for aerial vehicle applications was designed along with the presentation of an optimization framework for designing such high-power, sensitive devices based systems. The work also includes detailed considerations for layer stack design, EMI mitigation, PCB layout, and thermal management strategies. A method for parasitic parameter extraction is outlined, followed by its optimization using Double Pulse Testing (DPT), with results closely matching experimental data. Additionally, a comparative analysis against current state-of-the-art solutions highlights the proposed design's significant improvements in both power density and efficiency. Moreover, a unique heatsink geometry with a goal to integrate the motor and motor drive has been designed and the the performed thermal analysis over the drive cycle shows promising results, which paves the way to harness the integration benefits of motor and motor drive. For future work the multi-paralleled GaN approach can be applied to further increase the power level, and the integration concept can be improved and extended using novel and more efficient integrated heatsink geometries that offer better cooling and airflow, such as by utilizing fins or creating air pathways within the integrated heatsink geometry.

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