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THEORETICAL AND EXPERIMENTAL INVESTIGATION OF TRANSFERRED-ELECTRON AMPLIFIERS

by
Ashok Kumar Talwar

A dissertation submitted in partial fulfillment
of the requirements for the degree of
Doctor of Philosophy
(Electrical Engineering)
in The University of Michigan
1972

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LIST OF SYMBOLS

A	Area of cross section of the GaAs crystal.
A_a, A_b, A_c	Constants used in defining the relationship between I_{cond} and V.
a	A parameter defined in Eq. 2.12.
a_1, a_2	Parameters used in defining the relationship between v and E.
a_{11}	Value of a_1 near the cathode.
a_{12}	Value of a_1 near the anode.
a_{21}	Value of a_2 near the cathode.
a_{22}	Value of a_2 near the anode.
B	3-dB bandwidth.
B_a, B_b, B_c, B_d	Constants used in defining the relationship between v and E.
C_o	Low-field capacitance of the device.
C, C_1, C_2, C_3	Functions defined in Eqs. 2.30a through 2.30d.
D	Diffusion coefficient.
E	Electric field.
E_o	Static component of the electric field.
E_1	Electric field near the cathode.
E_{11}, E_{12}	Fundamental frequency components of the electric field.
E_2	Peak electric field in the domain.
E_3	Electric field near the anode.
E_n	Normalizing electric field used in the relationship between v and E.

E_{n1}	Value of E_n near the cathode.
E_{n2}	Value of E_n near the anode.
E_{RF}	Magnitude of the fundamental frequency component of the electric field.
E_{th}	Threshold electric field.
e	Magnitude of the electronic charge.
$F_1, F_2, \ldots, F_{12}$	Functions defined in Eqs. 2.18 through 2.29.
$F_{c1}, F_{c2}, \ldots, F_{c12}$	Correction terms for $F_1, F_2, \ldots, F_{12}$ when diffusion effects are included.
G	Power gain.
$G_1, G_2, \ldots, G_6$	Functions defined in Eqs. 2.34a through 2.34f.
I_{cond}	Conduction current.
I_{dis}	Displacement current.
I_k	Modified Bessel function of order k.
i	Index integer.
J	Total device current density.
J_o	Static (dc) component of the device current density.
J_{11}, J_{12}	Fundamental frequency components of the device current density.
J_d	Total diffusion current density.
J_{do}	Dc component of the diffusion current density.
J_{d11}, J_{d12}	Fundamental frequency components of the diffusion current density.
J_{DD}	Diffusion current density due to the gradient in the value of diffusion coefficient.
J_{DN}	Diffusion current density due to the gradient in mobile electron density.
J_{th}	Normalizing current density defined in Eq. 3.1.

k	Index integer.
L_a	Length of the passive region near the anode of the GaAs crystal.
L_n	Length of the active region of the GaAs crystal.
ℓ	Length of the GaAs crystal.
n	Mobile electron density.
n_o	Ionized donor density.
n_{o1}	Ionized donor density at the start of a gradient.
n_{o2}	Ionized donor density at the end of a gradient.
P	Constant used in the expression for D (Chapters II through VIII).
P	Constant used in defining the relation between domain width and excess domain voltage (Chapter IX).
P_{in}	Input signal power.
Q	Constant used in the expression for D (Chapters II through VIII).
Q	Constant used in defining the relationship between domain width and excess domain voltage.
R_d	Depletion ratio.
S	Constant used in defining the relationship between domain width and excess domain voltage.
S_1, S_2, S_3	Functions defined in Eqs. 2.30e through 2.30g.
T_1	Lattice temperature near the cathode.
T_2	Lattice temperature near the anode.
t	Time.
V	Total voltage across the diode.
V_o	Bias voltage.
V_1	Fundamental frequency component of the voltage across the diode.

V_2	Second-harmonic frequency component of the voltage across the diode.
V_B	Dc component of the voltage across the diode.
V_D	Excess domain voltage.
V_{Do}	Initial excess domain voltage.
V_S	Domain sustaining voltage.
V_{TH}	Threshold voltage.
v	Average electron drift velocity.
v_A	Velocity of the accumulation layer.
v_s	Average mobile electron velocity at high electric field.
v_{th}	Average mobile electron velocity at threshold electric field.
W	Width of the domain.
W_D	Width of the depletion layer.
X_1	Distance from the cathode where a gradient in donor density starts.
X_2	Distance from the cathode where a gradient in donor density ends.
x	Distance from the cathode.
Z_d	Diode impedance.
Z_L	Load impedance.
z	A parameter used in Eq. 2.14.
α	A parameter used in Eq. 2.14.
ϵ	Dielectric constant of the GaAs material.
θ	Phase defined in Eq. 9.22.
λ	Wavelength.
μ_o	The electron mobility in GaAs at low electric fields.

μ_n	Negative differential mobility.
σ	Conductivity of the GaAs material at low electric fields.
τ_p	Low-field dielectric relaxation time.
φ	A parameter defined in Eq. 2.11.
ω	Fundamental angular frequency.

CHAPTER I. INTRODUCTION

1.1 Microwave Amplification Using Transferred-Electron Devices

In 1961 Ridley and Watkins[1] predicted the possibility of negative differential resistance based on the mechanism of field-induced carrier transfer from a high-mobility conduction band to low-mobility satellite valleys. This mechanism is called the transferred-electron effect. Ridley[2] showed that the effect would lead to traveling high-field domains nucleating periodically at the cathode and disappearing at the anode. Hilsum[3] predicted that such an effect would occur in GaAs.

The first experimental evidence of this was found by Gunn[4,5] in 1963. He reported that when a dc voltage is applied to a bar of n-type GaAs or InP, the current first increases linearly with voltage and then oscillates when the average electric field reaches a certain critical value of several kilovolts per centimeter. The time period of these oscillations was found to be approximately equal to that of the transit time of the carriers from the cathode to the anode. Later he showed[6,7] the existence of traveling domains by direct probe measurements. Hutson et al.[8] and Shyam et al.[9] verified experimentally that the mechanism of carrier transfer proposed by Ridley and Watkins and Hilsum was responsible for the oscillations observed by Gunn.

Microwave amplification in transferred-electron (TE) devices was first observed by Thim et al.[10] They employed GaAs diodes with $n_o \ell$ product (n_o = ionized donor density, ℓ = length of the active region of the GaAs sample) below $10^{12}/cm^2$ in order to prevent domain formation. The

negative conductance at RF frequencies resulting from the transferred-electron effect was utilized to obtain microwave amplification in a reflection-type circuit. Oscillation was prevented by a proper choice of the circuit impedance. Such amplifiers are now referred to as the low $n_o \ell$ type or the subcritical type (i.e., $n_o \ell < 10^{12}/cm^2$).

Other methods of amplification using the transferred-electron effect have since been discovered. Robson et al.[11] and Kino and Fay[12,13] have studied amplification in high-resistivity GaAs of subcritical $n_o \ell$ product to get unilateral, wide bandwidth amplification. Since the amplifier is a two-port device, amplification can be described more conveniently as utilizing the growth of the slow-space-charge wave in the material when it is biased in the region of negative differential mobility. Thim[14,15] utilized the negative differential conductance present simultaneously with propagating domains in supercritically doped ($n_o \ell > 10^{12}/cm^2$) GaAs diodes to obtain microwave amplification. In addition, parametric amplification has been obtained by Aitchison et al.[16,17] by using the domain capacitance as the variable parameter. Large-signal microwave amplification has been achieved by locking[18-20] of a transferred-electron oscillator. Such operation is usable when linearity and stability at zero input power is not required. More recently, circuit stabilization of supercritically doped TE devices has been demonstrated.[21-24] Linear amplification over wide bandwidths has been achieved with such devices.

The present study is an investigation of stabilized TE amplifiers and of the delayed-domain mode of operation. The next section presents a brief description of the various modes of amplification mentioned here. This is followed by an outline of the present study.

1.2 Description of the Various Modes of Microwave Amplification in Transferred-Electron Devices

1.2.1 One-Port Stable Amplifiers. If the $n_o \ell$ product of a GaAs diode is less than $10^{12}/cm^2$, traveling domains are not usually formed in the diode when it is biased above the threshold for negative differential mobility. Instead, a static space-charge accumulation occurs. The accumulation is caused by the slowing down of the charge carriers as the electric field goes above the threshold value. The electric field increases monotonically from the cathode to the anode where it falls rapidly to zero because of the high conductivity of the anode contact. Because of the space-charge accumulation, the relation between current and bias voltage is not the same as the relation between carrier velocity and electric field. In fact, in accordance with Shockley's[25] positive conductance theorem, the diode does not exhibit a static negative resistance. The excess space-charge density (i.e., electron density in excess of the ionized donor density) increases with increasing bias voltage by an amount so large, that the current increases for an increase in voltage, even though there is a decrease in electron velocity throughout most of the crystal.

Despite the static positive resistance of subcritical GaAs diodes, the material does support growing space-charge waves because of the negative differential mobility. As a result, the diodes exhibit negative conductance for frequencies corresponding to electron transit angles[26-28] around 2π, 4π, 6π, etc. If placed in a lightly loaded resonant circuit, such a diode can oscillate because of its negative conductance. This happens when the

total diode and circuit susceptance is zero, and when the magnitude of the diode negative conductance is equal to or greater than the positive conductance of the circuit. However, if the load conductance is larger than the magnitude of the device negative conductance at all frequencies, the device is stable, and stable amplification can be obtained in a reflection-type circuit.

Thim et al.[10,29] demonstrated such negative conductance microwave amplification with n-type GaAs wafers 50 to 100 μm thick and mounted at the end of a coaxial line of 50-Ω characteristic impedance. A broad bandwidth circulator separated the input signal from the reflected wave. The GaAs materials used had resistivities of 40 Ω-cm and 80 Ω-cm which enabled the $n_o \ell$ product to be below the critical value for domain formation. Gain was obtained over S-band (i.e., 2 to 4 GHz). A crystal of 45-μm thickness showed gain near 10 GHz, a frequency that would correspond to a transit angle of approximately 8π. Foyt and Quist[30] also made somewhat similar observations using pulsed bias with a diode of $n_o \ell \simeq 5 \times 10^{10}/cm^2$ and pointed out the continued increase in current with increase in bias voltage beyond the threshold value. This behavior is different from that of a diode of high $n_o \ell$ product (i.e., $n_o \ell > 2 \times 10^{12}/cm^2$) where the current drops as domain formation occurs above the threshold voltage.

Hakki and Knight[31] experimented with diodes of different $n_o \ell$ products and found that negative-resistance amplification could be achieved for an $n_o \ell$ product in the range $2 \times 10^{10}/cm^2$ to $2 \times 10^{12}/cm^2$. For $n_o \ell \gtrsim 2 \times 10^{12}/cm^2$ the operation was found to be almost invariably in the dipole-domain mode. Kroemer[32] explained that for $n_o \ell$ product values below $2 \times 10^{10}/cm^2$, negative conductance is not observed because

of parasitic series resistance, even though a theoretical analysis which is "reasonably free from questionable assumptions" would predict negative conductance at such values of $n_o \ell$ product.

Thim[33] investigated the microwave-gain characteristics of bulk GaAs amplifiers experimentally as a function of temperature. The resistivity of the material he chose was strongly dependent on temperature and he interpreted the results in terms of changing carrier concentration assuming a constant mobility. He found the upper and lower limits of $n_o \ell$ product for stable negative conductance operation to be $5 \times 10^{11}/cm^2$ and $8 \times 10^{10}/cm^2$, respectively. He further found that (1) the frequency of the negative conductance region decreases with increasing bias field at a fixed temperature; (2) the magnitude of gain first increases with field, reaches a maximum and then decreases again at a fixed temperature; (3) the frequency of the negative conductance region decreases with decreasing temperature (and carrier density) at a fixed bias field and (4) at a fixed bias field, the magnitude of gain decreases with decreasing temperature. These results may not be very general since the range of variation in carrier density achieved was limited. As an example, even though result 3 was confirmed by Thim using the model of McCumber and Chynoweth,[26] Wang's[34] calculations show that the frequency of negative conductance at first increases and then decreases with carrier density.

Hayes,[35] like Thim,[33] varied the $n_o \ell$ product by varying the temperature of the diodes made of a material that showed a strong resistivity dependence on temperature. He found that there is an optimum range of applied voltages and $n_o \ell$ products to achieve maximum saturation power and

efficiency. The maximum efficiency observed was 4 percent. He also found that the stable reflection amplifiers can be operated as linear amplifiers to about half of their saturation power.

Supercritically doped devices do not, in general, lend themselves to stable negative conductance amplification. It is difficult to suppress domains in them, except under special conditions, such as by loading the GaAs material surface by dielectric[36-39] or ferrimagnetic[40] materials, or by using small transverse dimensions.[41] Gueret[42] has shown that the two-stream interaction between an active GaAs diode and a passive, biased semiconductor can reduce the space-charge wave growth and thereby inhibit domain formation. Narayan and Sterzer[43] discussed the possibility of stabilization by circuit loading the device heavily. More recently, circuit stabilization of supercritically doped devices has been achieved experimentally.[21-24,44-47]

Thim and Lehner[47] achieved stable and linear amplification in frequency ranges around 27 GHz and 50 GHz using n-GaAs wafers 5 μm thick. The $n_o \ell$ product was $2.5 \times 10^{12}/cm^2$. They attributed the stabilization of these somewhat high $n_o \ell$ product diodes to doping gradients and to a drop in mobility caused by heating.

Walsh et al.[21] were able to stabilize devices with $n_o \ell$ product as high as $4 \times 10^{12}/cm^2$ and obtained linear amplification with peak power output of 1 W at a gain of 10 dB in C-band (i.e., 4 to 6 GHz). Perlman et al.[46] constructed single-stage amplifiers with small-signal gains between 6 and 8 dB and instantaneous bandwidths in excess of 4 GHz for frequencies from 4 GHz to above 16 GHz. They obtained saturated power

outputs in excess of 0.5 W and reported a maximum efficiency of approximately 3 percent. In addition to the heavy circuit loading, the stabilization was aided by the reduction of negative differential mobility caused by heating in CW devices. Operation at high bias voltages was also found to aid stabilization.

Magarshack and Mircea[24] obtained linear gain over the frequency range of 7 GHz to 12 GHz using a diode 10 μm long and a donor density of $2 \times 10^{15}/cm^3$ ($n_o \ell = 2 \times 10^{12}/cm^2$). The diode was mounted at the end of a 50-Ω line and was biased to approximately two times the threshold voltage. They have made a small-signal analysis with the diffusion coefficient taken to be independent of the electric field and have found that a bandwidth of many octaves (L-band through 40 GHz) is possible with samples 5 μm thick and with $n_o \ell = 1.2 \times 10^{12}/cm^2$.

Magarshack and Mircea[44] have also studied the effect of diffusion on stability and have obtained a field distribution where a static field domain is "frozen" at the anode. The field outside the domain is below threshold, so that the steady current density is below the peak current density J_{th} where

$$J_{th} = n_o e v_{th},$$

n_o = the ionized donor density,

v_{th} = the peak electron velocity and

e = the magnitude of electronic charge.

They have found that diffusion effects are responsible for such a stable field configuration and thus should explain the stabilization of supercritically doped TE devices. However, they have neglected the field dependence of diffusion. This is an important component. Jeppesen and Jeppsson[48] have shown that the form of field dependence assumed can completely change the static field solution.

The dc and RF characteristics of supercritically doped, stabilized devices observed experimentally[46] are similar in many ways to the characteristics calculated for subcritically doped devices.[28,49] In fact, whatever the mechanism used for stabilization, the result is that of increasing the critical value, or value of $n_o \ell$ product for which domains form, to above the usual limit. Even though such devices have been referred to as "supercritically doped" in published literature, the devices are still, strictly speaking, subcritically doped under the special conditions of operation; because domain formation does not occur.

Several theoretical studies have been made of the behavior of stable TE devices. McCumber and Chynoweth[26] start with the two-valley model of Ridley and Watkins[1] and Hilsum.[3] The relative population of two valleys of vastly different mobility and density of states is determined by the average electron temperature which is contained in the energy transport equation. The equations were programmed for numerical solution on a digital computer. Steady state, as well as small-signal RF characteristics were obtained for subcritically doped devices. The critical value of $n_o \ell$ product for domain formation was found to be $2.7 \times 10^{11}/cm^2$.

Several other small-signal studies with different simplifying assumptions were made. Engelmann and Quate[50] assumed a model for carrier density in the main conduction band valley as a function of electric field. The mobility was considered field independent and was assumed nonzero only in the main valley. They neglected diffusion effects. Analyses of Mahrous and Robson,[51] and McWhorter and Foyt[52] assumed a

piecewise linear velocity-field characteristic and also neglected diffusion. Hakki[27] included electron diffusion effects but neglected static space charge and assumed a uniform dc field. Holmstrom[53] took the spatial field inhomogeneity into account but neglected diffusion. Hanson[54] did a nonisothermal analysis to extend the validity of the theory to frequencies above 30 GHz. The static field was assumed uniform.

The results of the small-signal analyses mentioned previously are qualitatively similar and largely agree with experimental observations. These theories have provided a good understanding of the small-signal behavior of these devices under conditions of uniform doping and lattice temperature.

Large-signal computer simulation of subcritically doped TE devices has been done by Yu et al.[55] Their computer program is similar to that of McCumber and Chynoweth.[28] They have found RF current waveforms for a given dc and RF voltage across the device, and device impedance has been calculated by Fourier analysis of these waveforms. They have shown that the efficiency can be improved greatly through controlled carrier injection which enables elimination of the passive cathode region. In one case the efficiency was shown to improve theoretically from a maximum of 1.7 percent to 16.5 percent. Experimentally, they have reported a maximum efficiency of 6.5 percent at 1.6 GHz using a controlled carrier injection diode.

Hariu et al.[56] have made calculations of the negative conductance of TE devices with a depleted Schottky-barrier contact and have shown that the negative conductance extends over at least several octaves.

Thim[57] has made calculations of the effect of field uniformity on amplifier noise and estimates a noise figure of 8 dB for samples with

injection-limited cathodes. Noise figures of 4 dB or less were predicted for materials with large negative differential mobility such as $In_{0.2}Ga_{0.8}Sb$.

From this discussion it is seen that stable and linear TE amplifiers with large gain-bandwidth products have been achieved. These devices show promise of extremely wideband, low-noise, linear microwave amplification. Presently, their dc to RF conversion efficiency has been low due to the large static field distortion. This problem can be remedied, at least in part, by using injection-limited diodes,[55] and by controlling the geometric or doping profile as well as by an understanding of lattice temperature gradients.[58,59] Potentially, these devices should have fairly good efficiencies.

1.2.2 Unilateral, Two-Port Stable Amplification. Robson et al.[11] and Kino and Fay[12,13] obtained unilateral, two-port amplification in long GaAs samples. The material must be of high resistivity in order that the $n_o l$ product be below $10^{12}/cm^2$, while keeping l large enough so that the two ends of the device are well separated. The samples are biased above the threshold for negative differential mobility but below the bias for which the negative conductance becomes large enough for oscillation. The input signal is applied at the cathode end of the sample. The slow space-charge wave grows as it travels along the sample because of negative differential mobility,[50] and the amplified signal is coupled out at the anode end. Such devices are called traveling-wave amplifiers. These amplifiers are broadband since electron transit-time effects are not important. The bandwidth is limited on the lower frequency side by the finite transverse dimensions.[60] The gain is considerably reduced when

$\omega a/v_o$ approaches unity or less.[60] Here ω is the frequency in rad/s, a is one half of the smallest transverse dimension and v_o is the drift velocity. The upper limit of frequency (and bandwidth) is imposed by diffusion effects.[13,61] Kino and Fay[13] have computed this limit to be 2 GHz for 1000 Ω-cm material and 6 GHz for 100 Ω-cm material.

Dean et al.[62] have obtained CW amplification in the X-band with 1-μm n-type epitaxial GaAs on a semi-insulating substrate. A maximum gain of 13 dB at 11.5 GHz was reported. The isolation was 20 dB to 30 dB.

These amplifiers have a number of attractive features. Unlike the reflection-type amplifiers discussed in Section 1.2.1, these are nonreciprocal and have significant reverse loss. They do not require a circulator and can be used to provide variable phase shift with constant gain.[62] However, coupler loss is a limitation which not only lowers the net gain but also increases the noise figure.[61,62] Because of the large lengths and high resistivity required for the GaAs samples, the transverse dimensions have to be large for significant power outputs. This is likely to add to the problem of efficient coupling. In addition, large GaAs samples of relatively uniform quality are required for those devices. The limit on resistivity may be reduced somewhat[12] by using metal-backed dielectric in the vicinity of the GaAs sample in order to inhibit domain formation.

1.2.3 Traveling-Domain Amplifiers. When a high $n_o l$ product GaAs sample is biased above threshold for negative differential mobility, high-field domains are usually generated near the cathode and travel toward the anode. If the externally applied voltage is gradually increased while a domain is in transit, the current decreases until the high field in the

domain reaches a certain maximum value.[39-41] Thus the device exhibits negative conductance simultaneously with oscillation in the domain mode. Thim[14,15] has used this negative conductance to obtain microwave amplification. This negative conductance is not sensitive to electron transit angles and is thus wideband. However, there is an upper limit to the frequency which is determined by the time the domain takes to readjust itself after a change of external voltage. Thim[15] has derived an upper limit for $f\ell$ product of approximately 10^8 cm/s (e.g., an upper limit of 10 GHz for a 100-μm long sample). Such amplification is not restricted to the transit-time mode, but may also be obtained in the quenched-domain mode.[63] Thim has reported[14] gain of 3 dB from 5.5 GHz to 6.5 GHz. He has obtained a maximum of 100 mW CW RF power output and 60 mW output with 9 dB gain at 6 GHz. The efficiency at 100 mW output was 2.5 percent. The circuit for such an amplifier has to provide both a short circuit at the Gunn oscillation frequency and a broadband circuit at the signal frequency. The amplifier will have to be operated at frequencies sufficiently removed from the Gunn oscillation frequency to avoid its AM and FM noise sidebands, if noise is a consideration.

1.2.4 Parametric Amplifier. Since a domain consists of a charge accumulation and a charge depletion layer, it can be regarded as a capacitor. The Gunn diode then becomes a capacitor in series with a resistor representing loss within the sample. When the domain is collected at the anode and before a new domain is formed, the capacitor can be assumed to have become infinite. The domain elastance thus varies between a nonzero and a zero value and the Gunn diode behaves as a capacitor pumped at the frequency corresponding to the domain transit time. Aitchison

proposed[16] the possibility of parametric amplification using a Gunn diode. Aitchison et al.[17] constructed a degenerate parametric amplifier in which the idler current was supported by the resonance provided by the inductance of the circuit and the mean capacitance of the Gunn sample. The injected signal frequency, approximately 6 GHz, was one half the frequency of Gunn oscillation, approximately 12 GHz. Small-signal gain of 20 dB and a 3-dB bandwidth of 10 MHz was reported, giving a $(\text{gain})^{1/2}$-bandwidth product of 100 MHz. It is difficult to distinguish between parametric and negative conductance amplification in such devices. These amplifiers will have limited bandwidth and will have to be operated in relatively complicated circuits.

1.2.5 Large-Signal Amplification by Locking of Transferred-Electron Oscillators. Locking of TE oscillators was demonstrated by Hakki et al.[64] and later by Judd and Hewitt.[65] It has been recognized as an attractive way of attaining large power outputs from TE devices,[18,66] and large-signal amplification has been achieved.[18-20] Fleri and Socci[67] have studied the amplification of a frequency-modulated signal using this method. In such amplifiers, the device is allowed to oscillate in a high $n_o l$ product or a low $n_o l$ product mode, and then the signal to be amplified is injected. If the frequency difference between the injected signal and the oscillator is less than Δf, given by the expression[68]

$$\Delta f = \frac{\eta f_o}{2} \sqrt{\frac{P_L}{P_o}} , \tag{1.1}$$

the oscillator locks to the injected signal. In this expression f_o is the oscillator frequency, P_o is the power output of the oscillator

and P_L is the power of the injected signal. η is nearly a constant for a given device and circuit.[68]

For a given locking efficiency, a large RF input level leads to a larger bandwidth and the total tuning range of the amplifier will, in general, be greater than that of the oscillator. This has been demonstrated.[20] It is found that[18,20] the total output of the locked oscillator is nearly equal to the sum of the oscillator and input power. When locking occurs there is no appreciable change in the dc power dissipated in the device.[20] Thus the efficiency of such amplifiers is nearly the same as that of the oscillator. In general, if P_L/P_o is not large, locking does not alter the mode of operation of the device. Any mode of oscillation can be used for such devices. Thim[69] has made a computer study of various oscillating modes and has reported the following values of efficiency:

1. Transit-time and quenched single-domain modes:

$$n_o l > 10^{12}/cm^2 , \quad fl \sim 10^7 \text{ cm/s} ,$$

Efficiency = 9 percent maximum.

2. Quenched multiple-domain and LSA modes:

$$n_o l > 10^{12}/cm^2 , \quad fl > 2 \times 10^7 \text{ cm/s} ,$$

Best LSA Efficiency = 18 percent.

3. Low $n_o l$ oscillator mode:

$$n_o l < 10^{12}/cm^2 , \quad fl \sim 10^7 \text{ cm/s} ,$$

Efficiency nearly 5 percent.

4. Inhibited, or delayed-domain mode:

$$n_o \ell > 10^{12}/cm^2 , \quad f\ell < 10^7 \text{ cm/s} ,$$

Efficiency = 27 percent maximum.

Efficiencies of over 30 percent have recently been reported in what appears to be the inhibited mode[70] (utilizing second-harmonic voltage). The inhibited mode seems to be very attractive for high-efficiency, large-signal amplifiers.

1.3 Scope of the Present Study

This study is an attempt to understand the behavior and potential of transferred-electron amplifiers. Both subcritically doped as well as supercritically doped devices are considered.

A large-signal analysis of subcritically doped, negative conductance-type devices is developed in Chapter II. The analysis is one-dimensional and includes the effects of diffusion, where the diffusion coefficient is dependent upon the electric field. First-order nonlinear equations involving the dc and RF electric fields in the material are obtained for given dc and RF currents driven through the diode.

The equations developed in Chapter II were solved on a digital computer and the results are presented in Chapters III through VII. Various dc and RF characteristics of the diodes are examined. The effects of diffusion, bandwidth considerations, the effects of bias, temperature effects and the effects of doping density are discussed.

The experimental study of stable negative conductance amplifiers is presented in Chapter VIII. Some of the important results of previous

chapters are confirmed. In order to understand and assess the potential of the delayed-domain mode, the domain collection process was examined and this analysis is given in Chapter IX. Using this analysis a model of the delayed-domain mode was developed; the results are presented in the same chapter.

CHAPTER II. LARGE-SIGNAL ANALYSIS OF STABILIZED TRANSFERRED-ELECTRON DEVICES

2.1 Introduction

A one-dimensional, large-signal analysis of subcritically doped transferred-electron devices, or stabilized, supercritically doped devices is developed in this chapter. Starting with Poisson's equation, the expression for total current and the velocity-field relationship appropriate to the lattice temperature, a system of first-order, nonlinear differential equations is obtained which determines the dc and RF electric fields inside the crystal as a function of the dc and RF cathode currents. Harmonics of the RF electric field and effects of diffusion are neglected in order to simplify the problem. However, harmonic currents, which result directly from the nonlinearity of the equations, are included. The lack of harmonic voltages and the presence of harmonic currents simulates diode operation in a simple parallel resonant circuit.

The equations may be solved numerically for dc and RF electric fields as a function of distance and time, progressing from the cathode contact with given boundary conditions. Integration of the electric-field quantities over the length of the crystal yields the total dc and RF voltages across the device. If the currents and the voltages are known, it is possible to calculate the impedance, dc power, RF power and the efficiency of a TE device.

In Section 2.3 the effect of field-dependent diffusion is discussed. A piecewise linear dependence is assumed for the diffusion coefficient as

a function of the electric field and expressions for the dc and fundamental frequency diffusion currents are obtained. Section 2.4 discusses the modifications required in the working equations when nonuniformly doped materials are considered.

2.2 A Diffusion-Free Analysis

The one-dimensional Poisson equation and the expression for total current density are, respectively,

$$\frac{\partial E}{\partial x} = \frac{e(n - n_o)}{\epsilon} \tag{2.1}$$

and

$$J = nev + \epsilon \frac{\partial E}{\partial t} , \tag{2.2}$$

where x = the distance from the cathode or negative contact,

n = the mobile electron density,

n_o = the ionized donor density,

ϵ = the dielectric constant of GaAs material (the relative dielectric constant is taken here to be 12.5) and

e = the magnitude of the electronic charge.

The diffusion current is presently not included. The positive direction of J and E is toward the cathode, while v, the average electron drift velocity, is directed toward the anode. The drift velocity is considered to be an instantaneous function of the electric field. This assumes that the intervalley scattering time between the upper and lower conduction band valleys of GaAs is much smaller than the time period of frequencies of interest. For practical purposes, this assumption may be considered reasonable up to a frequency[71] of approximately 30 GHz.

The v-E relationships theoretically derived by Ruch and Fawcett[72] are approximated by an analytical expression. For a large-signal analysis, it is desirable to use a single, analytical expression relating the average carrier velocity and electric field covering the whole range of electric-field values of interest. The following form is assumed:

$$v = a_2 \left[\left(\frac{E}{E_n} - a_1 \right) \exp\left(- \frac{E}{E_n} \right) + a_1 \right] . \qquad (2.3)$$

The constants a_1, a_2 and E_n have been evaluated for crystal lattice temperatures of 300°K, 375°K and 500°K by approximating the theoretical results of Ruch and Fawcett.[72] The values of these constants are as follows:

At 300°K, $a_1 = 0.19$, $a_2 = 3.95 \times 10^7$ cm/s, $E_n = 2.9$ kV/cm.

At 375°K, $a_1 = 0.235$, $a_2 = 3.05 \times 10^7$ cm/s, $E_n = 3$ kV/cm.

At 500°K, $a_1 = 0.345$, $a_2 = 1.972 \times 10^7$ cm/s, $E_n = 3.2$ kV/cm.

A comparison between Eq. 2.3 and the theoretical curves of Ruch and Fawcett is shown in Fig. 2.1. The agreement with the curves of Ruch and Fawcett is quite good except near the threshold field. In most practical devices operated at large-signal levels, the electric field stays well above the threshold value throughout most of the crystal and therefore the discrepancy near the threshold electric field is not expected to affect the results appreciably.

Substituting for n in Eq. 2.2 from Poisson's equation (Eq. 2.1) gives

$$J = \epsilon v \frac{\partial E}{\partial x} + \epsilon \frac{\partial E}{\partial t} + n_o e v . \qquad (2.4)$$

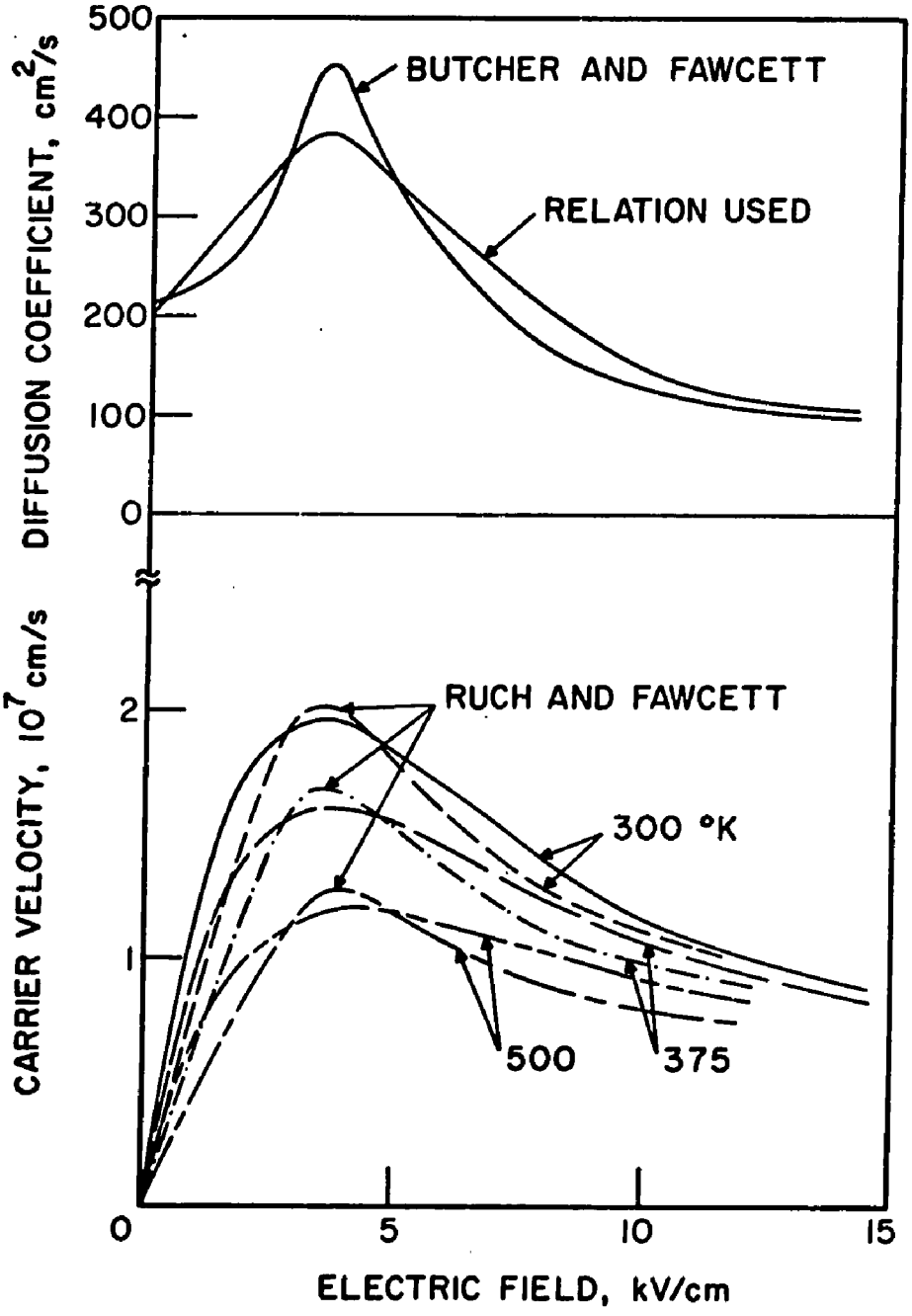


FIG. 2.1 DIFFUSION COEFFICIENT AND VELOCITY VS. ELECTRIC FIELD.

Substituting for v from Eq. 2.3 into Eq. 2.4 results in

$$J = a_2 \epsilon \left[\left(\frac{E}{E_n} - a_1 \right) \exp\left(-E/E_n\right) + a_1 \right] \frac{\partial E}{\partial x} + \epsilon \frac{\partial E}{\partial t} + n_o e a_2 \cdot \left[\left(\frac{E}{E_n} - a_1 \right) \exp\left(-E/E_n\right) + a_1 \right] \quad . \quad (2.5)$$

The following form of electric field is assumed:

$$E = E_o + E_{11} \cos \omega t + E_{12} \sin \omega t \quad , \quad (2.6)$$

where all frequencies above the fundamental are neglected. This is a simplifying assumption. E_o, E_{11} and E_{12} are all functions of the distance x.

Substituting the expression for E into Eq. 2.5 and rearranging gives the following expression for the total current density:

$$J = a_1 a_2 \epsilon \frac{\partial E_o}{\partial x} + a_1 a_2 n_o e + a_1 a_2 \epsilon \frac{\partial E_{11}}{\partial x} \cos \omega t + a_1 a_2 \epsilon \frac{\partial E_{12}}{\partial x} \sin \omega t$$

$$- \omega \epsilon E_{11} \sin \omega t + \omega \epsilon E_{12} \cos \omega t + \exp\left(-E_o/E_n\right) \exp\left[-\left(E_{11}/E_n\right) \cos \omega t\right]$$

$$\cdot \exp\left[-\left(E_{12}/E_n\right) \sin \omega t\right] \left[\frac{a_2 \epsilon}{E_n} \left(E_o + E_{11} \cos \omega t + E_{12} \sin \omega t\right) \right.$$

$$\cdot \left(\frac{\partial E_o}{\partial x} + \frac{\partial E_{11}}{\partial x} \cos \omega t + \frac{\partial E_{12}}{\partial x} \sin \omega t \right) - a_1 a_2 \epsilon \left(\frac{\partial E_o}{\partial x} + \frac{\partial E_{11}}{\partial x} \cos \omega t + \frac{\partial E_{12}}{\partial x} \sin \omega t \right)$$

$$\left. + \frac{n_o e a_2}{E_n} \left(E_o + E_{11} \cos \omega t + E_{12} \sin \omega t\right) - a_1 a_2 n_o e \right] \quad . \quad (2.7)$$

This expression contains dc, fundamental frequency and harmonic currents and may be written as

$$J = J_o + J_{11} \cos \omega t + J_{12} \sin \omega t + J_{21} \cos 2\omega t + J_{22} \sin 2\omega t + \ldots \quad , \tag{2.8}$$

where J_o, J_{11}, J_{12}, etc., are independent of time but involve the first derivatives with respect to x of E_o, E_{11} and E_{12} and powers of E_o, E_{11} and E_{12}. J_o, J_{11}, J_{12}, etc., must be independent of x by the condition of continuity of current. In order to determine the current amplitudes, J_o, J_{11}, J_{12}, etc., an expansion of the product of exponentials in Eq. 2.7 is necessary.

Designate

$$E_{11}/E_n = a \cos \varphi \tag{2.9}$$

and

$$E_{12}/E_n = a \sin \varphi \quad , \tag{2.10}$$

then it is seen that

$$\varphi = \tan^{-1} (E_{12}/E_{11}) \quad , \tag{2.11}$$

$$a = \sqrt{(E_{11}/E_n)^2 + (E_{12}/E_n)^2} \tag{2.12}$$

and

$$\exp [-(E_{11}/E_n) \cos \omega t] \exp [-(E_{12}/E_n) \sin \omega t] = \exp [-a \cos (\omega t - \varphi)] \quad . \tag{2.13}$$

The following identity[73] is then used to evaluate the various harmonics in Eq. 2.13:

$$\exp(z\cos\alpha) = I_o(z) + 2\sum_{k=1}^{\infty} I_k(z)\cos(k\alpha) \quad , \tag{2.14}$$

where I_k is a modified Bessel function of order k.

After substituting this series into Eq. 2.7 and rearranging terms, the amplitudes of dc and fundamental currents can then be written as

$$J_o = F_1 \frac{\partial E_o}{\partial x} + F_2 \frac{\partial E_{11}}{\partial x} + F_3 \frac{\partial E_{12}}{\partial x} + F_4 \quad , \tag{2.15}$$

$$J_{11} = F_5 \frac{\partial E_o}{\partial x} + F_6 \frac{\partial E_{11}}{\partial x} + F_7 \frac{\partial E_{12}}{\partial x} + F_8 \tag{2.16}$$

and

$$J_{12} = F_9 \frac{\partial E_o}{\partial x} + F_{10} \frac{\partial E_{11}}{\partial x} + F_{11} \frac{\partial E_{12}}{\partial x} + F_{12} \quad , \tag{2.17}$$

where

$$F_1 = \epsilon\left\{a_1 a_2 + a_2 \exp(-E_o/E_n)\left[C\left(\frac{E_o}{E_n} - a_1\right) + \frac{1}{2}\left(C_1 \frac{E_{11}}{E_n} + S_1 \frac{E_{12}}{E_n}\right)\right]\right\} \quad , \tag{2.18}$$

$$F_2 = \frac{a_2}{2}\epsilon \exp(-E_o/E_n)\left[\frac{E_{11}}{E_n}\left(C + \frac{C_2}{2}\right) + C_1\left(\frac{E_o}{E_n} - a_1\right) + \frac{S_2}{2}\frac{E_{12}}{E_n}\right] \quad , \tag{2.19}$$

$$F_3 = \frac{a_2}{2}\epsilon \exp(-E_o/E_n)\left[\frac{E_{12}}{E_n}\left(C - \frac{C_2}{2}\right) + S_1\left(\frac{E_o}{E_n} - a_1\right) + \frac{S_2}{2}\frac{E_{11}}{E_n}\right] \quad , \tag{2.20}$$

$$F_4 = n_o e\, a_2\left\{a_1 + \exp(-E_o/E_n)\left[C\left(\frac{E_o}{E_n} - a_1\right) + \frac{1}{2}\left(C_1 \frac{E_{11}}{E_n} + S_1 \frac{E_{12}}{E_n}\right)\right]\right\} \quad , \tag{2.21}$$

$$F_5 = a_2 \epsilon \exp(-E_o/E_n)\left[C\frac{E_{11}}{E_n} + C_1\left(\frac{E_o}{E_n} - a_1\right) + \frac{1}{2}\left(C_2 \frac{E_{11}}{E_n} + S_2 \frac{E_{12}}{E_n}\right)\right] \quad , \tag{2.22}$$

$$F_6 = a_1 a_2 \epsilon + a_2 \epsilon \exp(-E_o/E_n) \left[\left(C + \frac{C_2}{2} \right) \left(\frac{E_o}{E_n} - a_1 \right) + \frac{3}{4} C_1 \frac{E_{11}}{E_n} + \frac{1}{4} \left(C_3 \frac{E_{11}}{E_n} + (S_1 + S_3) \frac{E_{12}}{E_n} \right) \right] , \quad (2.23)$$

$$F_7 = a_2 \epsilon \exp(-E_o/E_n) \left[\frac{C_1}{4} \frac{E_{12}}{E_n} + \frac{1}{4} \left((S_1 + S_3) \frac{E_{11}}{E_n} - C_3 \frac{E_{12}}{E_n} \right) + \frac{S_2}{2} \left(\frac{E_o}{E_r} - a_1 \right) \right] , \quad (2.24)$$

$$F_8 = \omega \epsilon E_{12} + n_o e a_2 \exp(-E_o/E_n) \left[\left(C + \frac{C_2}{2} \right) \frac{E_{11}}{E_n} + C_1 \left(\frac{E_o}{E_n} - a_1 \right) + \frac{S_2}{2} \frac{E_{12}}{E_n} \right] , \quad (2.25)$$

$$F_9 = a_2 \epsilon \exp(-E_o/E_n) \left[\left(C - \frac{C_2}{2} \right) \frac{E_{12}}{E_n} + S_1 \left(\frac{E_o}{E_n} - a_1 \right) + \frac{S_2}{2} \frac{E_{11}}{E_n} \right] , \quad (2.26)$$

$$F_{10} = a_2 \epsilon \exp(-E_o/E_n) \left[\frac{1}{4} (C_1 - C_3) \frac{E_{12}}{E_n} + \frac{1}{4} (S_1 + S_3) \frac{E_{11}}{E_n} + \frac{S_2}{2} \left(\frac{E_o}{E_n} - a_1 \right) \right] , \quad (2.27)$$

$$F_{11} = a_1 a_2 \epsilon + a_2 \epsilon \exp(-E_o/E_n) \left[C \left(\frac{E_o}{E_n} - a_1 \right) + \frac{1}{4} (C_1 - C_3) \frac{E_{11}}{E_n} + \frac{1}{4} (3S_1 - S_3) \frac{E_{12}}{E_n} \right] , \quad (2.28)$$

$$F_{12} = -\omega\epsilon E_{11} + a_2 n_o e \exp(-E_o/E_n) \left[\left(C - \frac{C_2}{2} \right) \frac{E_{12}}{E_n} + S_1 \left(\frac{E_o}{E_n} - a_1 \right) + \frac{S_2}{2} \frac{E_{11}}{E_n} \right] , \quad (2.29)$$

$$C = I_o(-a) , \quad (2.30a)$$

$$C_1 = 2I_1(-a) \cos \varphi , \quad (2.30b)$$

$$C_2 = 2I_2(-a) \cos 2\varphi , \quad (2.30c)$$

$$C_3 = 2I_3(-a) \cos 3\varphi , \quad (2.30d)$$

$$S_1 = 2I_1(-a) \sin \varphi , \quad (2.30e)$$

$$S_2 = 2I_2(-a) \sin 2\varphi \quad (2.30f)$$

and

$$S_3 = 2I_3(-a) \sin 3\varphi . \quad (2.30g)$$

Each F_i is a function of E_o, E_{11} and E_{12} and does not involve any derivatives of electric fields or any time-dependent quantities.

Equations 2.15 through 2.17 are then solved for $\partial E_o/\partial x$, $\partial E_{11}/\partial_x$ and $\partial E_{12}/\partial x$ and the following set of simultaneous first-order nonlinear equations is obtained:

$$\frac{\partial E_o}{\partial x} = \frac{G_3 G_5 - G_6 G_2}{G_5 G_1 - G_4 G_2} , \quad (2.31)$$

$$\frac{\partial E_{11}}{\partial x} = \frac{G_6 - G_4 \frac{\partial E_o}{\partial x}}{G_5} \quad (2.32)$$

and

$$\frac{\partial E_{12}}{\partial x} = \frac{J_o - F_4 - F_1 \frac{\partial E_o}{\partial x} - F_2 \frac{\partial E_{11}}{\partial x}}{F_3} , \tag{2.33}$$

where

$$G_1 = F_1 F_7 - F_5 F_3 , \tag{2.34a}$$

$$G_2 = F_2 F_7 - F_6 F_3 , \tag{2.34b}$$

$$G_3 = F_7 (J_o - F_4) + F_3 (F_8 - J_{11}) , \tag{2.34c}$$

$$G_4 = F_5 F_{11} - F_9 F_7 , \tag{2.34d}$$

$$G_5 = F_6 F_{11} - F_{10} F_7 \tag{2.34e}$$

and

$$G_6 = F_{11} (J_{11} - F_8) + F_7 (F_{12} - J_{12}) . \tag{2.34f}$$

Knowing the values of E_o, E_{11} and E_{12} at the cathode boundary, $x = 0$, Eqs. 2.31 through 2.33 can be solved simultaneously for E_o, E_{11} and E_{12} using the Runge-Kutta technique[74] on a digital computer. But in view of the large number of steps required to solve the problem for a practical TE device, the computations can become quite costly. A predictor-corrector[74] method is better since it uses information from previous steps to predict new points and therefore requires fewer computations at each step. Predictor-corrector methods are, however, not self-starting and require the values of the electric-field quantities for the first few steps of integration as part of the input, which may be obtained by a Runge-Kutta method. This combination of the two

techniques is used here.[74] Input values of J_o, J_{11}, J_{12} and n_o are required for the solution. Since the phase of the driving current is arbitrary, either J_{11} or J_{12} may be chosen to be zero for convenience. The results presented in later chapters of this study are all for $J_{12} = 0$.

Integration of the electric-field quantities over the length of the device gives the dc and RF voltages along with phase. These, along with the driving dc and RF currents, can be used to find dc and RF impedance, dc and RF power, and efficiency.

A simplification of Eqs. 2.31 through 2.33 is obtained for regions of the GaAs crystal where the static electric field is large by noting that the electron drift velocity is constant for values of electric field greater than approximately 15 kV/cm. Thus when

$$E_o - |(E_{RF})| \geq 15 \text{ kV/cm} \quad , \tag{2.35}$$

$v = v_s$, a constant, where

$$E_{RF} = \sqrt{E_{11}^2 + E_{12}^2} \quad , \tag{2.36}$$

and from Eq. 2.3

$$v_s \approx a_1 a_2 \quad . \tag{2.37}$$

The current equation becomes (again, neglecting diffusion)

$$J = \epsilon v_s \frac{\partial E}{\partial x} + \epsilon \frac{\partial E}{\partial t} + n_o e v_s \quad . \tag{2.38}$$

Substituting for E from Eq. 2.6 gives

$$J_o = \epsilon v_s \frac{\partial E_o}{\partial x} + n_o e v_s \quad , \tag{2.39}$$

$$J_{11} = \epsilon v_s \frac{\partial E_{11}}{\partial x} + \omega\epsilon E_{12} \quad , \tag{2.40}$$

$$J_{12} = \epsilon v_s \frac{\partial E_{12}}{\partial x} - \omega\epsilon E_{11} \tag{2.41}$$

or

$$\frac{\partial E_o}{\partial x} = (J_o - n_o e v_s)/\epsilon v_s \quad , \tag{2.42}$$

$$\frac{\partial E_{11}}{\partial x} = (J_{11} - \omega\epsilon E_{12})/\epsilon v_s \tag{2.43}$$

and

$$\frac{\partial E_{12}}{\partial x} = (J_{12} + \omega\epsilon E_{11})/\epsilon v_s \quad . \tag{2.44}$$

Equations 2.42 through 2.44 are simplified versions of Eqs. 2.31 through 2.33, respectively, and may be solved by the same numerical method.

2.3 Inclusion of the Effects of Diffusion

The total diffusion current[75] is taken here as $-e[\partial(Dn)/\partial x]$ or

$$J_d = -en \frac{\partial D}{\partial x} - eD \frac{\partial n}{\partial x} \quad , \tag{2.45}$$

where D is the diffusion coefficient. Using Poisson's equation, and for uniformly doped material,

$$J_d = -e\left(n_o + \frac{\epsilon}{e} \frac{\partial E}{\partial x}\right) \frac{\partial D}{\partial E} \frac{\partial E}{\partial x} - \epsilon D \frac{\partial^2 E}{\partial x^2} \quad . \tag{2.46}$$

As a simplification, a piecewise linear dependence of D upon the electric field is assumed, approximating the relationship calculated by

calculated by Butcher and Fawcett.[76] Thus, at any position in the GaAs crystal the following may be written:

$$D = P + QE \quad . \tag{2.47}$$

P and Q may be assumed to be constant for a small range of electric-field values. The results will be valid provided the RF electric field is not very large.

Substituting for D from Eq. 2.47 into Eq. 2.46, writing

$$J_d = J_{do} + J_{d11} \cos \omega t + J_{d12} \sin \omega t$$

and using Eq. 2.6 gives

$$J_{do} = \frac{\partial E_o}{\partial x}\left(-en_oQ - \epsilon Q \frac{\partial E_o}{\partial x}\right) + \frac{\partial E_{11}}{\partial x}\left(-\frac{1}{2}\epsilon Q \frac{\partial E_{11}}{\partial x}\right) + \frac{\partial E_{12}}{\partial x}$$

$$\cdot \left(-\frac{1}{2}\epsilon Q \frac{\partial E_{12}}{\partial x}\right) - \epsilon \frac{\partial^2 E_o}{\partial x^2}(P + QE_o) - \frac{1}{2}\epsilon Q\left(E_{11}\frac{\partial^2 E_{11}}{\partial x^2} + E_{12}\frac{\partial E_{12}}{\partial x^2}\right) , \tag{2.48}$$

$$J_{d11} = \frac{\partial E_{11}}{\partial x}\left(-en_oQ - 2\epsilon Q \frac{\partial E_o}{\partial x}\right) - \epsilon \frac{\partial^2 E_{11}}{\partial x^2}(P + QE_o) - \epsilon Q E_{11}\frac{\partial^2 E_o}{\partial x^2} \tag{2.49}$$

and

$$J_{d12} = \frac{\partial E_{12}}{\partial x}\left(-en_oQ - 2\epsilon Q \frac{\partial E_o}{\partial x}\right) - \epsilon \frac{\partial^2 E_{12}}{\partial x^2}(P + QE_o) - \epsilon Q E_{12}\frac{\partial^2 E_o}{\partial x^2} \quad . \tag{2.50}$$

The preceding expressions contain terms involving $\partial E_o/\partial x$, $\partial E_{11}/\partial x$, $\partial E_{12}/\partial x$ and those involving second derivatives of dc and RF electric-field components.

If the effects of diffusion are to be included in the analysis, then J_{do}, J_{d11} and J_{d12} must be added to Eqs. 2.15 through 2.17 for J_o, J_{11} and J_{12}. This modifies F_i to $F_i + F_{ci}$ where F_{ci} are the (correction) terms obtained from Eqs. 2.48 through 2.50 and i = 1,...,12. Unlike F_i, F_{ci} involve first and second derivatives of electric-field quantities. The F_{ci} terms are written as follows:

$$F_{c1} = -en_oQ - \epsilon Q \frac{\partial E_o}{\partial x} , \tag{2.51}$$

$$F_{c2} = -\frac{1}{2} \epsilon Q \frac{\partial E_{11}}{\partial x} , \tag{2.52}$$

$$F_{c3} = -\frac{1}{2} \epsilon Q \frac{\partial E_{12}}{\partial x} , \tag{2.53}$$

$$F_{c4} = -\epsilon(P + QE_o) \frac{\partial^2 E_o}{\partial x^2} - \frac{1}{2} \epsilon Q \left(E_{11} \frac{\partial^2 E_{11}}{\partial x^2} + E_{12} \frac{\partial^2 E_{12}}{\partial x^2} \right) , \tag{2.54}$$

$$F_{c5} = 0 , \tag{2.55}$$

$$F_{c6} = -en_oQ - 2\epsilon Q \frac{\partial E_o}{\partial x} , \tag{2.56}$$

$$F_{c7} = 0 , \tag{2.57}$$

$$F_{c8} = -\epsilon(P + QE_o) \frac{\partial^2 E_{11}}{\partial x^2} - \epsilon Q E_{11} \frac{\partial^2 E_o}{\partial x^2} , \tag{2.58}$$

$$F_{c9} = 0 , \tag{2.59}$$

$$F_{c10} = 0 , \tag{2.60}$$

$$F_{c11} = -en_oQ - 2\epsilon Q - \frac{\partial E_o}{\partial x} \tag{2.61}$$

and

$$F_{c12} = -\epsilon(P + QE_o)\frac{\partial^2 E_{12}}{\partial x^2} - \epsilon Q E_{12}\frac{\partial^2 E_o}{\partial x^2} \quad . \tag{2.62}$$

A solution of Eqs. 2.15 through 2.17 with F_{ci} terms included becomes difficult. If F_{ci} are small compared to F_i then an approximate solution may be obtained by treating F_{ci} as small corrections to F_i. In order to estimate their relative magnitudes, F_{ci} were estimated from the results of a diffusion-free computation. These were found to be less than one tenth of F_i for distances greater than 0.1 μm from the cathode. The solutions including diffusion effects were then obtained by starting with the diffusion-free solutions and then estimating and adding F_{ci} to F_i at each step of integration. The calculations were made using the Runge-Kutta method rather than the predictor-corrector method which fails in such situations.

The diffusion coefficient vs. electric-field relation used for the calculations is shown in Fig. 2.1 along with the calculated results of Butcher and Fawcett[76] at room temperature. The curved parts of the relationship used indicate that the slope was varied in several small steps.

Apart from the calculations of Butcher and Fawcett,[76] other studies of field dependence of diffusion coefficient have been made.[77-80] However, the dependence of the D-E relationship on lattice temperature is not well understood. In view of this and the fact that diffusion effects

cause only a small modification in the equations, the same D-E relationship (Fig. 2.1) was used for all lattice temperatures between 300°K and 500°K for which calculations are presented in this report.

2.4 Nonuniformly Doped Material

If n_o varies along the length of the crystal, its value must be changed accordingly as the integration of Eqs. 2.31 through 2.33 or Eqs. 2.42 through 2.44 proceeds for diffusion-free calculations. If effects of diffusion are included, then, in addition to varying the magnitude of n_o with x, the expression for the diffusion current J_d must be modified to include the gradient in n_o. Thus Eq. 2.46 changes to

$$J_d = -e\left(n_o + \frac{\epsilon}{e}\frac{\partial E}{\partial x}\right)\frac{\partial D}{\partial E}\frac{\partial E}{\partial x} - \epsilon D\frac{\partial^2 E}{\partial x^2} - eD\frac{\partial n_o}{\partial x} \quad . \tag{2.63}$$

This change adds the term $-eD(\partial n_o/\partial x)$ to Eq. 2.63 for the dc diffusion current. The solution then proceeds in a manner similar to that described in Sections 2.2 and 2.3.

2.5 Summary

A one-dimensional, large-signal analysis of subcritically doped and stabilized supercritically doped transferred-electron devices has been presented. The static and RF electric fields are calculated for given dc and RF currents flowing through a GaAs crystal. From these, the static and RF terminal characteristics of the transferred-electron devices can be obtained.

The effects of diffusion are included by treating the diffusion terms as small corrections to the diffusion-free terms, thus avoiding

the solution of second-order equations. The procedure for taking any doping variations into account has also been outlined.

CHAPTER III. THE LARGE-SIGNAL CHARACTERISTICS OF STABILIZED TRANSFERRED-ELECTRON DEVICES WITHOUT DIFFUSION EFFECTS

3.1 Introduction

A large-signal analysis of stabilized transferred-electron devices was presented in the last chapter. The working equations derived there were solved on a digital computer for specific crystal parameters and operating conditions. Device characteristics, such as the static-field profile in the crystal and the RF impedance, have been calculated for given amounts of dc and RF currents flowing through the crystal. Salient results of these calculations are presented in this chapter. Diffusion effects have been neglected for the present discussion and will be considered in later chapters.

Section 3.2 gives small-signal results based on the present theory. These are compared with the results of previous small-signal theories. The comparison was done as a check on the validity of the analysis, the accuracy of the equations given in Chapter II and the accuracy of the computer program. Section 3.3 discusses the large-signal characteristics of stabilized TE devices. The behavior of the RF impedance as the length of the GaAs crystal is varied and as the RF signal level is increased from a small value is investigated. The implications of the latter for the linearity and saturation characteristics of a stabilized TE amplifier are discussed. Dc to RF conversion efficiency is calculated for different signal levels and is shown as a function of crystal length for a fixed frequency. The effect of signal

level on the static-field profile is also described. Movement and growth of space-charge layers in the crystal is discussed in Section 3.4.

3.2 Comparison of Small-Signal Results with Those of Previous Theories

Figure 3.1 shows plots of the static field E_o as a function of x, the distance from the cathode, for three different values of normalized dc current through the GaAs crystal. The calculations are based on the analysis of Chapter II and are for the small-signal case and a low frequency. Also shown in the figure are the corresponding results of McCumber and Chynoweth[26] for comparison. All the plots are for a uniform doping density of $n_o = 10^{13}/cm^3$. The currents are normalized with respect to J_{th} as follows:

$$J_{th} = n_o e v_{th} \quad , \tag{3.1}$$

where v_{th} is the average electron drift velocity at the threshold electric field.

The velocity-field characteristic used by McCumber and Chynoweth is shown in Fig. 3.2 (curve II). The approximation to their curve, used for calculations based on the present theory, is also shown (curve I). The following parameters were used for the approximation:

$$a_1 = 0.55 \quad ,$$

$$a_2 = 1.43 \times 10^7 \text{ cm/s} \quad ,$$

$$E_n = 2.17 \times 10^3 \text{ V/cm} \quad .$$

The discrepancy between the two sets of plots in Fig. 3.1 can be explained in terms of the differences in the velocity-field

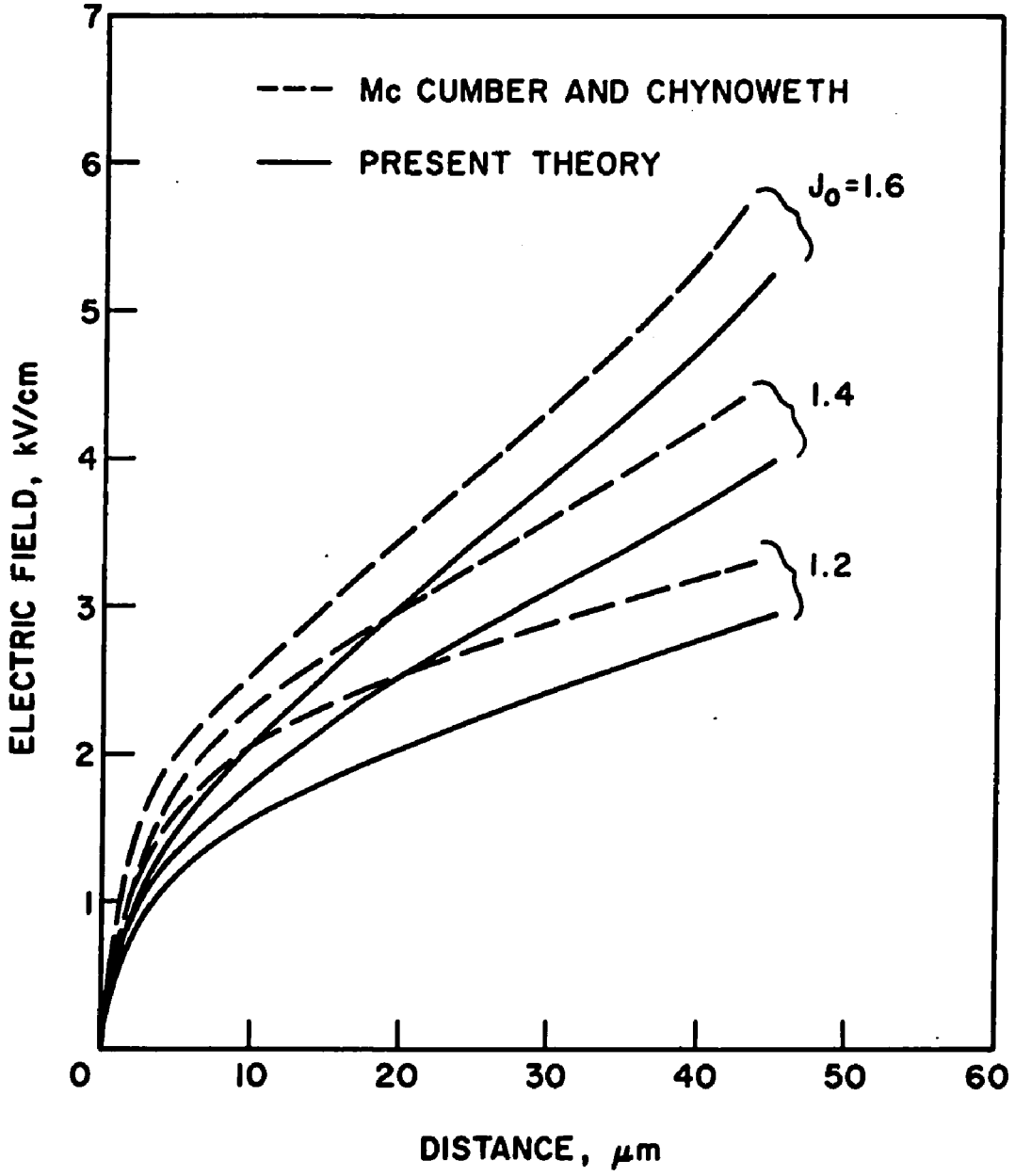


FIG. 3.1 STATIC FIELD (FOR SMALL ac SIGNALS) VS. DISTANCE FOR $n_o = 10^{13}/cm^3$.

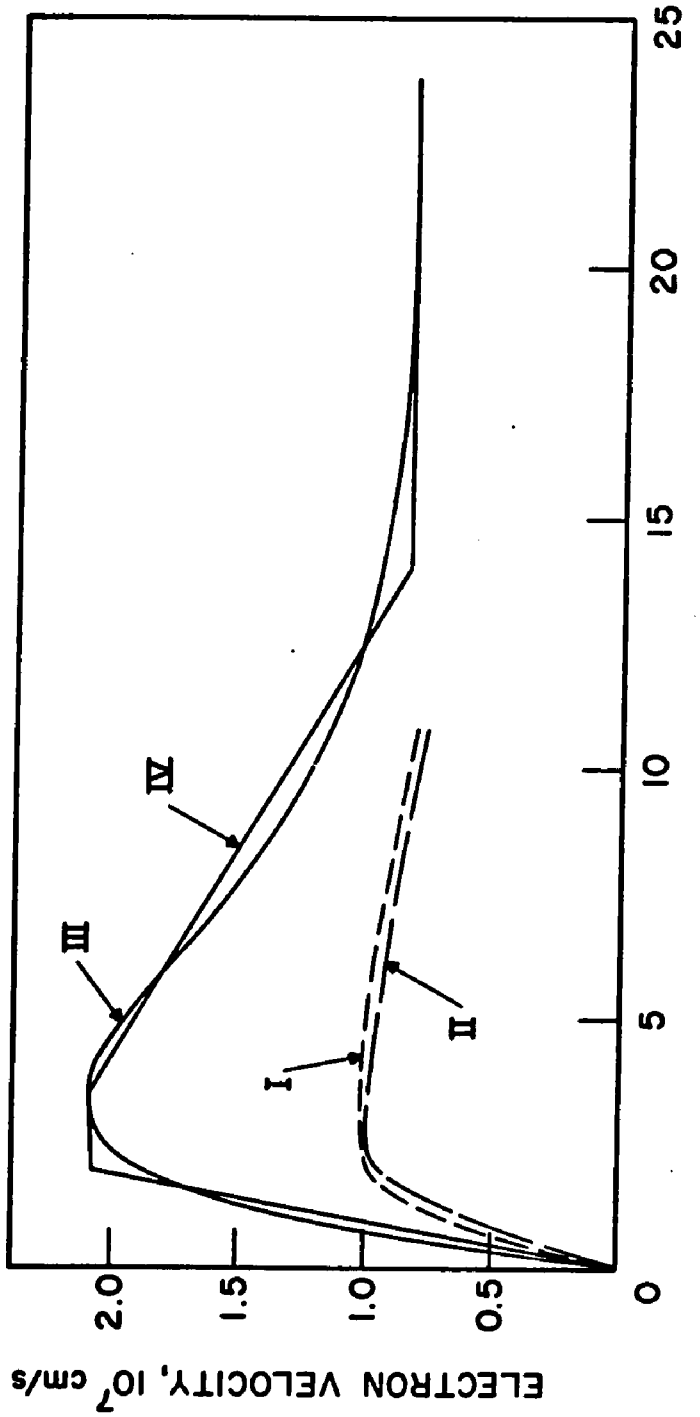


FIG. 3.2 VELOCITY-FIELD CHARACTERISTICS. I. $a_1 = 0.55$, $a_2 = 1.43 \times 10^7$ cm/s, $E_n = 2.17$ kV/cm.

II. MC CUMBER AND CHYNOWETH. III. $a_1 = 0.19$, $a_2 = 4.25 \times 10^7$ cm/s, $E_n = 2.8333$ kV/cm.

IV. PIECEWISE LINEAR CHARACTERISTIC USED FOR SMALL-SIGNAL ANALYSIS.

relationships used. At fields below threshold, the characteristic used by McCumber and Chynoweth has a lower velocity requiring a greater accumulation of carriers for the same current density. This greater excess carrier density leads to higher slopes of static electric field near the cathode. The slopes at greater distances from the cathode are nearly the same for both sets of curves implying the same amount of excess carrier density. This is because the average carrier velocity is approximately the same at higher electric fields for both of the velocity-field relationships.

A comparison of the small-signal impedance of a GaAs diode calculated from the present theory and from the analysis of Holmstrom[53] will now be presented. Calculations with the present theory were made using the velocity-field characteristic labeled III in Fig. 3.2 for which

$$a_1 = 0.19 \ ,$$

$$a_2 = 4.25 \times 10^7 \text{ cm/s} \ ,$$

$$E_n = 2.8333 \text{ kV/cm} \ .$$

The other parameters were arbitrarily chosen as

$$n_o = 5 \times 10^{14}/\text{cm}^3 \ ,$$

$$J_o = 1.3 \ ,$$

$$J_{11} = 0.001 \ ,$$

$$J_{12} = 0 \ ,$$

$$\text{Area} = 0.7 \times 10^{-4} \text{ cm}^2 \ ,$$

$$\text{Frequency} = 15 \text{ GHz} \ .$$

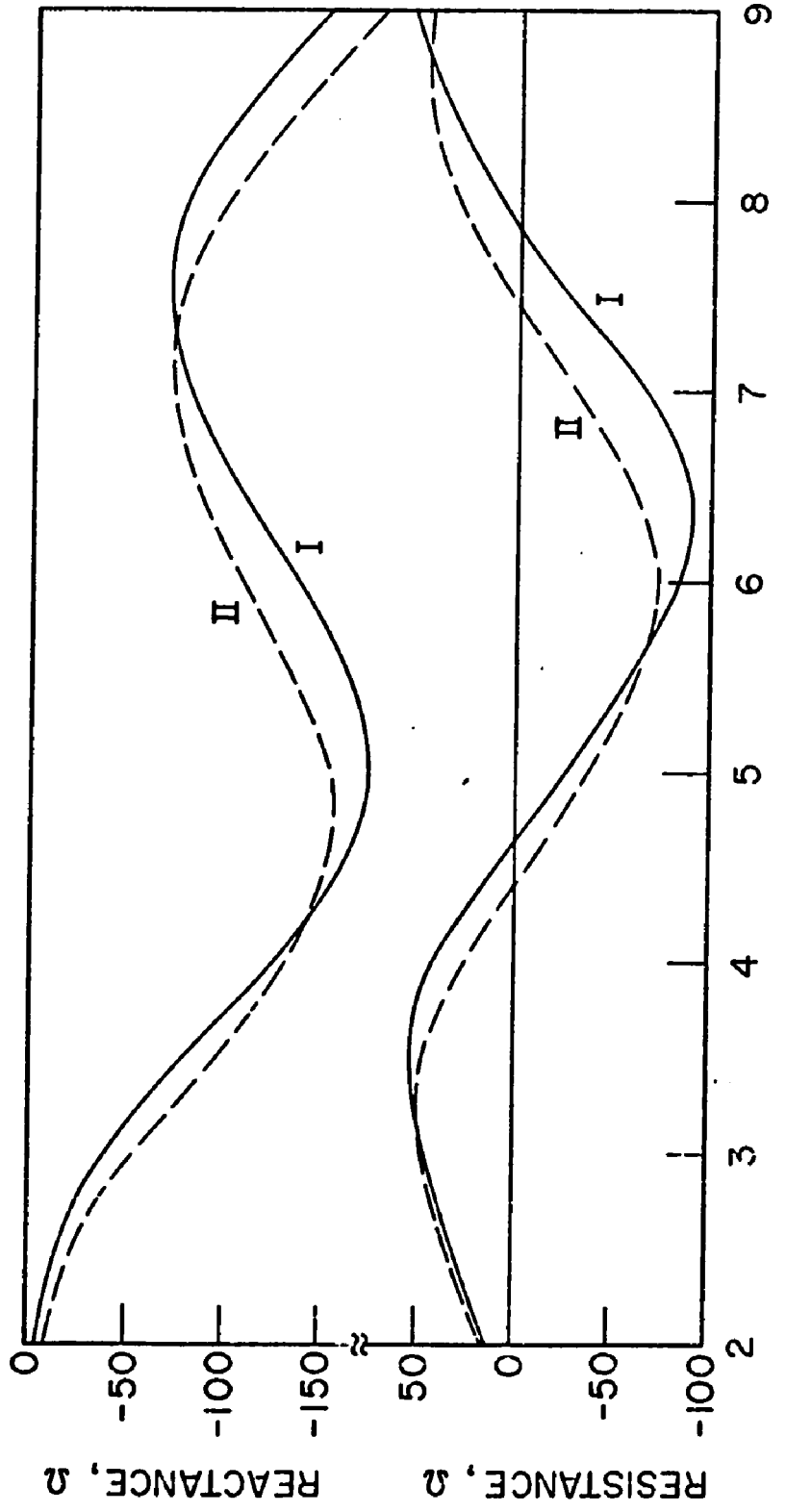
The resistance and reactance of the crystal for these parameters are plotted as functions of crystal length in Fig. 3.3. $J_{11} = 0.0001$ is a small-signal case since any value less than this leads to the same results.

Curve III in Fig. 3.2 was approximated by a piecewise linear relationship labeled curve IV in Fig. 3.2, and the impedance of the crystal was calculated for the same material and operating parameters using a small-signal analysis based on the basic equations of Holmstrom. These results are also plotted in Fig. 3.3 for comparison. The agreement is quite good. Similar agreement was found for other values of crystal and operating parameters.

3.3 Large-Signal Characteristics for the Diffusion-Free Case

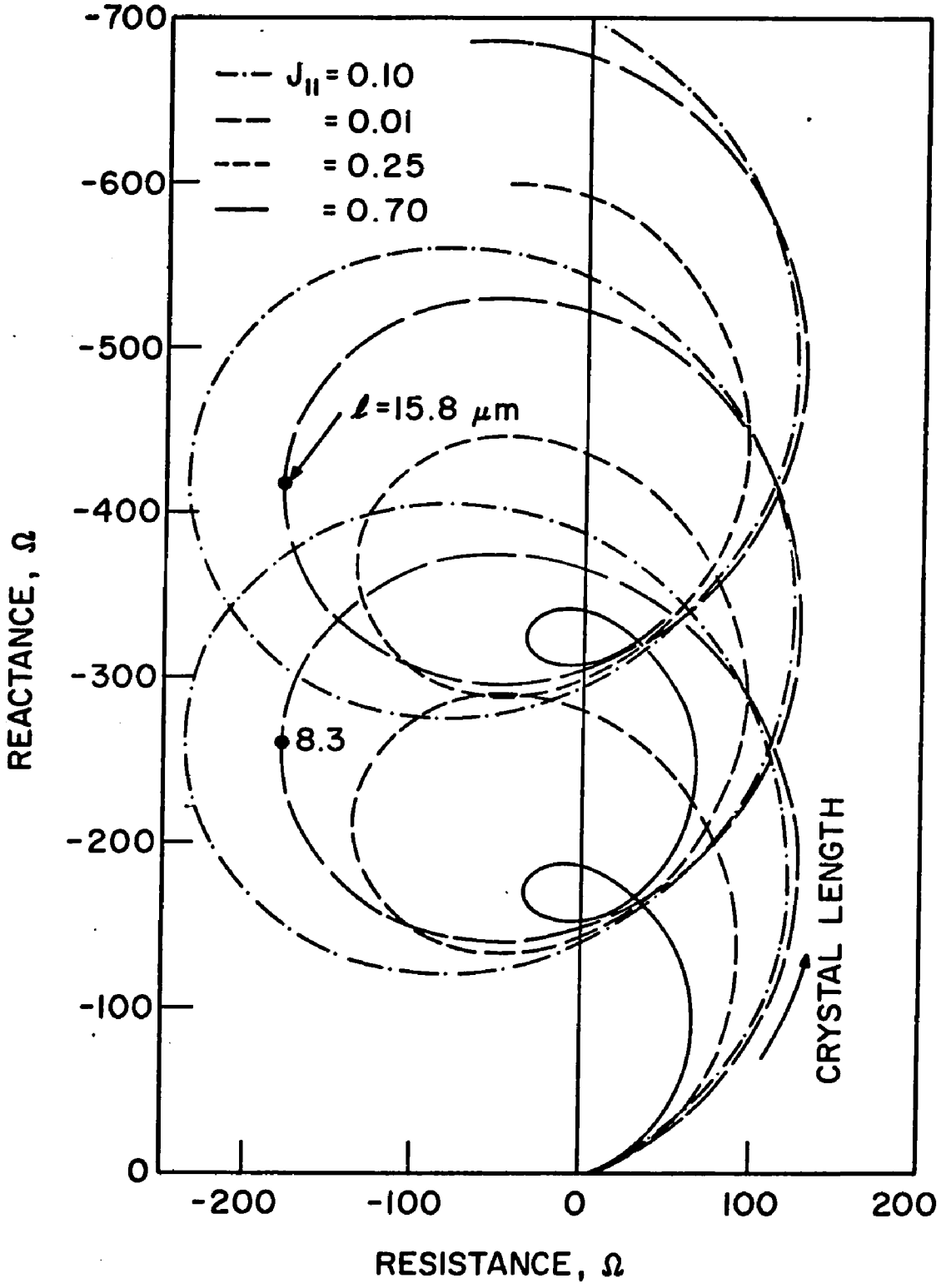
In order to assess the potential of an active device as an amplifier, it is important to understand the behavior of its impedance or admittance as the device parameters or the operating conditions are varied. Whether it is the impedance or the admittance that is examined is almost a matter of convenience. However, diode impedance calculations are preferred for the following reason. Calculations start with an assumed value of RF current, and impedances at two frequencies can be compared easily for the same RF current. On the other hand, RF voltage is not known until diode impedance is known. Thus it is harder to compare diode admittances for two frequencies for the same RF voltage.

Figure 3.4 shows the variation in impedance of a device as its length is increased from zero for different values of the normalized RF current density J_{11} ($J_{12} = 0$). The device and operating parameters are:



$J_o = 1.3$, $n_o = 5 \times 10^{14}/cm^3$, $A = 0.7 \times 10^{-4}$ cm^2, Frequency = 15 GHz

FIG. 3.3 RESISTANCE AND REACTANCE VS. DEVICE LENGTH. CURVES I. SMALL-SIGNAL ANALYSIS.[53] CURVES II. PRESENT ANALYSIS WITH $J_{11} = 0.0001$.



n_o = 5 x 10^{14}/cm^3, J_o = 1.2, Frequency = 10 GHz, A = 0.7 x 10^{-4} cm^2,

Lattice Temperature = 300°K

FIG. 3.4 IMPEDANCE PLANE CURVES FOR A GaAs CRYSTAL.

$$n_o = 5 \times 10^{14}/cm^3 ,$$

$$\text{Area} = 0.7 \times 10^{-4} \text{ cm}^2 ,$$

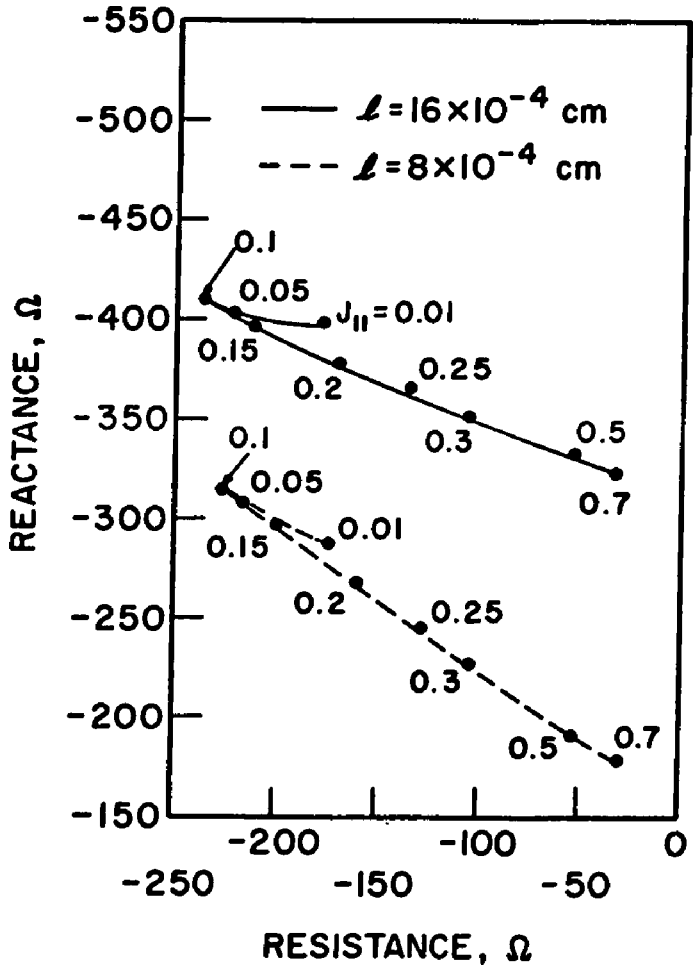
$$J_o = 1.2 ,$$

$$\text{Frequency} = 10 \text{ GHz} .$$

The lattice temperature is taken to be 300°K. The curves start at zero impedance for zero length and go through positive- and negative-resistance regions alternately, along with a general increase in reactance, as the length is increased. The magnitude of the negative resistance goes through a maximum repeatedly. The first two maxima are shown in the figure for each value of J_{11}, along with the length and the bias voltage at which they occur for $J_{11} = 0.01$.

Notice that the magnitude of each maximum of negative resistance is the same for a constant J_{11}. No decrease in this magnitude was seen for higher-order maxima which are not shown in the figure. This is a consequence of neglecting diffusion and assuming constant average carrier velocity at high electric fields. This point will be discussed further when movement and growth of space-charge layers is discussed in Section 3.4 and again in the next chapter when diffusion effects are discussed.

The magnitude of the maximum negative resistance initially increases as J_{11} is increased from a small value and then decreases as J_{11} is increased further. This is seen more clearly in Fig. 3.5. Here impedance is plotted for different values of RF current for device lengths of 8 and 16 μm. The RF power generated by a device may be



$n_o = 5 \times 10^{14}/cm^3$, $J_o = 1.2$, Frequency = 10 GHz, $A = 0.7 \times 10^{-4}$ cm^2,

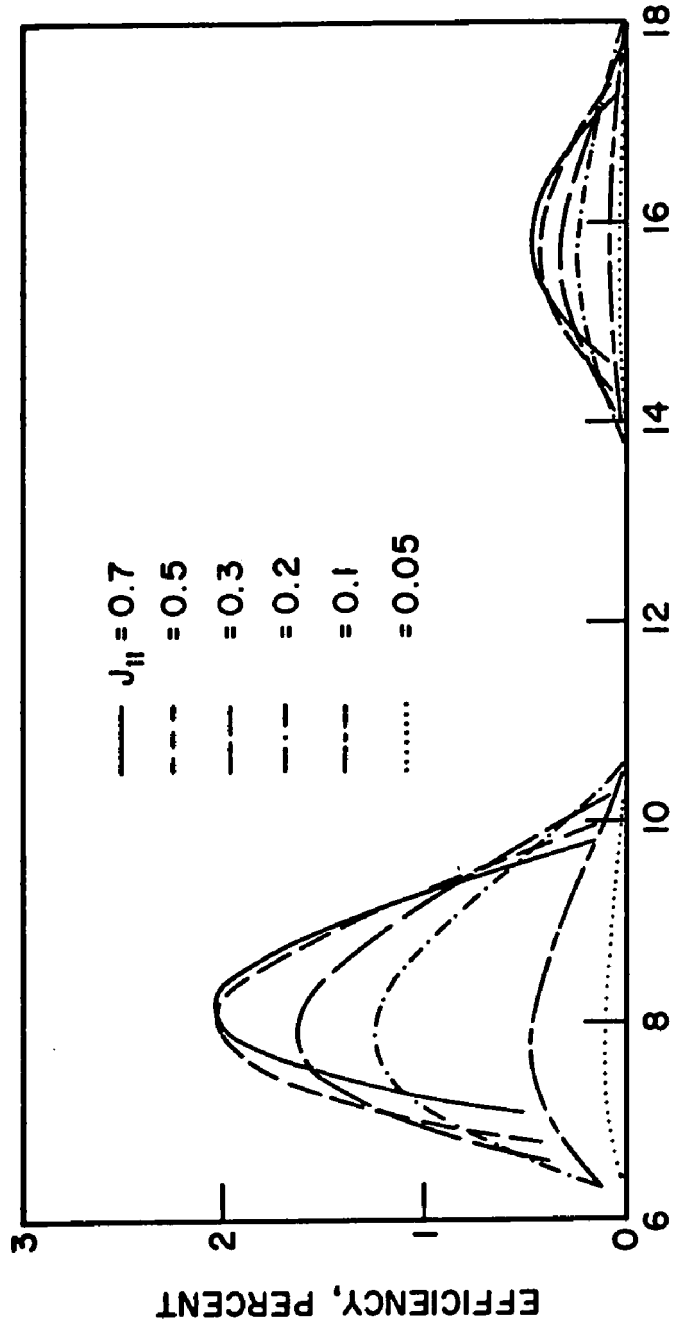
Lattice Temperature = 300°K

FIG. 3.5 IMPEDANCE PLANE CURVES FOR TWO CRYSTALS.

calculated by time averaging the product of the RF current and the 180 degrees out-of-phase component of RF voltage. The dc power input to the device is simply the product of dc current and voltage. The ratio of the RF power generated to the dc bias power gives the dc to RF conversion efficiency of the device. Plots of efficiency calculated for the case of Fig. 3.3 are shown in Fig. 3.6 for different values of the normalized RF current density J_{11} and as a function of crystal length. Again, the first two regions of power generation are shown. For lengths between these regions the device will absorb RF power since it has a positive RF resistance. Since, as shown in Fig. 3.3, the magnitude of the negative resistance is the same at the two maxima for the same J_{11}, the RF power generated is also the same. However, because of a higher dc (bias) voltage at longer lengths, the efficiency is lower in the second region of negative resistance, as shown in Fig. 3.6. The efficiency is lower still if the device is operated in higher-order regions (corresponding to greater crystal lengths).

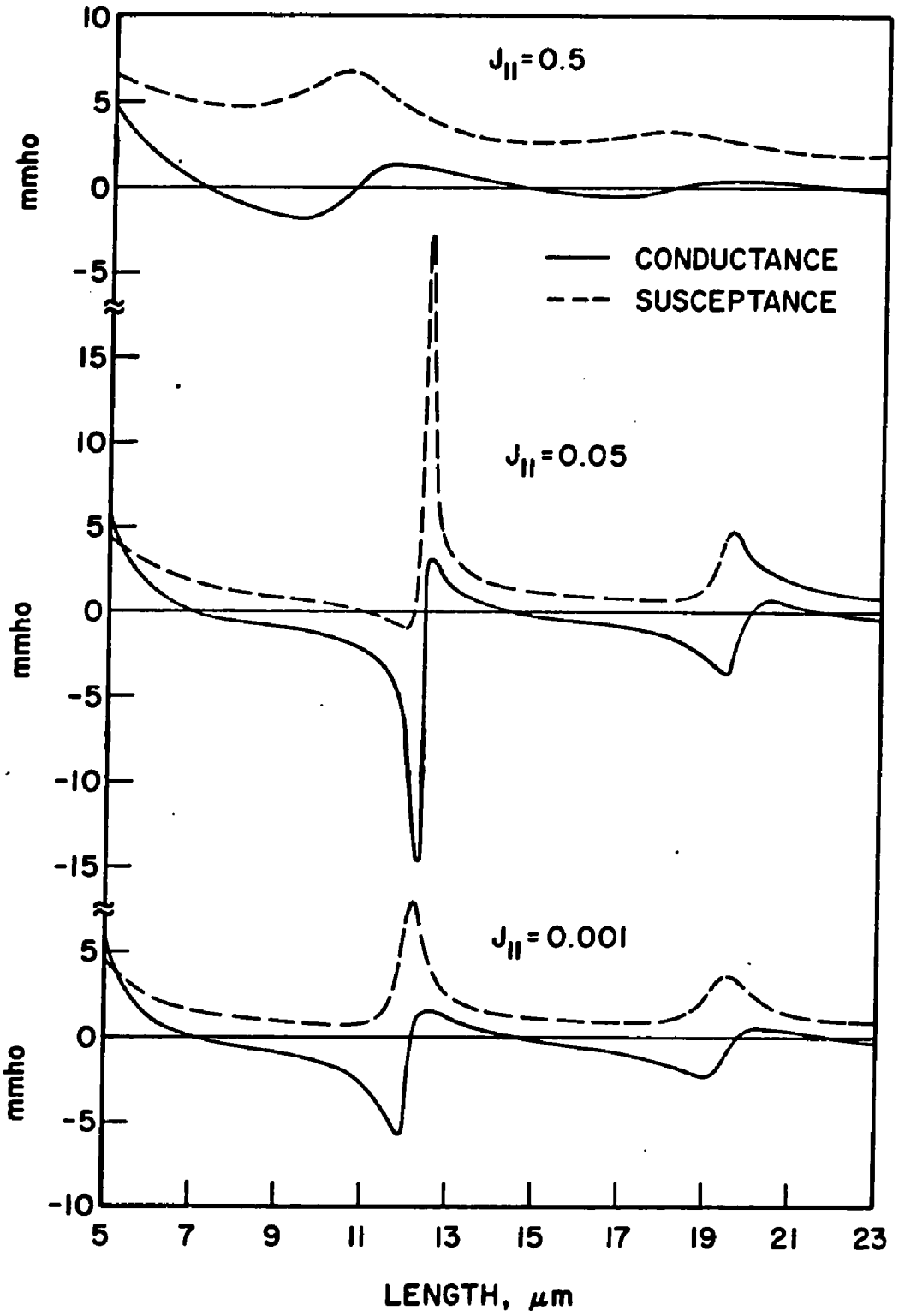
The figure also shows that as J_{11} is increased from a small value, the maximum efficiency increases, but the increase is very small as J_{11} is increased from a normalized value of 0.5 to 0.7. It is shown in Chapter V that the efficiency reaches a maximum as a function of J_{11} for a constant bias current as well as when bias voltage is held constant.

Conductance and susceptance for the crystal parameters and conditions of Fig. 3.3 (except that $J_o = 1.1$) are shown in Fig. 3.7 as functions of crystal length. Again, the first two negative conductance regions are shown. The magnitude of maximum negative conductance in the



$n_o = 5 \times 10^{14}/cm^3$, $J_o = 1.2$, Frequency = 10 GHz, A = 0.7×10^{-4} cm^2, Lattice Temperature = 300°K

FIG. 3.6 RF EFFICIENCY VS. CRYSTAL LENGTH.



n_o = 5 x $10^{14}/cm^3$, J_o = 1.1, Frequency = 10 GHz, A = 0.7 x 10^{-4} cm^2,

Lattice Temperature = 300°K

FIG. 3.7 CRYSTAL ADMITTANCE VS. LENGTH.

second region is smaller than that in the first region despite the fact that the magnitude of maximum negative resistance in the two regions is the same. The reason for this is the greater reactance in the second region.

The change in sign of susceptance for $J_{11} = 0.05$ along with negative conductance for the same device length indicates that the crystal could sustain oscillations in a purely resistive circuit. However, it is shown in the next chapter that such behavior may not be observed when diffusion effects are included. This change in the sign of susceptance as well as the sharp peaks in both conductance and susceptance were not observed for $J_o \geq 1.2$ for any value of J_{11} for this donor density and frequency.

The maximum value of negative conductance increases initially as J_{11} is increased from a small value and then decreases as the RF current density is increased further. This behavior is similar to that of negative resistance seen in Fig. 3.4. This effect is also observed in Fig. 3.8 where the resistance and reactance for a device with the following parameters are plotted as functions of the normalized RF current density J_{11}:

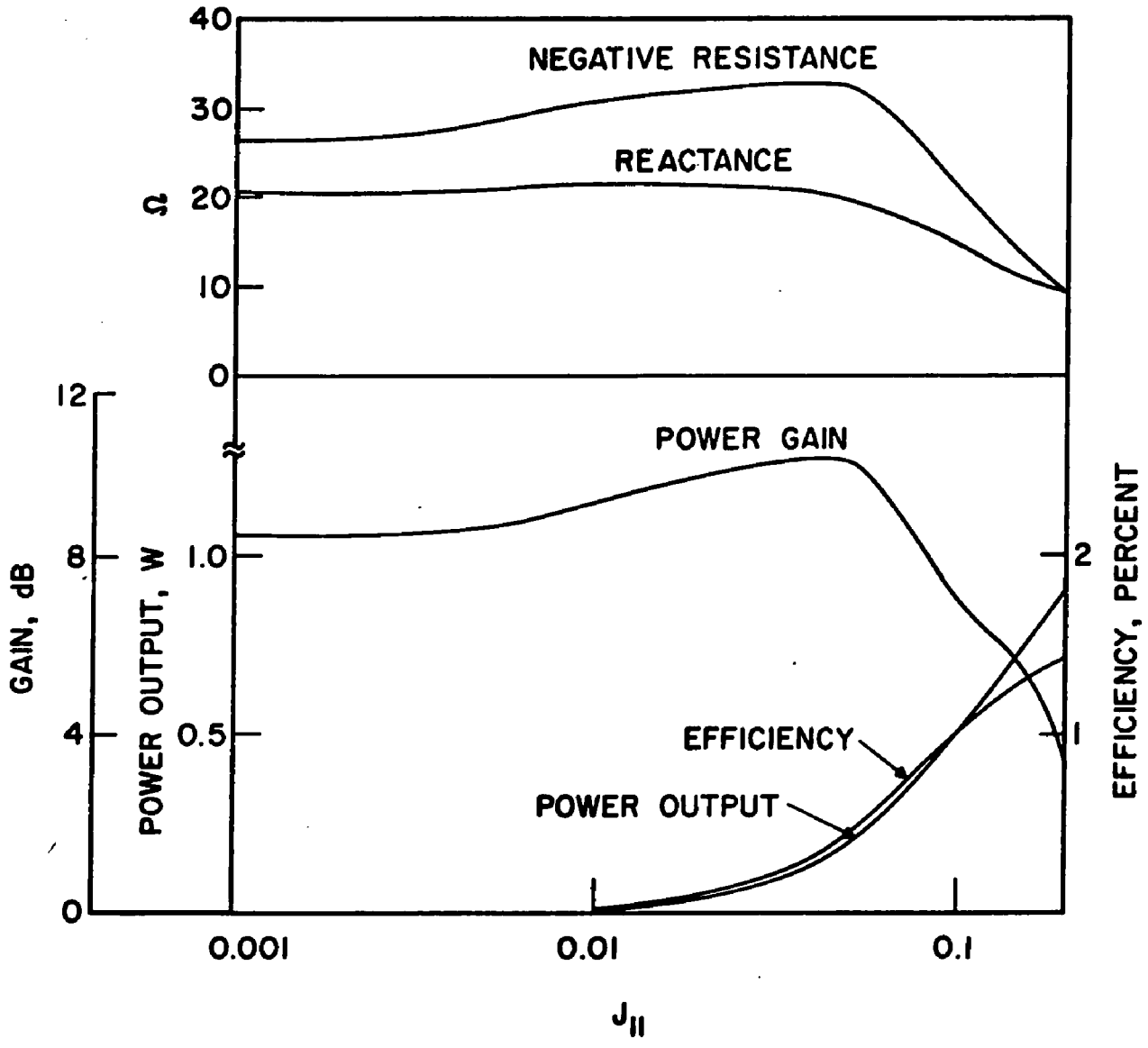
$$n_o = 5 \times 10^{14}/cm^3 ,$$

$$\ell = 9.6\ \mu m ,$$

$$A = 1.4 \times 10^{-3}\ cm^2 ,$$

$$\text{RF Frequency} = 10\ GHz ,$$

$$J_o = 1.1 .$$



J_o = 1.1, n_o = 5 x $10^{14}/cm^3$, Length = 9.6 μm, Frequency = 10 GHz,

Lattice Temperature = 300°K

FIG. 3.8 IMPEDANCE, POWER GAIN, POWER OUTPUT AND EFFICIENCY.

The length of 9.6 μm was chosen because the magnitude of negative resistance is maximum at this length for the small-signal case of $J_{11} = 0.001$. The negative resistance is seen to decrease rapidly at large signal levels. The nature of variation of the resistance and reactance of the crystal with RF current magnitude has a direct bearing on the linearity of an amplifier using the crystal as the active device. The calculated power gain, power output and efficiency are also shown in Fig. 3.8 for the crystal connected in series with a 50-Ω load. For a reflection amplifier, power gain is simply the square of the magnitude of reflection coefficient and is calculated as

$$G = \left| \frac{Z_L - Z_d}{Z_L + Z_d} \right|^2 , \qquad (3.2)$$

where Z_L is the load or circuit impedance and Z_d is the impedance of the device. A slight "peaking" of gain is observed as J_{11} is increased from a small value. This effect is likely to be more evident when the device is operated at high gain, i.e., when the positive resistance of the circuit is only slightly greater than the magnitude of the negative resistance of the TE device, since then the gain becomes sensitive to small changes in the negative resistance. Such peaking has been observed experimentally by Sene and Rosenbaum[81] and Monroe and Kennedy.[82] It is shown in Chapter V that this type of behavior is more pronounced at higher bias voltages.

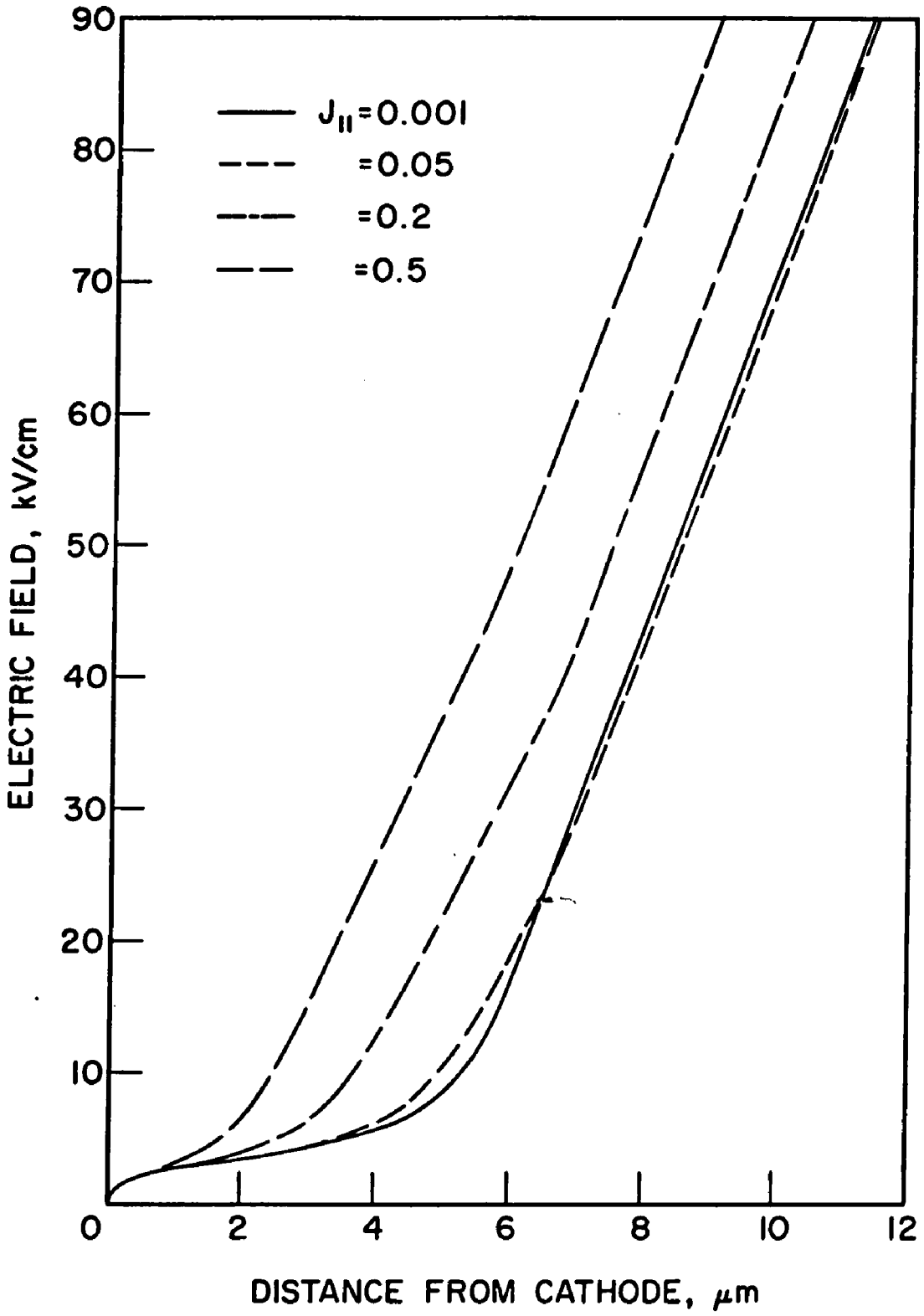
It is also seen from Fig. 3.8 that the efficiency does not increase as rapidly as the power output for large values of J_{11}. This occurs because, for a constant dc bias current, the static-field distortion

increases as the input RF signal is increased. This leads to a greater bias voltage for the same dc current and thus reduces efficiency. This effect also implies an increase in the dc resistance of the crystal. In circuits where the bias voltage is kept constant, this property is manifested as a current decrease as the RF amplitude in the crystal increases and is readily observed as negative conductance oscillations build up in a TE device.

The increase in static-field distortion at large RF current amplitudes is shown in Fig. 3.9 where static electric field is plotted against distance from the cathode for the crystal parameters and operating conditions of Figs. 3.7 and 3.8. Even though the increase in static-field distortion with increase in J_{11} is substantial at large values of J_{11}, it is not the same for small values of J_{11}. While the magnitude of the static field increases with J_{11} closer to the cathode, it decreases further away from it for small values of J_{11}. A closer study showed that this decrease in the value of static field away from the cathode is associated with an increase in the amplitude of that component of RF electric field which is 180 degrees out of phase with the RF current. In other words, the increase in the magnitude of negative resistance with J_{11}, for small J_{11}, noted in Figs. 3.6 and 3.8 seems to have the effect of reducing the static field in the active region of the crystal.

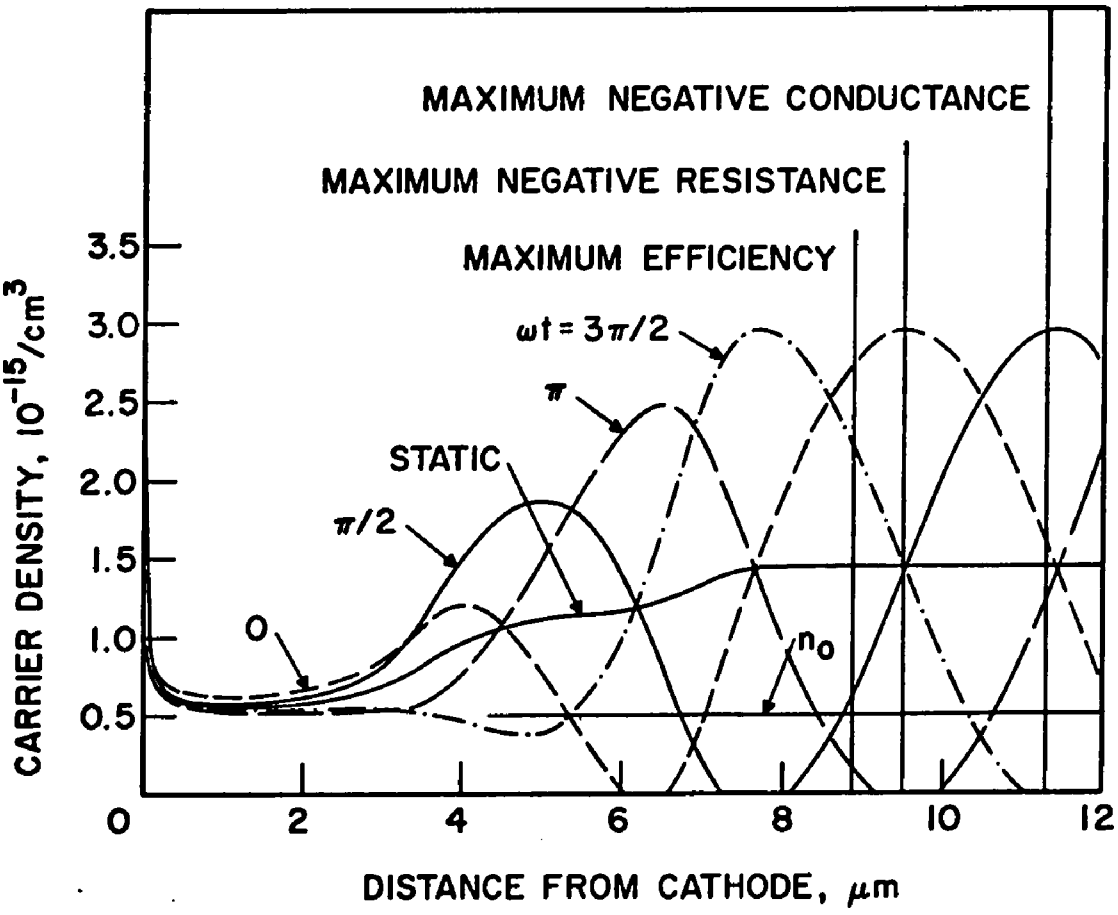
3.4 Movement and Growth of Space-Charge Layers in Stabilized TE Devices

Figure 3.10 shows a plot of instantaneous carrier density as a function of distance from the cathode at different times during the RF cycle for the same GaAs crystal and bias current J_o as that of Fig. 3.9



$n_o = 5 \times 10^{14}/cm^3$, $J_o = 1.1$, Frequency = 10 GHz, Lattice Temperature = 300°K

FIG. 3.9 STATIC ELECTRIC FIELD VS. DISTANCE FROM THE CATHODE.



$n_o = 5 \times 10^{14}/cm^3$, $J_o = 1.1$, $J_{11} = 0.15$, Frequency = 10 GHz

FIG. 3.10 INSTANTANEOUS CARRIER DENSITY VS. DISTANCE FROM THE CATHODE AT 300°K.

and for a normalized RF current density of $J_{11} = 0.15$ at 10 GHz. Growing space-charge accumulation and depletion layers are seen moving away from the cathode. The static component or the average carrier density is also shown in the figure.

At large distances from the cathode, i.e., beyond 8 μm in the figure, the average carrier density is constant. This is required by the condition of continuity of current since the average carrier velocity is constant because of the high electric field in this region. In addition, growth of space-charge layers is seen to stop in this region and their amplitude becomes constant with distance. This last effect is also caused by the constant carrier velocity which implies zero differential mobility, thus there is neither growth nor decay. The extent of carrier depletion calculated by the theory turns out to be greater than the doping density for the large-signal case. In actual devices this would lead to a distortion of the space-charge waveform. However, such distortion is not accounted for by the present theory. It will be shown that diffusion effects reduce the amount of depletion for the same values of J_{11}. If an analysis were made to include this distortion term, then it would be desirable to include time harmonics of the electric field which also have been neglected.

Figure 3.11 shows the corresponding total electric field $E_o + E_{11} \cos \omega t + E_{12} \sin \omega t$ as well as the average electric field E_o for the cases plotted in Fig. 3.10. Notice that the dominance of the excess electron charge causes the pattern to resemble an accumulation layer mode rather than a domain mode. Figures 3.10 and 3.11 also show device lengths for which maximum dc to RF conversion efficiency, negative resistance and negative conductance occur.

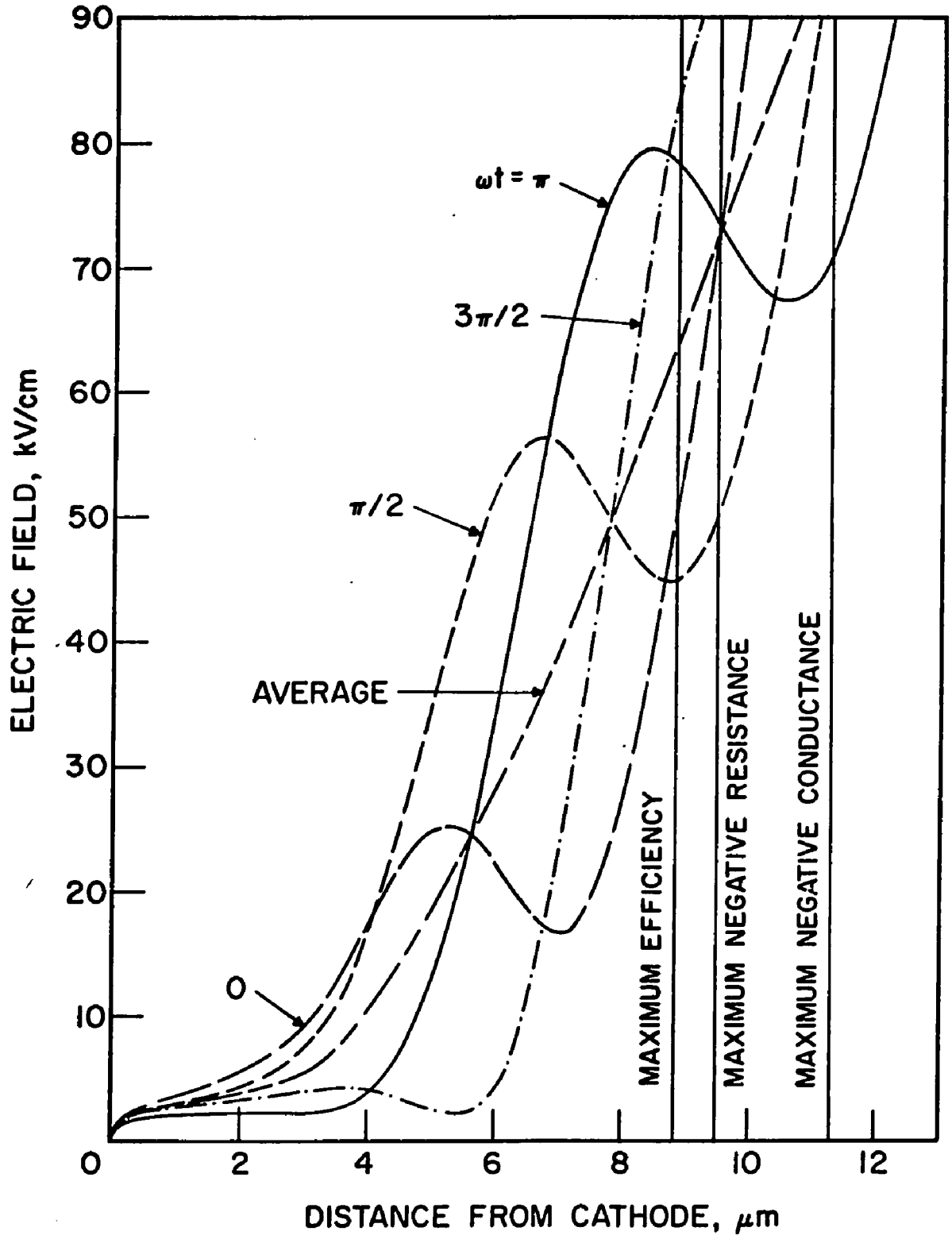


FIG. 3.11 ELECTRIC FIELD VS. DISTANCE FROM THE CATHODE FOR THE CASES SHOWN IN FIG. 3.10.

3.5 Summary

Small-signal calculations of TE device characteristics using the analysis presented in Chapter II have been shown to agree with calculations based on previous small-signal theories. This is true for static as well as RF characteristics.

It was shown that as the length of a GaAs crystal biased above threshold is increased from a small value, its RF negative resistance goes through successive maxima. The magnitude of these maxima is the same for a constant value of J_{11} if diffusion is neglected.

The magnitude of the negative resistance of a device at first increases and then decreases as J_{11} is increased from a small value. This leads to a peaking in the RF power gain as the RF signal level is varied.

The dc resistance of a TE device generally increases with an increase in RF signal level. This is caused by an increase in static-field distortion when J_{11} is increased. This effect explains the decrease in current observed when negative conductance oscillations build up in a TE device.

Space-charge layers were shown to grow as they move away from the cathode. The growth stops at larger distances from the cathode because the average electric field is so high that the differential mobility is zero.

CHAPTER IV. THE EFFECTS OF DIFFUSION UPON THE CHARACTERISTICS OF STABILIZED TRANSFERRED-ELECTRON DEVICES

4.1 Introduction

The inclusion of the effects of diffusion in the large-signal analysis of stabilized TE devices was discussed in Chapter II. It was stated that diffusion currents are quite small compared to the conduction current, except near the cathode. Nevertheless, these currents do affect the performance of these devices and the modifications in device characteristics resulting from these currents are discussed in this chapter.

Section 4.2 discusses the dc effects of diffusion currents. Both of the components of the diffusion current caused by gradients in both the average carrier density and the diffusion coefficient are examined, and their overall effect on the static device characteristics is analyzed.

The effect of diffusion upon the RF characteristics of TE devices is treated in Section 4.3. The effect upon the growth of space-charge accumulation layers is shown. In addition, the effect upon external device characteristics, namely, the RF impedance and the dc to RF conversion efficiency, is also discussed.

4.2 Effects of Diffusion on the Static Characteristics of Stabilized TE Devices

The diffusion currents in GaAs crystals have two components: that resulting from gradients in carrier density and that caused by a gradient in the magnitude of diffusion coefficient. The second component is usually called "thermal" current since diffusion coefficient is a function of

average carrier temperature. However, the case of GaAs is complicated in that as the carrier temperature increases with increase in electric field, the mobility of the carrier decreases. This more than compensates for the increase in carrier temperature at higher electric fields. Thus the diffusion coefficient at first increases with the electric field and then decreases for high electric fields as shown in Fig. 2.1.

Since the average electric field increases monotonically away from the cathode in a stabilized TE device, the average value of the diffusion coefficient at first increases and then decreases with distance from the cathode. However, the carrier density varies in the opposite manner as is shown in Fig. 4.1. These results are for a GaAs crystal with $n_o = 5 \times 10^{14}/cm^3$ at room temperature and are for

$$J_o = 1.1 \ ,$$

$$J_{11} = 0.0001 \text{ (small signal)} \ ,$$

$$\text{Frequency} = 10 \text{ GHz} \ .$$

The calculations are based on the analysis of Chapter II for the velocity and diffusion coefficient relationships shown in Fig. 2.1. It is clear from Fig. 4.1 that the two components of diffusion current caused by the gradient in average carrier density and that caused by the gradient in diffusion coefficient flow in opposite directions. An assessment of the relative magnitude of the two diffusion current components was made early in this study using a case analyzed by McCumber and Chynoweth.[26]

The diffusion current density due to a gradient in carrier density is

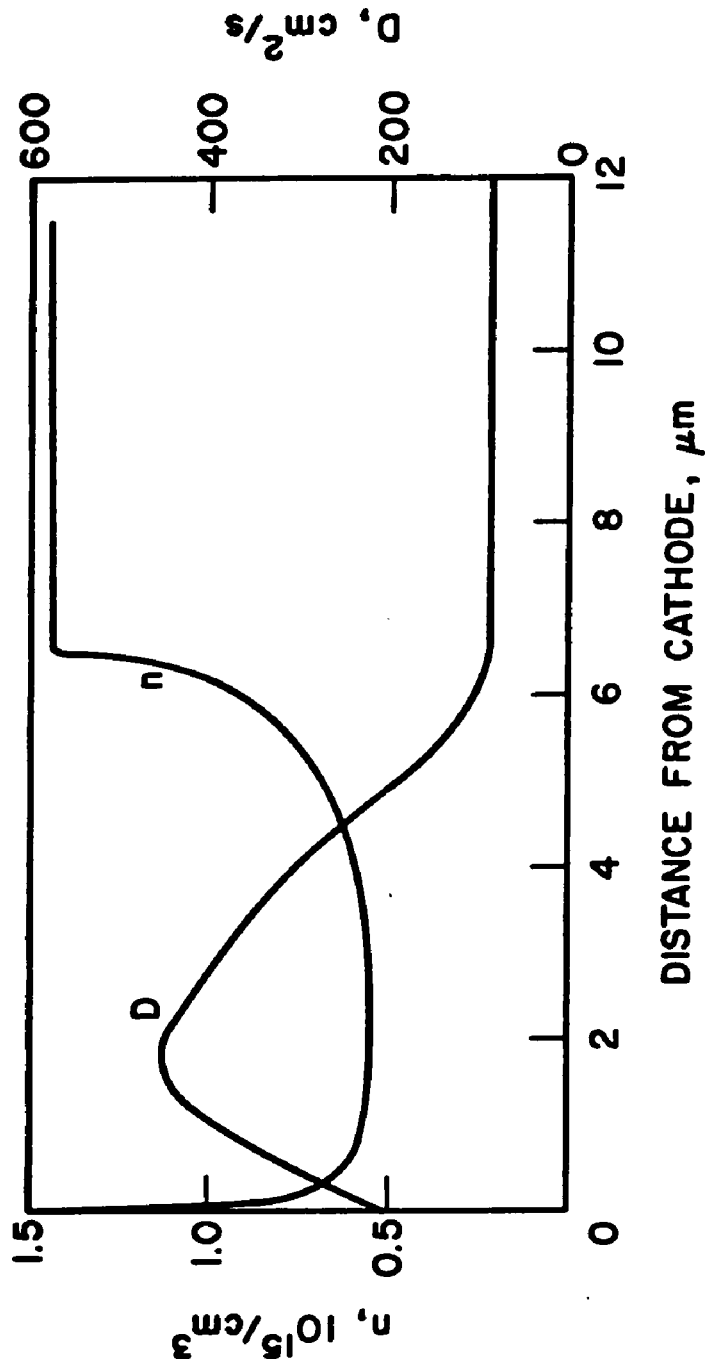


FIG. 4.1 AVERAGE CARRIER DENSITY AND DIFFUSION COEFFICIENT VS. DISTANCE FROM THE CATHODE AT 300°K WITH DIFFUSION EFFECTS INCLUDED. ($n_o = 5 \times 10^{14}/cm^3$, $J_o = 1.1$, $J_{11} = 0.001$ AND FREQUENCY = 10 GHz)

$$J_{DN} = -eD \frac{\partial n}{\partial x} = -\epsilon D \frac{\partial^2 E}{\partial x^2} \qquad (4.1)$$

and the thermal current density is

$$J_{DD} = -en \frac{\partial D}{\partial x} = -e \left(n_o + \frac{\epsilon}{e} \frac{\partial E}{\partial x} \right) \frac{\partial D}{\partial E} \frac{\partial E}{\partial x} , \qquad (4.2)$$

where Poisson's equation (Eq. 2.1) has been used to eliminate n. The diffusion-free static results of McCumber and Chynoweth[26] were used to estimate the various terms in Eqs. 4.1 and 4.2. The velocity-field relation used by McCumber and Chynoweth is shown in the upper half of Fig. 4.2. The static field calculated by them for $n_o = 10^{13}/cm^3$ is shown in the top part of Fig. 4.3 as a function of distance from the cathode for two values of normalized dc current. The slopes of these curves, along with Poisson's equation (Eq. 2.1) were used to calculate the corresponding carrier density which is plotted in the middle section of Fig. 4.3.

The electric-field dependence of diffusion coefficient measured by Ruch and Kino[78] and shown in the lower half of Fig. 4.2 was used for the values of D and $\partial D/\partial E$ at each point along the crystal length. The second derivative of the electric field $\partial^2 E/\partial x^2$ was calculated from the slope of the carrier density vs. distance from the cathode plots of Fig. 4.3. The values of the diffusion current components thus calculated (from Eqs. 4.1 and 4.2) are plotted in the bottom part of Fig. 4.3.

This calculation is a first-order estimate assuming that the diffusion currents are small compared to the total current. That this is true can be seen from the figure. It is also clear from the figure that the two components of diffusion tend to cancel each other. It shows that if

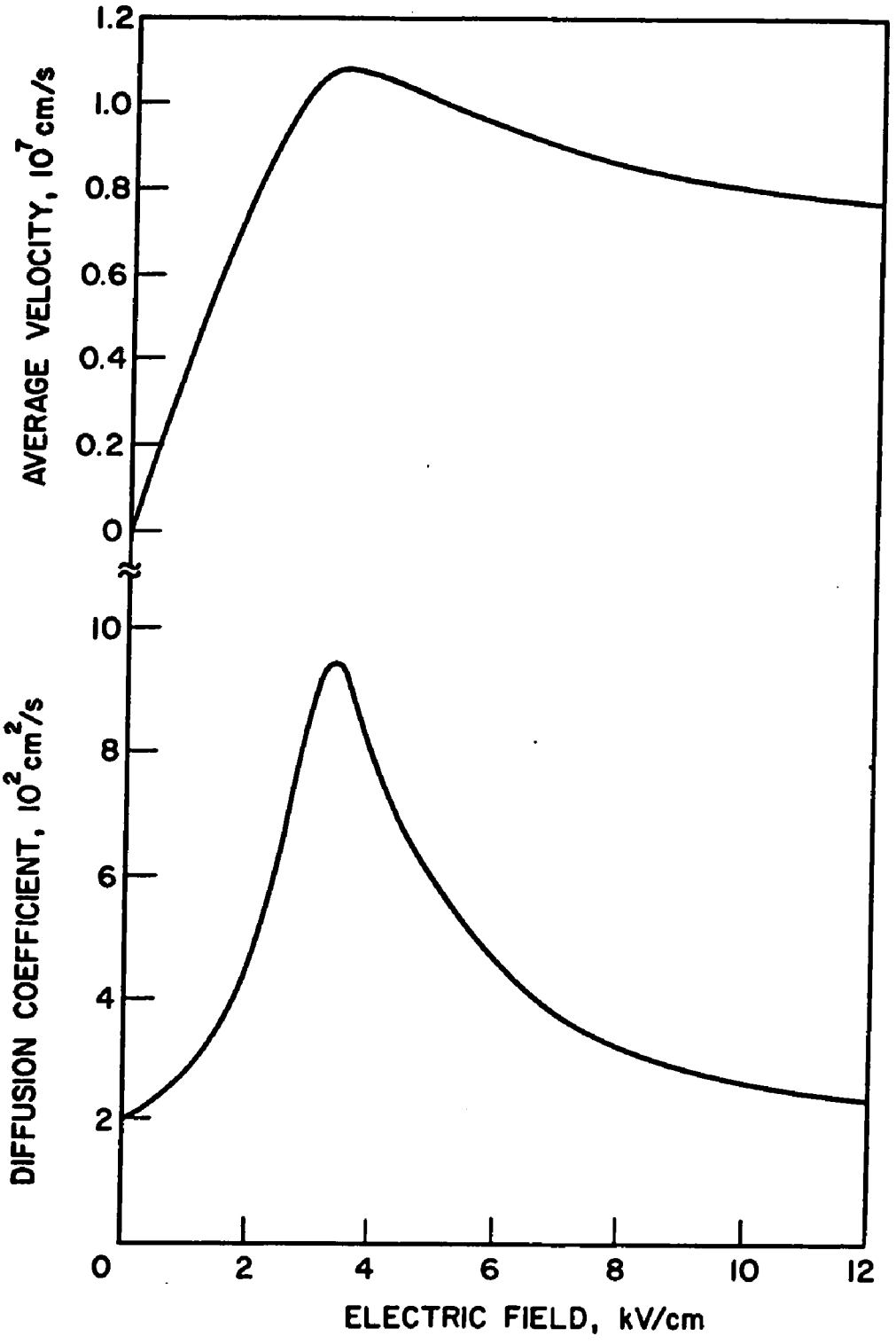


FIG. 4.2 ELECTRON VELOCITY VS. ELECTRIC FIELD (MC CUMBER AND CHYNOWETH[26]) AND DIFFUSION COEFFICIENT VS. ELECTRIC FIELD (RUCH AND KINO[78]).

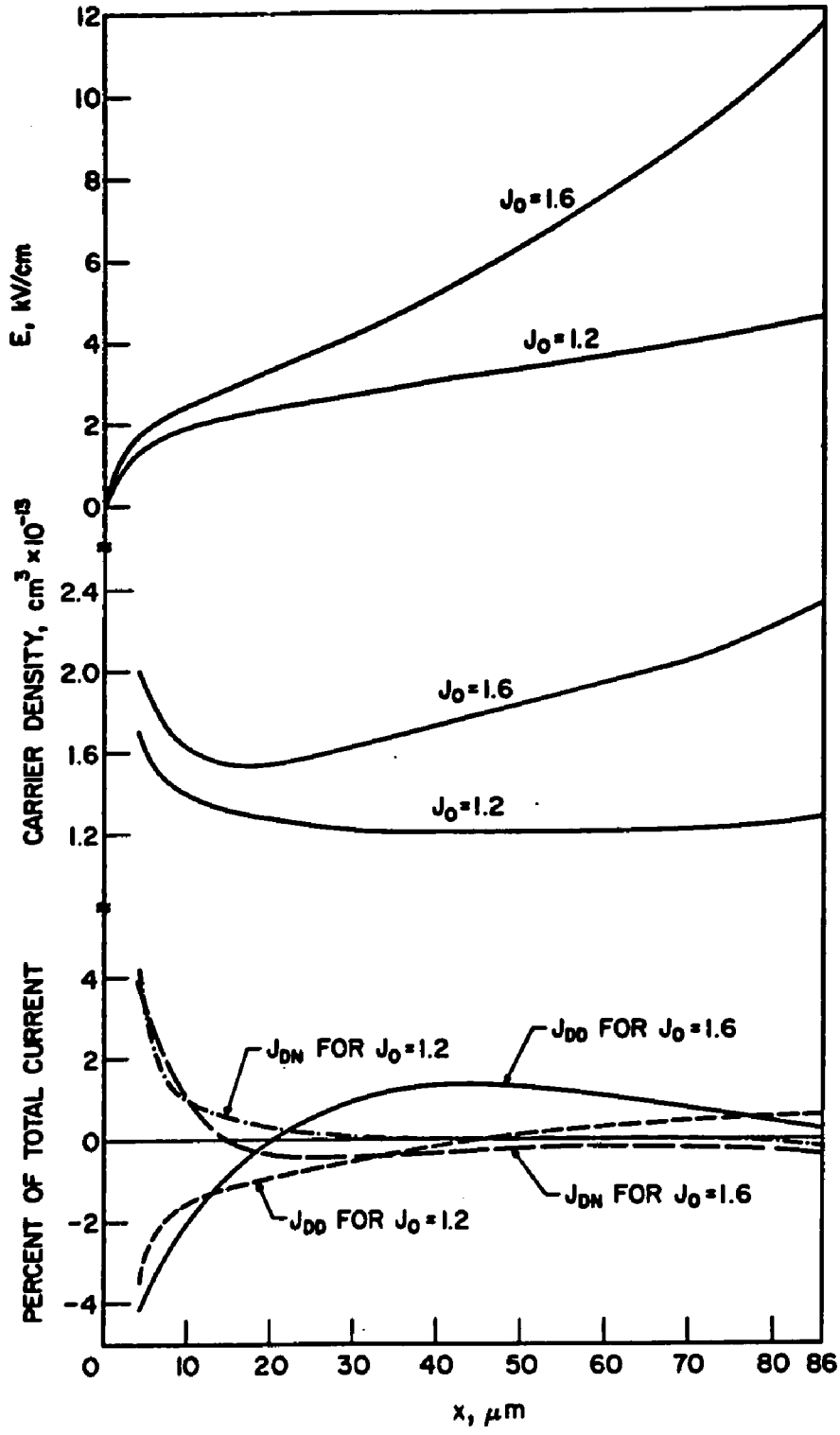
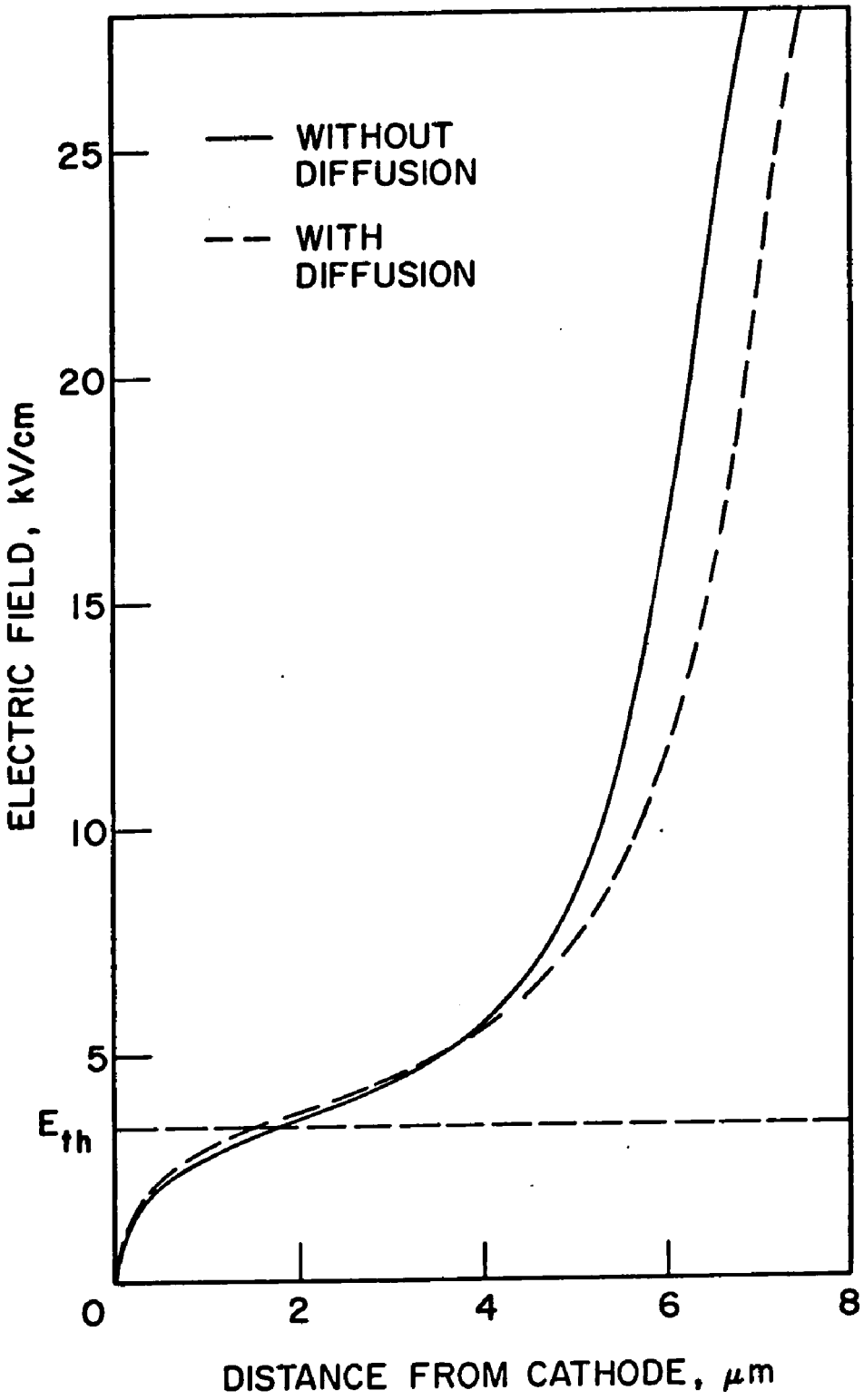


FIG. 4.3 ELECTRIC FIELD, CARRIER DENSITY, AND DIFFUSION AND THERMAL CURRENTS VS. DISTANCE FROM THE CATHODE. ($n_o = 10^{13}/cm^3$)

diffusion effects are to be included in this analysis of TE devices, both of the components of the diffusion current must be included. In other words, the field dependence of diffusion coefficient must be taken into account. The assumption of a field-independent, constant diffusion coefficient would lead to erroneous results. In fact, a more accurate dc solution is obtained if the diffusion is neglected completely than if it is taken to be a constant. If only the current due to gradients in carrier density were considered, the diffusion would have the effect of reducing carrier density gradients, thus reducing the static-field distortion. However, since thermal currents are also present and since this component is somewhat larger than the J_{DN} component and flows in the opposite direction, the overall effect of diffusion would be to increase the static-field distortion. This conclusion is based on the use of a specific dependence of D on the electric field. If the relationship found by Butcher and Fawcett[76] (Fig. 2.1) is used instead of the curve of Ruch and Kino, this is no longer true. This is illustrated by Fig. 4.4 which shows the static field for a crystal of $n_o = 5 \times 10^{14}/cm^3$, $J_o = 1.1$, $J_{11} = 0.01$, Frequency = 10 GHz and at room temperature. Here the static-field distortion is reduced rather than increased. This behavior can be understood by observing that while the value of D calculated by Butcher and Fawcett is smaller than that found by Ruch and Kino, the slope of D with respect to electric field is, in general, even smaller; thus the reduction in the magnitude of thermal currents is greater than that in the other component of diffusion current (J_{DN}). In fact the diffusion current due to gradients in carrier density is now slightly larger than J_{DD}, leading to a slight reduction in static-field distortion.



$J_o = 1.1$, $J_{11} = 0.01$, $n_o = 5 \times 10^{14}/cm^3$ and Frequency = 10 GHz

FIG. 4.4 STATIC ELECTRIC FIELD VS. DISTANCE FROM THE CATHODE AT 300°K.

It may be concluded from this discussion that not only the quantitative but the qualitative nature of the effect of diffusion on the static-field profile depends on the exact nature of the relationship between diffusion coefficient and the electric field. The overall effect, however, remains small as stated previously.

4.3 Effect of Diffusion on the RF Characteristics of Stabilized TE Devices

In Fig. 4.4 it is seen that when the D-E relationship of Butcher and Fawcett is used the overall effect of diffusion is to reduce the static-field distortion. It is also clear from the figure that the length of the passive region near the cathode, i.e., the region where the average electric field is below the threshold value, is reduced. The length of the passive region near the anode is also reduced by the lower static-field values in that region. Thus the active region, where the differential mobility is negative, becomes longer. It might appear that the magnitude of negative resistance and the efficiency of the TE device should improve. However, this is not true since the diffusion effects which cause a reduction in static-field distortion by reducing space-charge accumulation also tend to reduce density modulation of the space-charge wave and cause a reduction in its amplitude.

This can be seen by comparing the plots of instantaneous carrier density as a function of distance shown in Fig. 4.5 (where diffusion effects have been included), with the corresponding plots of Fig. 3.10 (where diffusion effects are neglected). The average carrier density at distances greater than approximately 8 μm from the cathode is unaffected by the inclusion of diffusion effects. This is because D is constant at

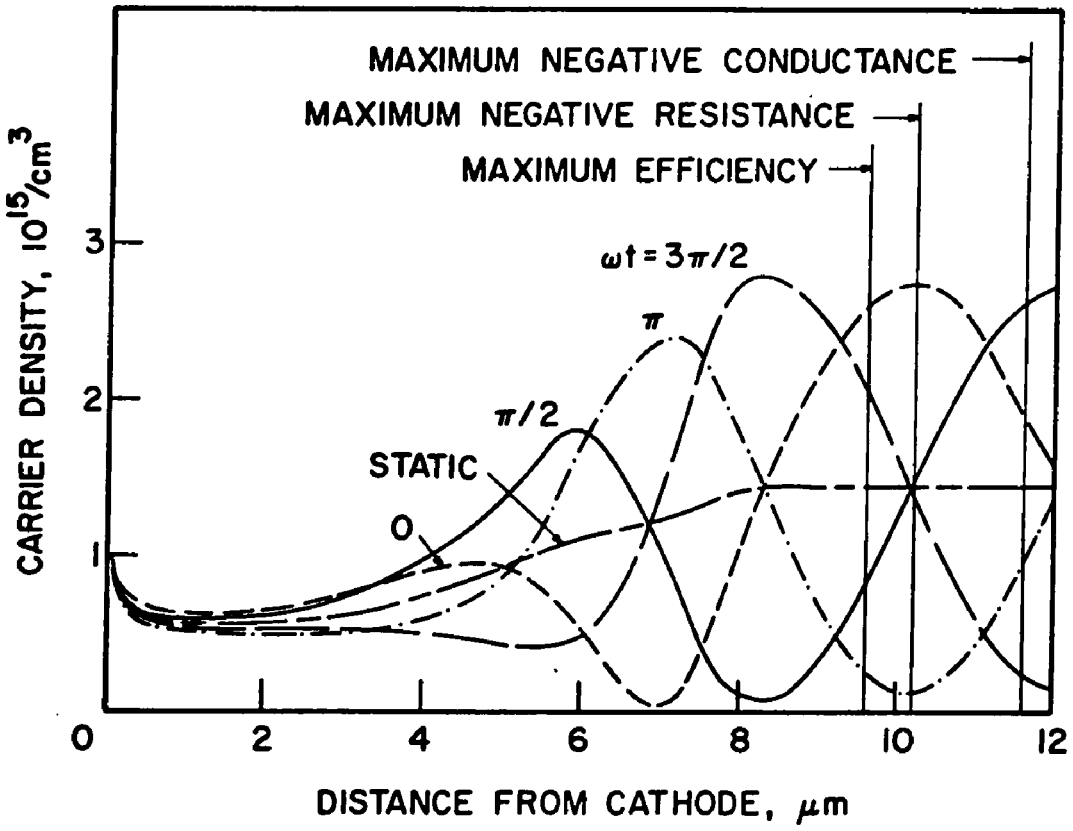


FIG. 4.5 INSTANTANEOUS CARRIER DENSITY VS. DISTANCE FROM THE CATHODE AT 300°K WITH DIFFUSION EFFECTS INCLUDED. ($n_o = 5 \times 10^{14}/cm^3$, $J_o = 1.1$, $J_{11} = 0.15$ AND FREQUENCY = 10 GHz)

high electric fields and because the carrier density is also constant; there are no diffusion currents. The space-charge wave, however, is seen to decay slightly beyond 8 μm unlike the diffusion-free case of Fig. 3.10 where the amplitude stays constant. The decay is because of the diffusion currents resulting from the carrier density modulation. Note that there are no RF thermal currents in this region since the electric field is high enough so that D is constant.

The plots of instantaneous as well as average electric fields corresponding to the carrier density plots of Fig. 4.5 are shown in Fig. 4.6. The amplitude of the waves is again smaller than that in the diffusion-free case of Fig. 3.11.

The damping of charge modulation discussed previously is reflected in the external characteristics of stabilized TE devices. The magnitudes of maximum negative resistance, conductance and efficiency are all reduced. Figure 4.7 shows resistance and reactance as functions of length of a device with the parameters of Fig. 4.6 and for different values of the normalized RF current density J_{11}. As in the diffusion-free case, the magnitude of maximum negative resistance at first increases and then decreases as J_{11} is increased from a small value. However, unlike the diffusion-free case, which is shown for $J_{11} = 0.15$ in the same figure, the second negative-resistance peak has a smaller magnitude than the first. The latter result is a consequence of the reduction in wave amplitude as it travels farther away from the cathode (Fig. 4.5). The overall reduction in the magnitude of negative resistance caused by diffusion can also be seen by comparing the results for $J_{11} = 0.15$, with and without diffusion effects.

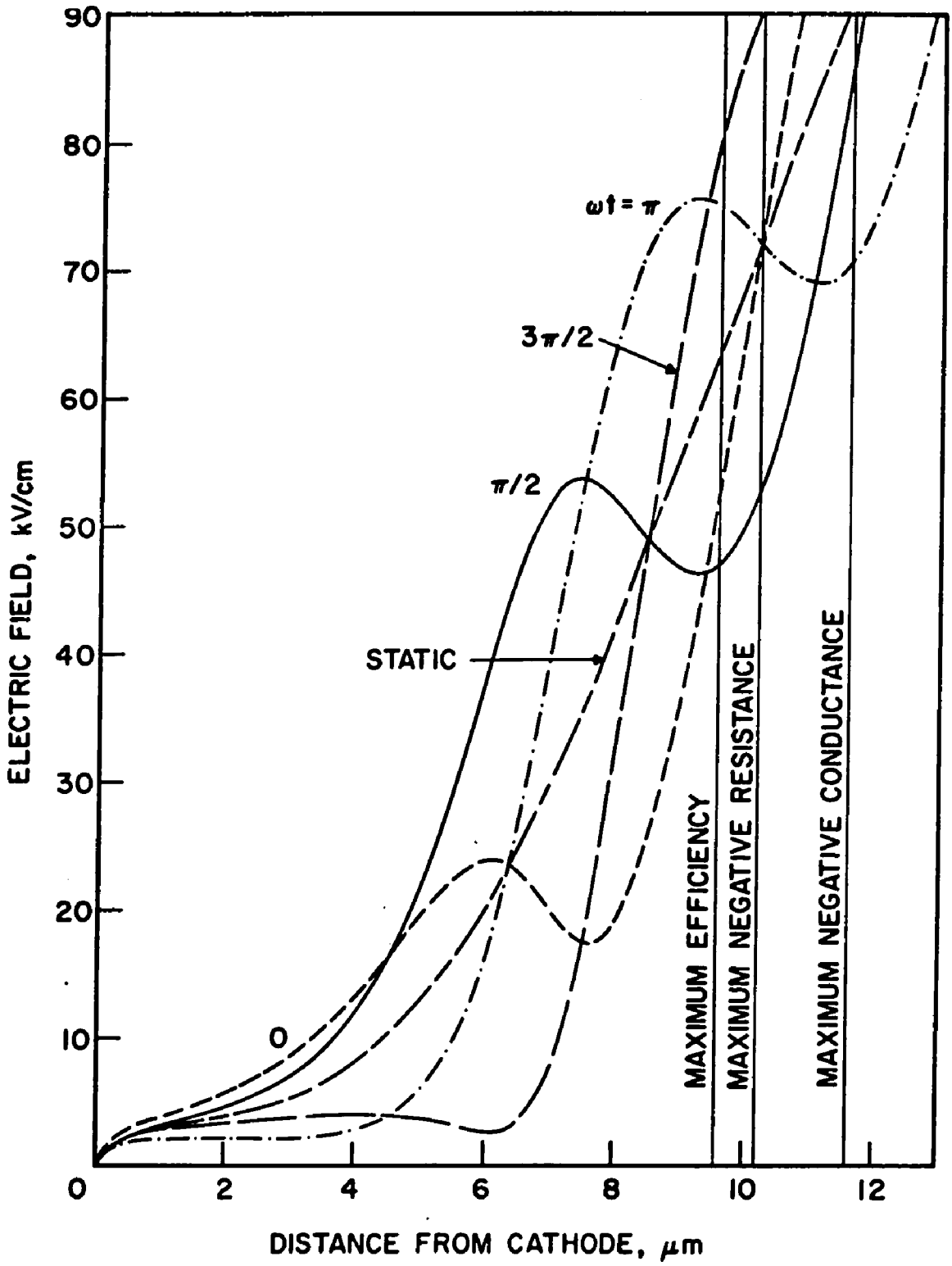


FIG. 4.6 ELECTRIC FIELD VS. DISTANCE FROM THE CATHODE CORRESPONDING TO THE PLOTS OF FIG. 4.5.

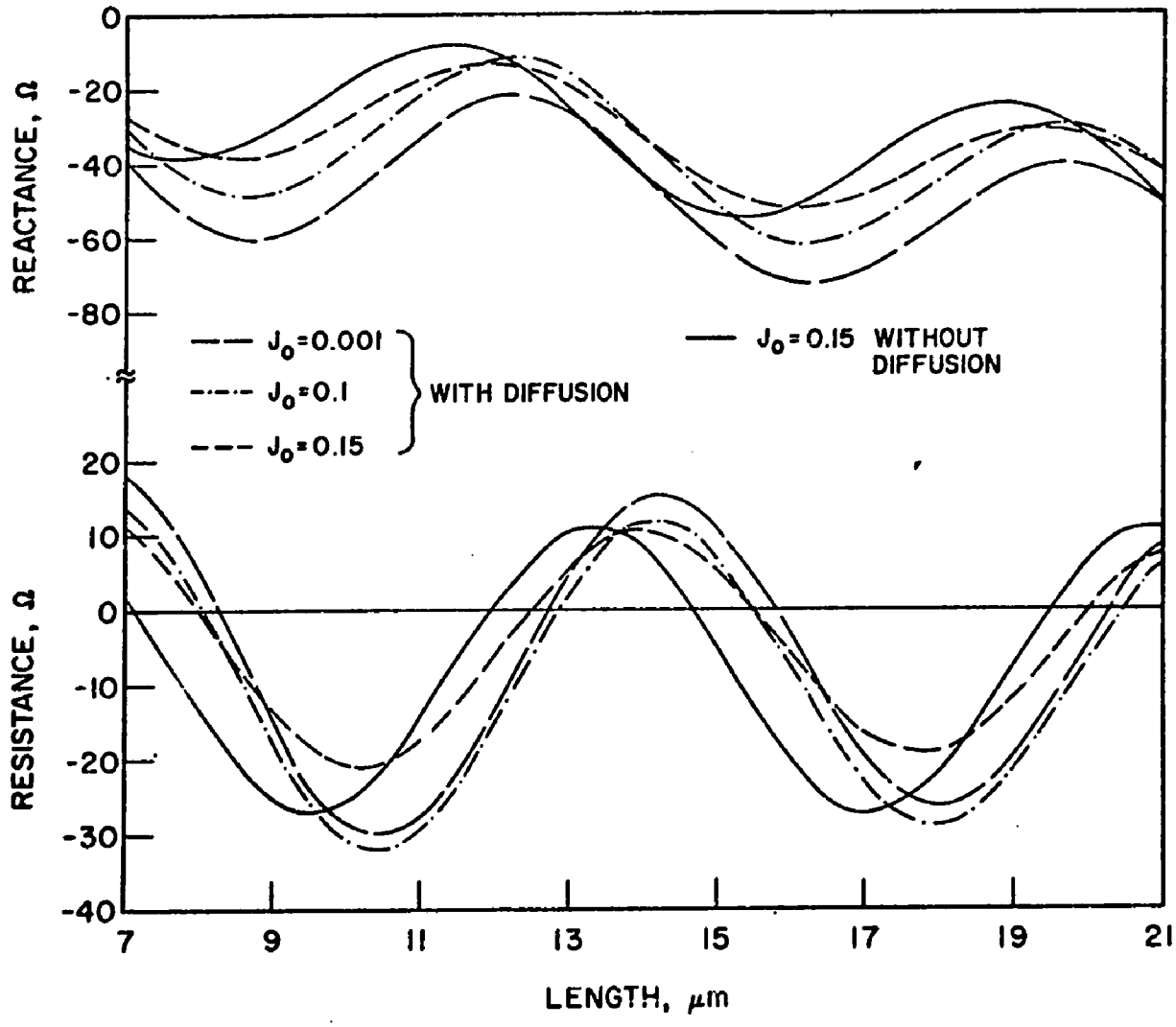


FIG. 4.7 RESISTANCE AND REACTANCE VS. CRYSTAL LENGTH AT 300°K. (J_0 = 1.1, $n_o = 5 \times 10^{14}/cm^3$, $A = 0.7 \times 10^{-3}$ cm^2 AND FREQUENCY = 10 GHz)

A similar reduction in the magnitude of negative conductance also takes place. Figure 4.8 shows the conductance and susceptance of a device with the same material and operating parameters as those of Fig. 3.7. A comparison of the two figures shows that the magnitude of negative conductance obtained when diffusion effects are included is smaller than in the diffusion-free case. Notice, also, that the change in the sign of susceptance is not seen when diffusion effects are included. The sharp peaks in the values of conductance and susceptance seen in the diffusion-free case are also not evident when diffusion effects are taken into account.

As expected, the dc to RF conversion efficiency is also affected. The best efficiency obtainable at 10 GHz, irrespective of device length, is shown in Fig. 4.9 for the crystal and operating parameters of Fig. 4.8, with and without the inclusion of diffusion effects. It is seen that diffusion slightly reduces the efficiency for all values of RF current.

4.4 Summary

The components of diffusion current caused by gradients in carrier density (J_{DN}) and by the gradient in diffusion coefficient (J_{DD}) have been examined. They flow in opposite directions along most of the device length, thereby reducing the overall effect of diffusion on the static characteristic of a TE device. Thus the field dependence of diffusion coefficient must be taken into account for an accurate evaluation of the effect of diffusion on device characteristics.

The relative magnitudes of J_{DN} and J_{DD} depend on the exact nature of the relationship between diffusion coefficient and electric field. If J_{DN} is larger than J_{DD}, the static-field distortion is reduced. The opposite is true if J_{DD} is larger.

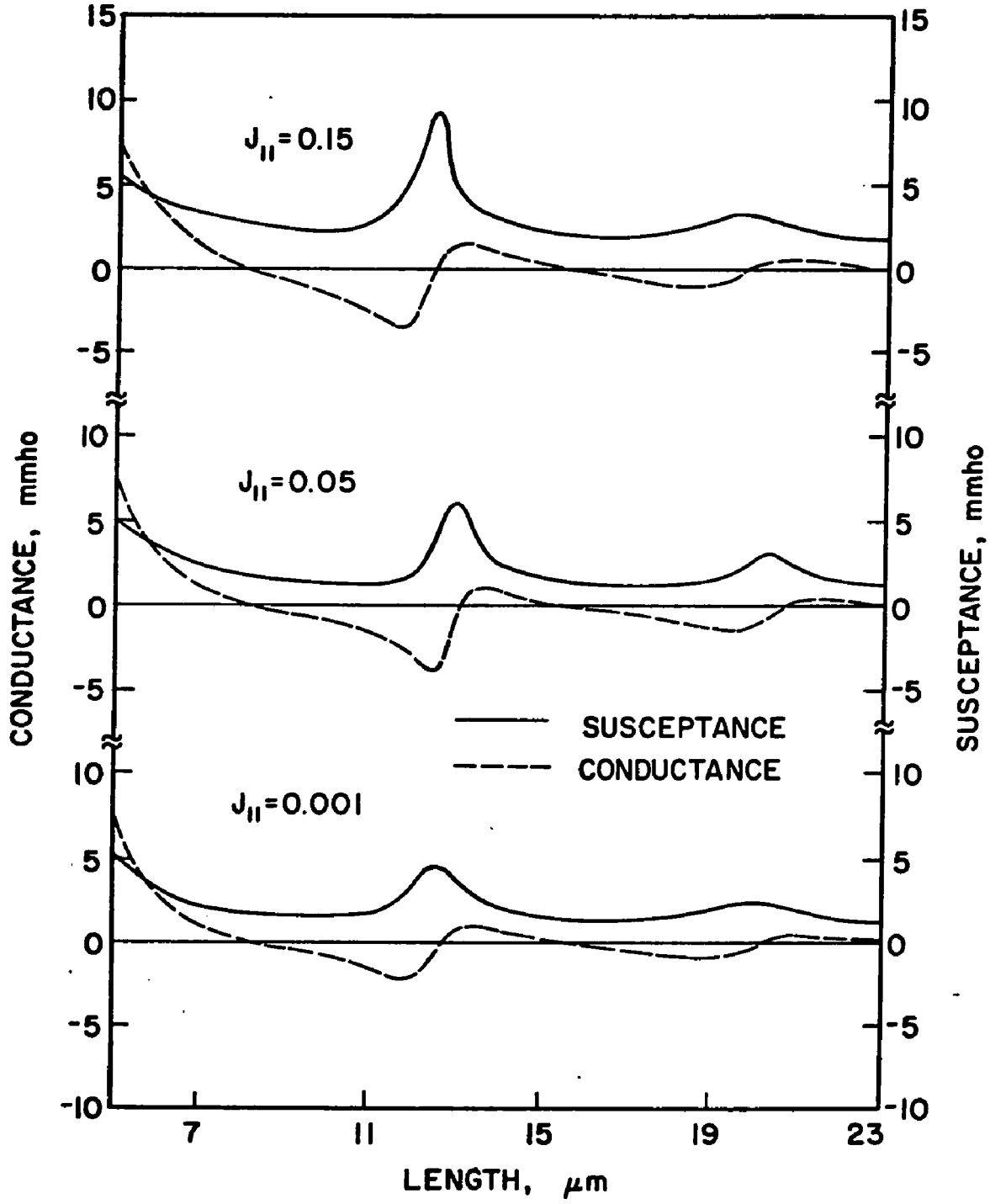


FIG. 4.8 ADMITTANCE VS. LENGTH. (n_o = 5 x $10^{14}/cm^3$, J_o = 1.1, FREQUENCY = 10 GHz, A = 0.7 x 10^{-4} cm^2 AND LATTICE TEMPERATURE = 300°K)

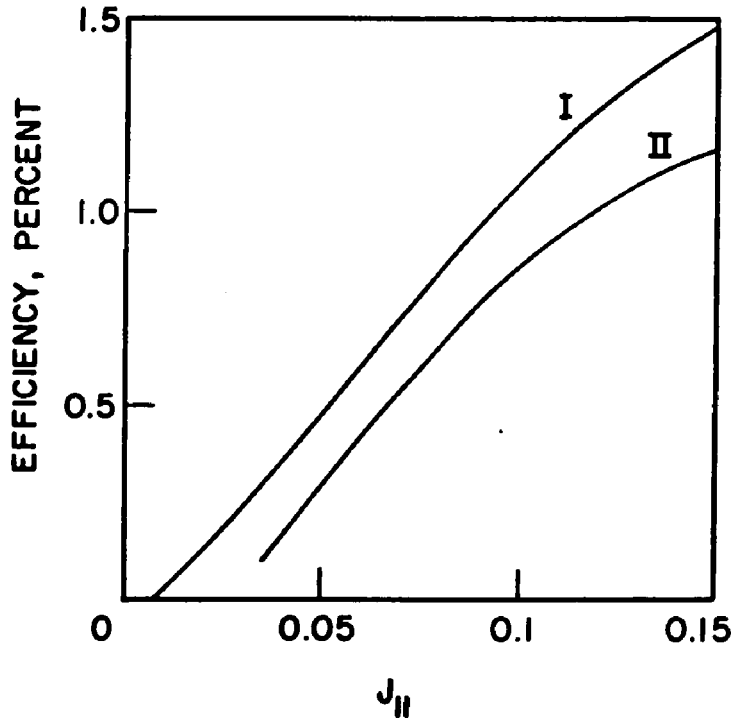


FIG. 4.9 EFFICIENCY VS. J_{11}. CURVE I IS FOR THE DIFFUSION-FREE CASE AND CURVE II IS WITH FIELD-DEPENDENT DIFFUSION INCLUDED. (n_o = $5 \times 10^{14}/cm^3$, J_o = 1.1, FREQUENCY = 10 GHz, LATTICE TEMPERATURE = 300°K AND A = 0.7×10^{-4} cm^2)

Diffusion tends to reduce the amplitude of traveling space-charge accumulation layers. This has the effect of reducing the magnitude of RF negative resistance and the dc to RF conversion efficiency.

CHAPTER V. BANDWIDTH CONSIDERATIONS AND THE EFFECT OF BIAS CONDITIONS ON THE BEHAVIOR OF STABILIZED TRANSFERRED-ELECTRON DEVICES

5.1 Introduction

In the preceding two chapters diffusion-free characteristics of stabilized TE devices have been presented and the effects of diffusion on the static as well as RF characteristics of these devices have been discussed. In this chapter examination is made of the dependence of device impedance on the bias value and the bandwidth of the device negative resistance. These calculations include the effects of diffusion except where otherwise stated.

In order to enable an assessment of the bandwidth capabilities of stabilized TE devices, small- and large-signal impedance calculations were made at different frequencies and the results are presented in Section 5.2. The effects of RF signal level and bias voltage (or current) upon bandwidth are discussed. Small-signal calculations of Hariu et al.[56] have shown that if the cathode contact is nonohmic (resulting in a nonzero value of electric field at the contact), the diode can exhibit negative resistance over several octaves. Such cases have also been examined in Section 5.2.

Section 5.3 discusses the effects of operating bias on the RF impedance and the efficiency of these devices. These results are used to draw conclusions with regard to the effect of bias voltage on the stability of these devices. Several interesting effects that occur at large RF signal levels, such as gain expansion, are studied at various values of bias voltage.

5.2 Bandwidth Considerations

In Chapters III and IV, impedance and admittance of stabilized TE devices were examined with respect to variation in device length for a fixed frequency. In order to study the bandwidth capabilities of these devices, it is necessary to know what happens to the impedance for a constant crystal length as the frequency is varied. Because of the transit-time character of these devices it may be intuitively argued that a slight increase or decrease in frequency of operation would have nearly the same effect as a slight decrease or increase, respectively, in the crystal length. In order to examine this premise the large-signal impedance of a GaAs crystal is plotted against three different abscissae in Fig. 5.1. The crystal parameters and operating conditions are:

$n_o = 5 \times 10^{14}/cm^3$,

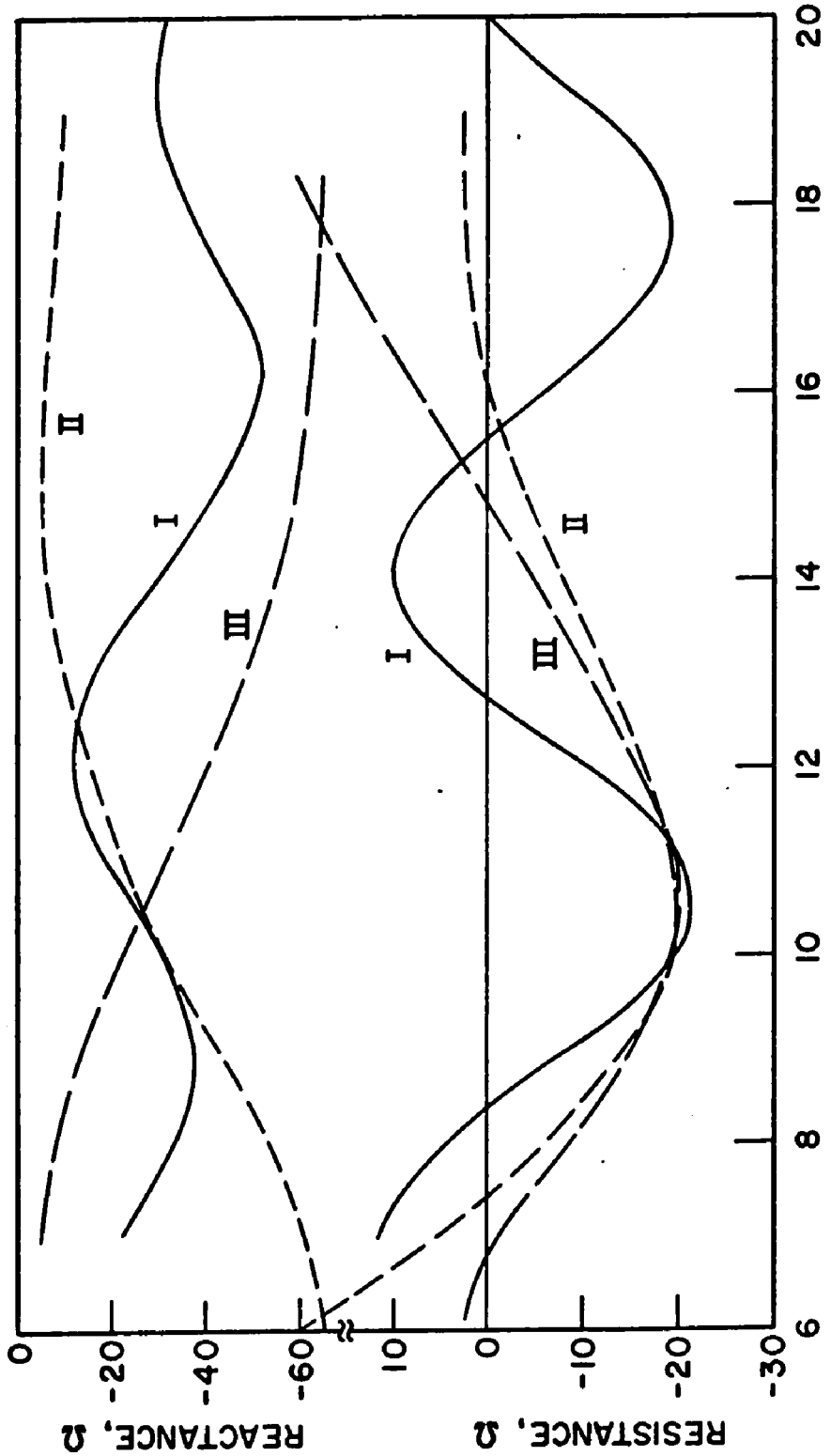
Area $= 0.7 \times 10^{-4}$ cm^2,

Lattice temperature = 375°K,

Normalized bias current $J_o = 1.1$,

Normalized RF current $J_{11} = 0.15$.

The curves labeled I in Fig. 5.1 show the impedance at 10 GHz as a function of crystal length; the curves labeled II represent the impedance for a fixed length of 10.1 μm but as a function of frequency. The impedance is also shown as a function of the inverse of frequency (curves labeled III). The device and operating parameters and abscissae have been chosen so as to obtain the peak of negative resistance at about the same position in the figure. It is clear that the resistance and reactance change more rapidly if the crystal length is varied rather than



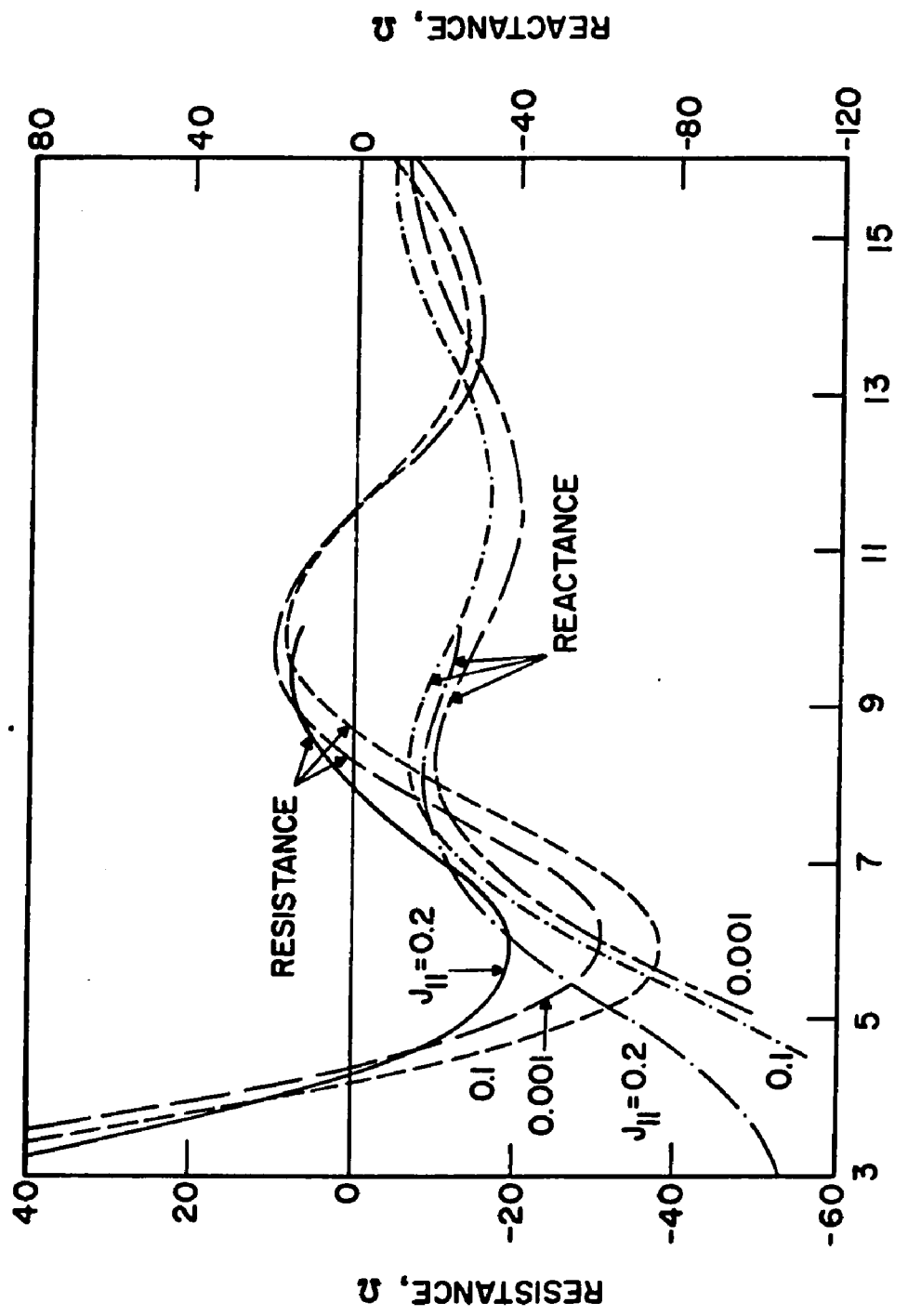
$n_o = 5 \times 10^{14}/cm^3$, $A = 0.7 \times 10^{-3}$ cm^2, Lattice Temperature = 375 Degrees, $J_o = 1.1$, $J_{11} = 0.15$

FIG. 5.1 CRYSTAL RESISTANCE AND REACTANCE. (I) AT 10 GHz VS. DEVICE LENGTH, (II) OF A CRYSTAL 10.1 μm LONG VS. FREQUENCY AND (III) OF A CRYSTAL 10.1 μm LONG VS. 110/FREQUENCY (GHz).

if the frequency is changed. Starting from the peak of negative resistance, a certain percentage change in frequency gives results similar to those obtained by changing the crystal length by about one half of that percentage. The percentage width of the negative-resistance region in curves I is about one half the percentage bandwidth (curves II). Thus there is not a precise quantitative correspondence to frequency bandwidth and only qualitative conclusions should be drawn from calculations made for various crystal lengths. Unfortunately, it causes an investigation of bandwidth to be very expensive since calculation must be made separately at each frequency.

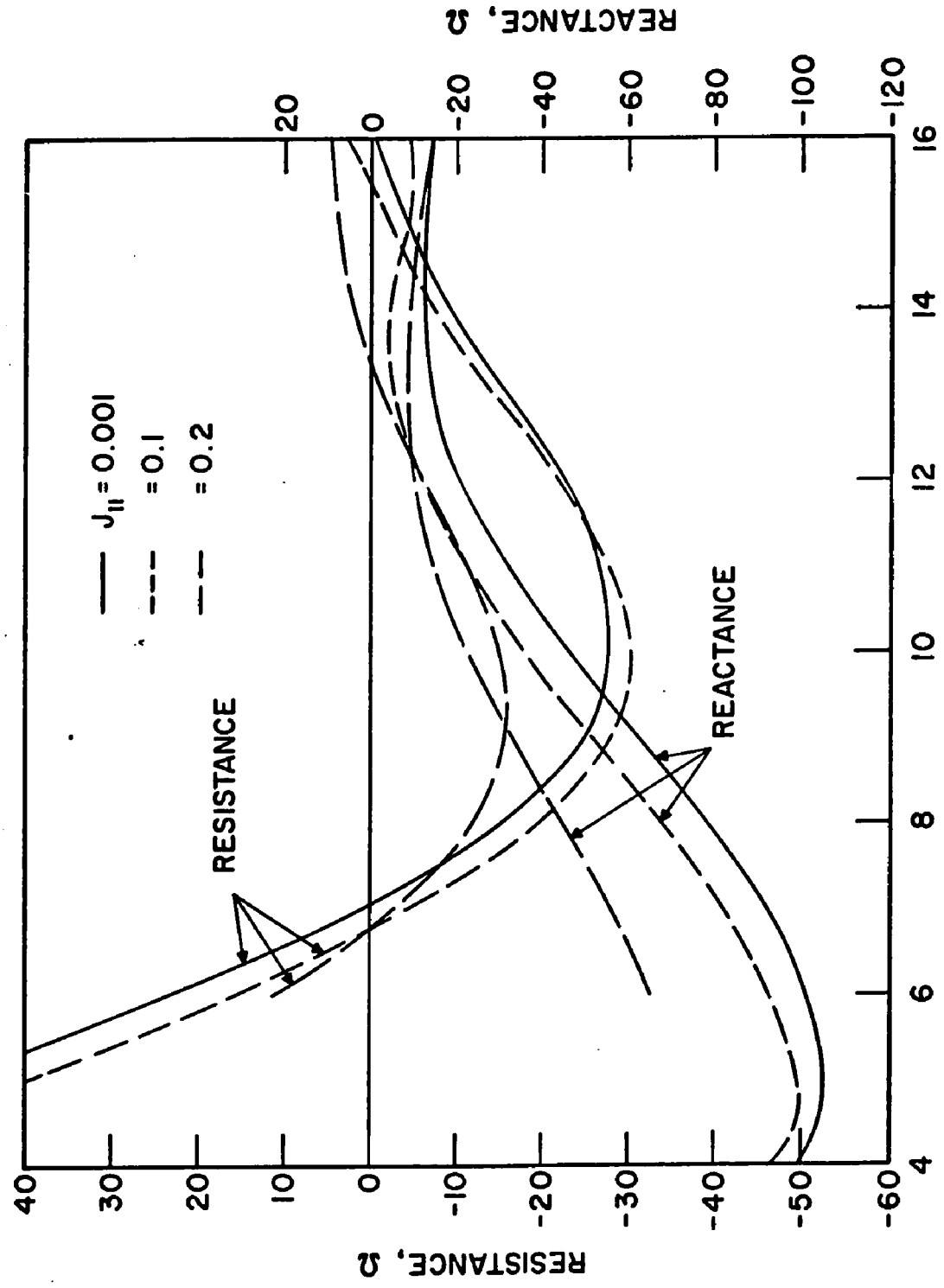
Figure 5.2 shows the resistance and reactance of a 14-μm long crystal with $n_o = 5 \times 10^{14}/cm^3$ plotted as functions of frequency for different values of normalized RF current density and including the effects of diffusion. J_o is taken to be 10 percent above J_{th} and the area is 0.98×10^{-3} cm^2. The impedance plots show two negative-resistance frequency regions which may be used for reflection amplification. The low-frequency region occurs near the transit-time frequency (since 6 GHz times 14 μm is 0.84×10^7 cm/s). As observed before, the magnitude of maximum negative resistance at first increases and then decreases as the RF current density (J_{11}) is increased from a small value. The reactance in the negative resistance region is only about two times the magnitude of negative resistance. This gives a low "Q" for the diode and aids wideband operation.[83]

Figure 5.3 shows a plot similar to that of Fig. 5.2 for a crystal with the same donor density but with a length of 10.1 μm and an area of 7×10^{-4} cm^2. The low-field resistance is kept the same in the two



A = 9.8×10^{-4} cm^2, $n_o = 5 \times 10^{14}$/cm^3, $J_o = 1.1$

FIG. 5.2 RESISTANCE AND REACTANCE OF A 14-μm CRYSTAL AT 300°K VS. FREQUENCY.



l = 10.1 μm, A = 7 x 10^{-4} cm^2, n_o = 5 x $10^{14}/cm^3$, J_o = 1.1

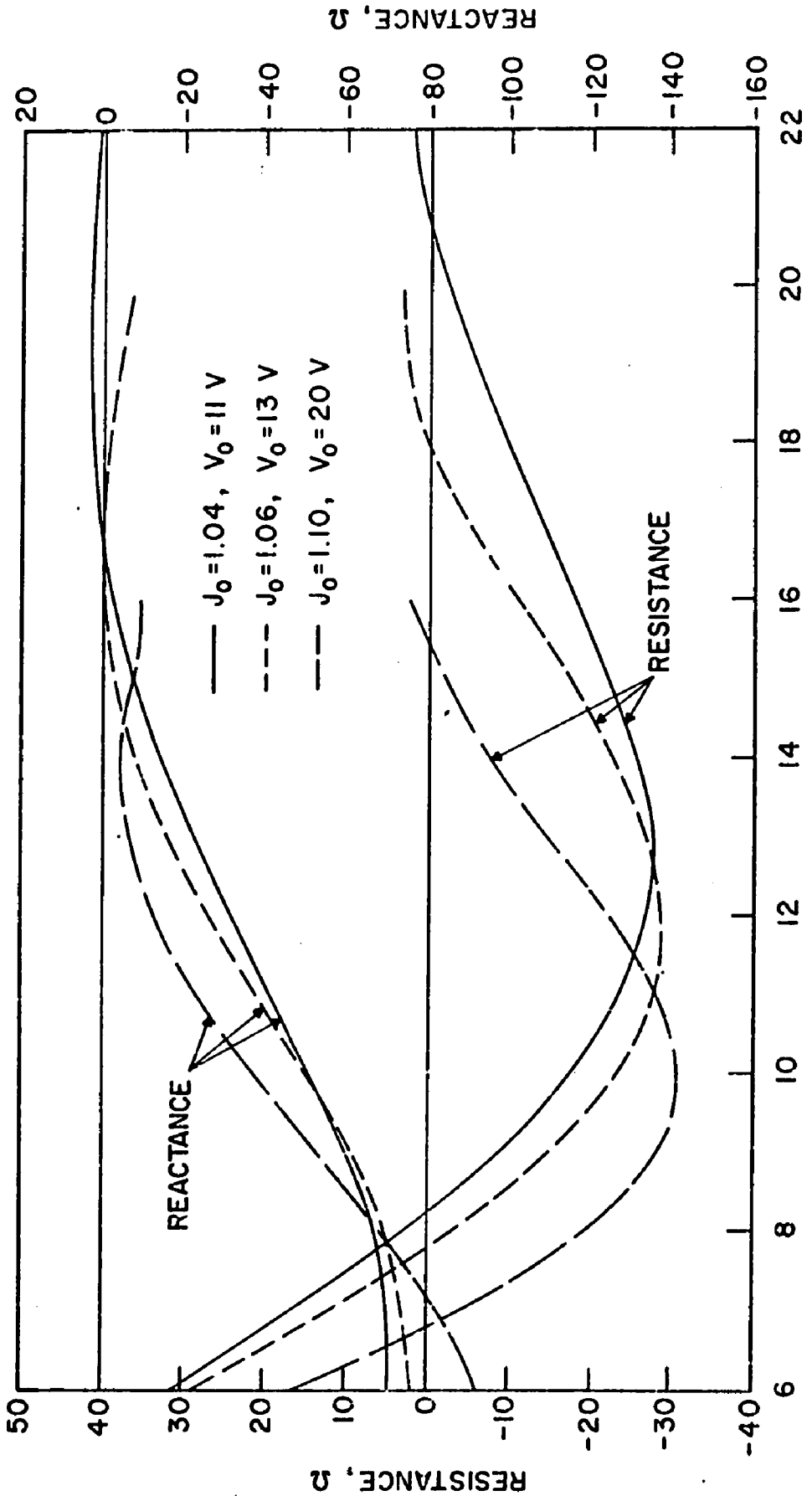
FIG. 5.3 RESISTANCE AND REACTANCE OF A 10.1-μm CRYSTAL AT 300°K VS. FREQUENCY.

cases (approximately 2.5 Ω). The dc current density is also the same. The shorter device (Fig. 5.3) has a slightly smaller magnitude of negative resistance. As expected, the negative-resistance frequency region is shifted to higher frequencies, but notice that the frequency range of this region is larger than that of the longer device, implying that shorter devices may exhibit wider bandwidths. It should be noted in this regard that Magarshack and Mircea[24] have found very large bandwidths for short devices in their small-signal calculations.

The operating bias current or voltage has considerable effect on the bandwidth of these devices and this may be seen in Figs. 5.4a and 5.4b. The resistance and reactance are plotted as functions of frequency at different bias levels for the diode of Fig. 5.3 with $J_{11} = 0.1$. The bandwidth is seen to decrease greatly as the average bias current is increased even though the magnitude of maximum negative resistance increases somewhat. Such behavior has been observed experimentally by Perlman.[22]

At low bias voltages the passive region near the cathode becomes significantly long because of a slower rise in the value of electric field away from the contact. This leads to a shorter active region. Since transit-time effects are important in these devices, the negative-resistance region occurs at higher RF frequencies at lower bias voltages as shown clearly in Fig. 5.4b. Such a shift in the frequency band of negative resistance can be seen in the experimental results of Perlman[22] and was also observed by Thim.[33]

At $J_o = 1.04$ in Fig. 5.4a the reactance is seen to change sign at approximately 17 GHz. At that operating point the diode impedance is a



A = 7 x 10^{-4} cm^2, n_o = 5 x $10^{14}/cm^3$, J_{11} = 0.1, Lattice Temperature = 300°K

FIG. 5.4a RESISTANCE AND REACTANCE OF A 10.1-μm LONG CRYSTAL VS. FREQUENCY.

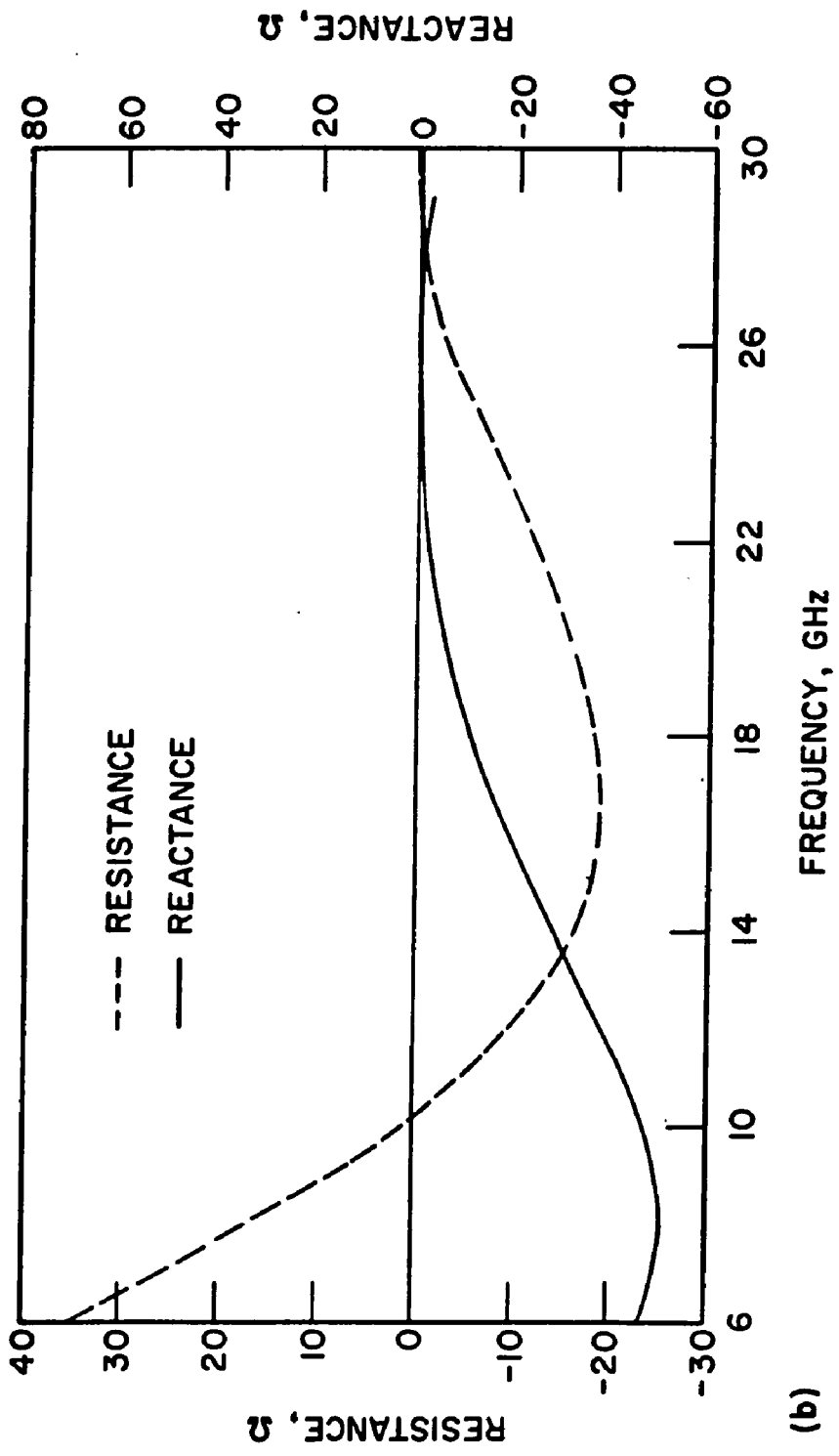


FIG. 5.4b RESISTANCE AND REACTANCE OF A 10.1-μm LONG CRYSTAL VS. FREQUENCY.

$A = 7 \times 10^{-4}$ cm^2, $n_o = 5 \times 10^{14}$/cm^3, $J_o = 1.02$, $J_{11} = 0.1$, Lattice Temperature = 300°K, Bias Voltage = 5.5

pure negative resistance. Earlier, it was observed (in Figs. 3.7 and 4.8) that the sign change did not occur when diffusion effects were included. The present case (with diffusion included) demonstrates that diffusion does not prevent such a possibility.

Under certain conditions it is possible to get negative resistance over very wide frequency bands as shown in Fig. 5.5, which is for the same device parameters as those of Fig. 5.3 but is for $J_o = 1.09$. However, such behavior is limited to relatively small signal levels. At $J_{11} = 0.1$, the resistance becomes positive around 18 GHz. At high frequencies, near 30 GHz, intervalley scattering times become important[71] and the negative resistance calculated in Fig. 5.5 at these frequencies would probably not exist in practice.

Small-signal calculations of Hariu et al.[56] have shown that negative resistance is possible over several octaves in diodes with injection-limited cathodes or when the cathode field is above the threshold value so that the passive region near this contact is eliminated. They have assumed static field to be uniform and diffusion effects have been neglected. Nonuniformity of the electric field can lead to a passive region near the anode and this along with diffusion would cause a reduction in the negative-resistance magnitude. However, calculations based on the present theory (in which the static field is not assumed constant and diffusion effects are included) show that such performance is still possible at small signal levels and at relatively low bias voltages, as shown in Fig. 5.6. The device and operating parameters are:

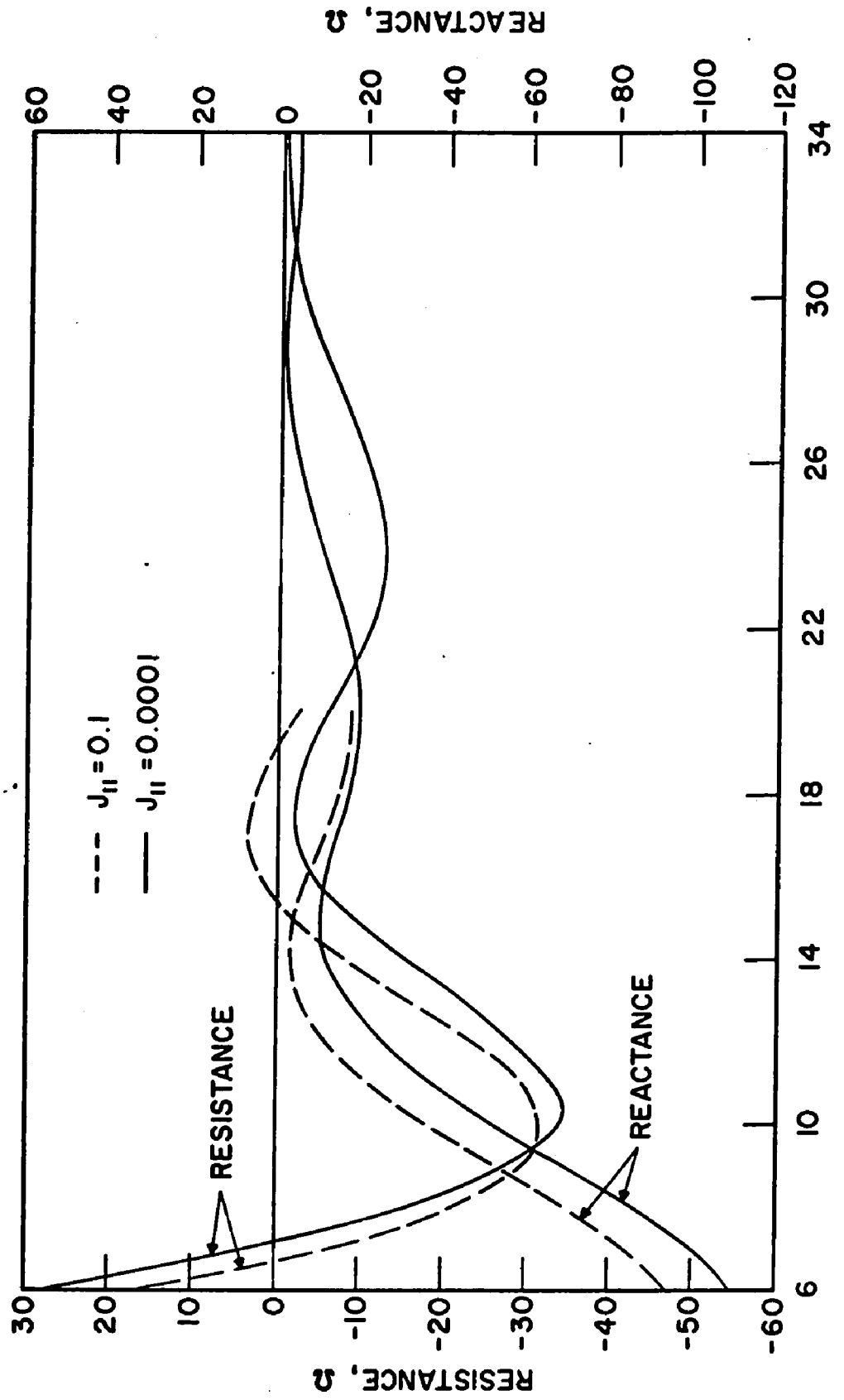
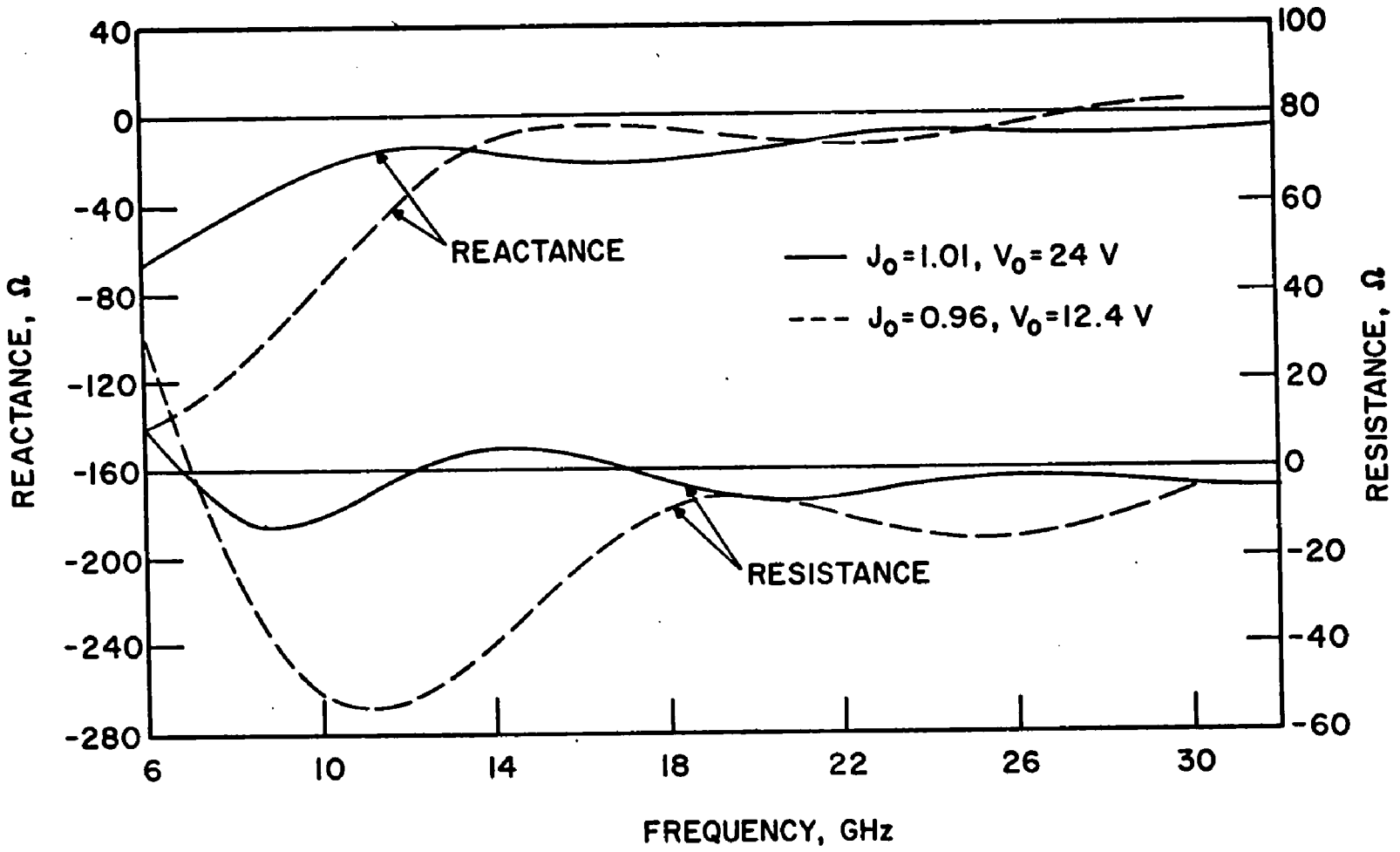


FIG. 5.5 RESISTANCE AND REACTANCE OF A 10.1-μm DIODE AT 300°K VS. FREQUENCY FOR $V_o = 16$ V AT $J_{11} = 0.0001$.



$n_o = 5 \times 10^{14}/cm^3$, $A = 7 \times 10^{-4}$ cm^2, Lattice Temperature = 300°K, $J_o = 0.96$ ($V_o = 12.4$ V), $J_o = 1.01$ ($V_o = 24$ V)

FIG. 5.6 SMALL-SIGNAL ($J_{11} = 0.0001$) RESISTANCE AND REACTANCE OF AN 8.6-μm DIODE VS. FREQUENCY WITH THE STATIC ELECTRIC FIELD AT THE CATHODE = 5 kV/cm.

$n_o = 5 \times 10^{14}/cm^3$,

$\ell = 8.6\ \mu m$,

$A = 0.7 \times 10^{-4}\ cm^2$,

$J_{11} = 0.0001$.

The cathode field is arbitrarily chosen to be 5 kV/cm.

The plots are restricted to approximately 30 GHz because, as stated before, the negative resistance beyond this frequency is expected to be less than calculated. The case for $J_o = 0.96$ shows that amplification over the frequency band 8 to 30 GHz is possible. Even though the negative resistance near 20 GHz and above is small, significant gain may still be obtainable because of the small value of reactance.

The performance of Fig. 5.6 will be limited, as in Fig. 5.5, to relatively small signal levels, despite the absence of the passive region near the cathode contact. This is shown in Fig. 5.7 where small- and large-signal ($J_{11} = 0.1$) results are compared for the device of Fig. 5.6. The normalized bias current density is 0.96 and bias voltage is 12.4 V for both small- and large-signal cases.

The effect of bias on the bandwidth of a device with cathode field above the threshold is shown in Figs. 5.8a and 5.8b. The device parameters are:

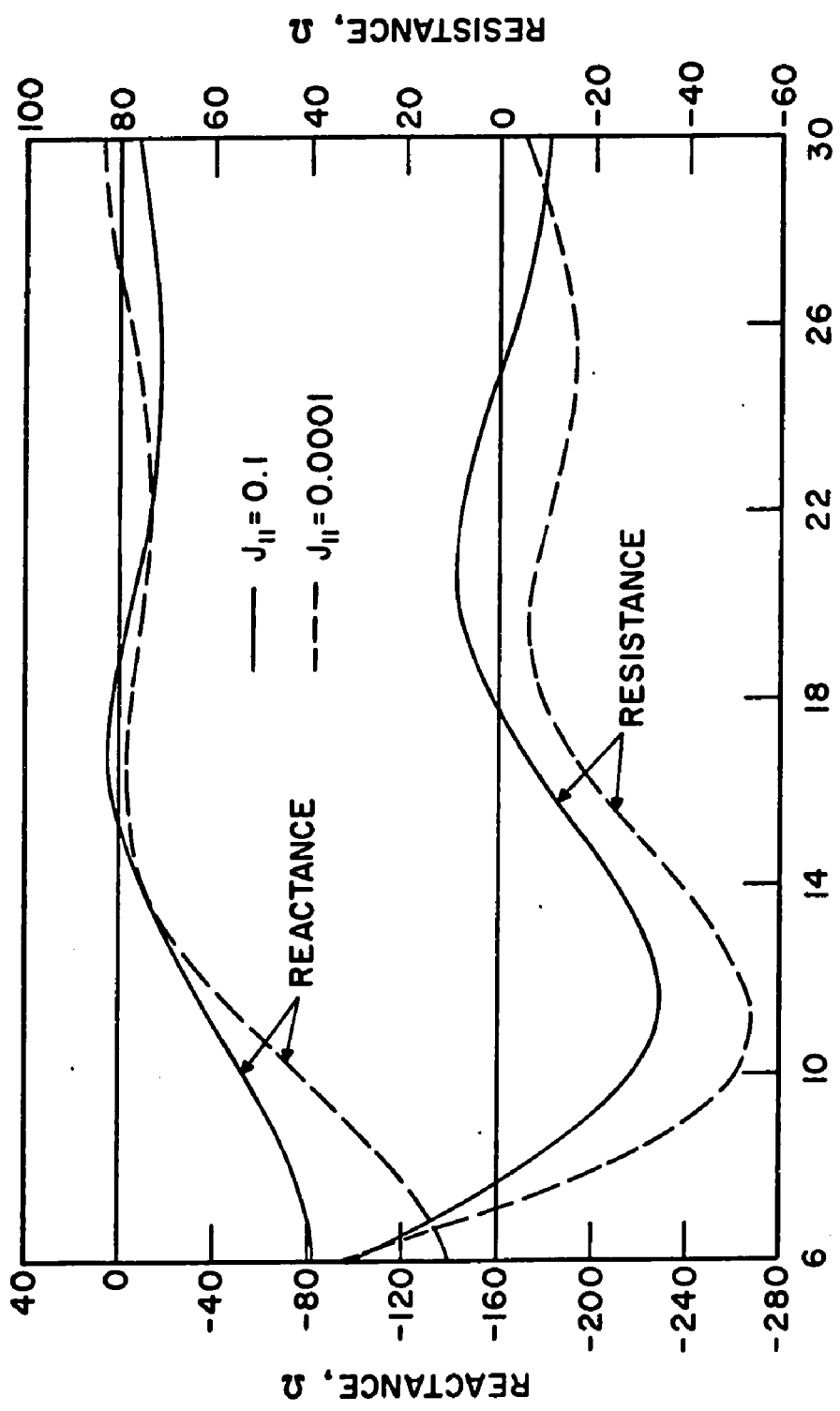
$n_o = 5 \times 10^{14}/cm^3$,

$\ell = 10.1\ \mu m$,

Electric field at cathode = 5 kV/cm,

$J_{11} = 0.1$,

$A = 0.7 \times 10^{-3}\ cm^2$.



V_o = 12.4 V for Both J_{11} = 0.0001 and J_{11} = 0.1

FIG. 5.7 SMALL- AND LARGE-SIGNAL RESISTANCE AND REACTANCE OF THE DIODE OF FIG. 5.6 VS. FREQUENCY FOR J_o = 0.96.

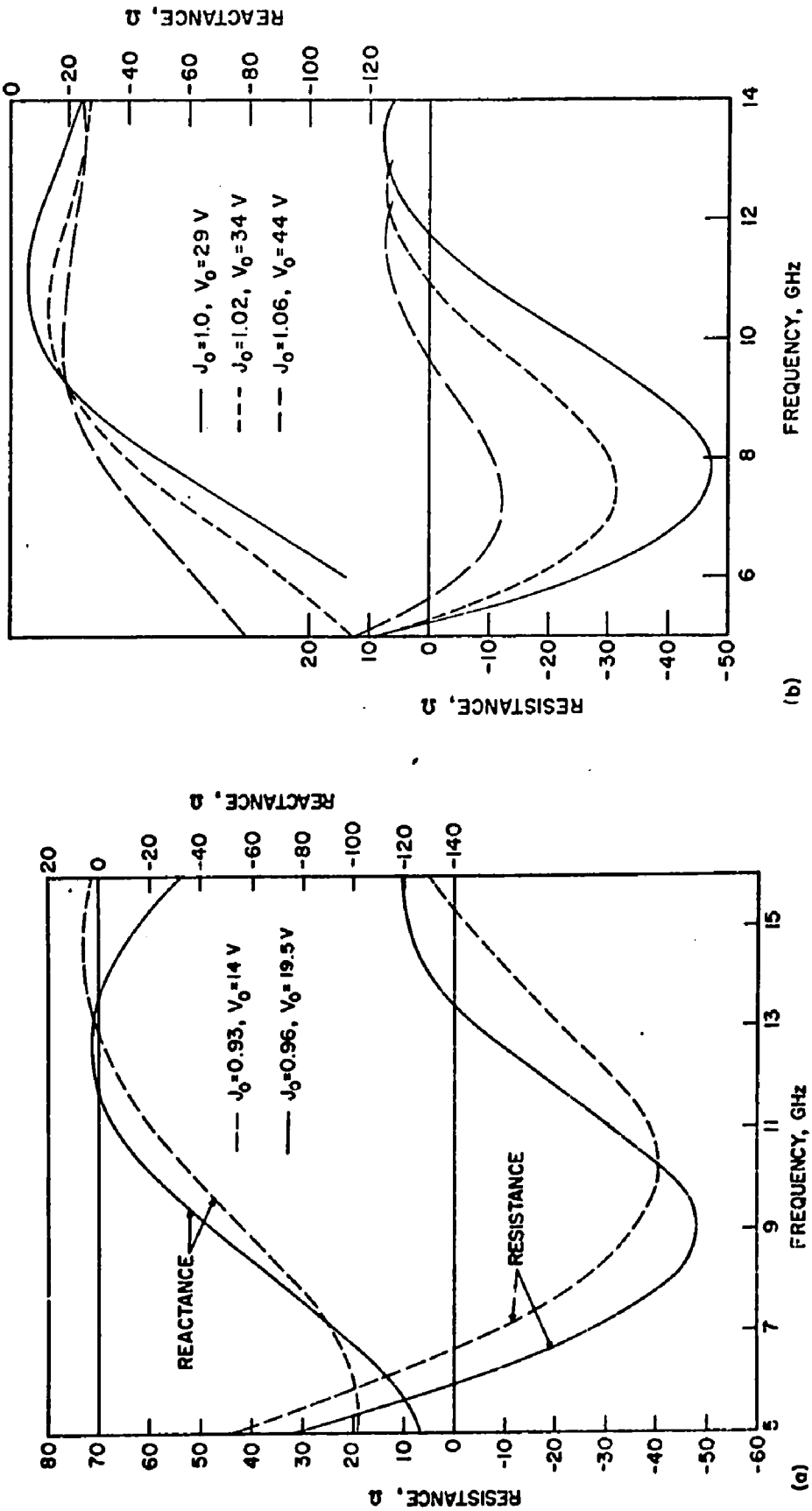


FIG. 5.8 LARGE-SIGNAL (J_{11} = 0.1) RESISTANCE AND REACTANCE OF A 10.1-μm DIODE VS. FREQUENCY. THE ELECTRIC FIELD AT THE CATHODE IS 5 kV/cm.

$n_o = 5 \times 10^{14}/cm^3$, $A = 7 \times 10^{-4}$ cm^2, Lattice Temperature = 300°K

As in the case of a diode with an ohmic cathode contact or zero cathode field (Figs. 5.4a and 5.4b), the bandwidth decreases as the bias is increased. However, the downward shift in the negative-resistance frequency region at higher bias voltages, is much smaller in the present case. This is because of the absence of a passive region near the cathode.

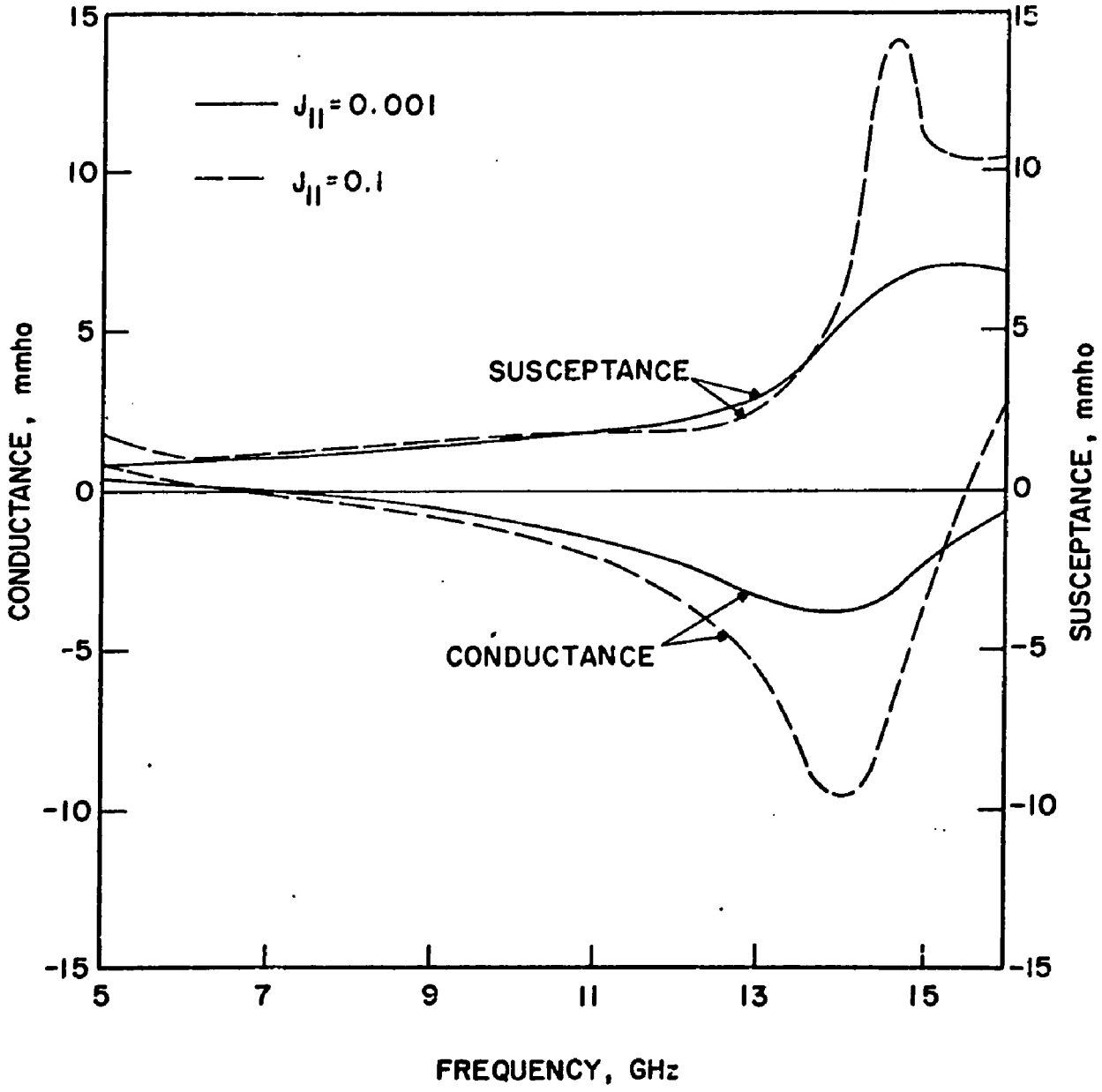
Notice that the magnitude of the maximum negative resistance at first increases, then decreases as the bias is increased from a small value. This "peaking" of the negative resistance will be discussed in greater detail in the next section.

An example of negative conductance and susceptance plotted as functions of frequency is given in Fig. 5.9 which is for a crystal similar to that of Fig. 5.3 but with area = 0.7×10^{-4} cm^2. The curves resemble the experimental observations of Perlman et al.[84]

5.3 Effects of Operating Bias on Impedance and Efficiency

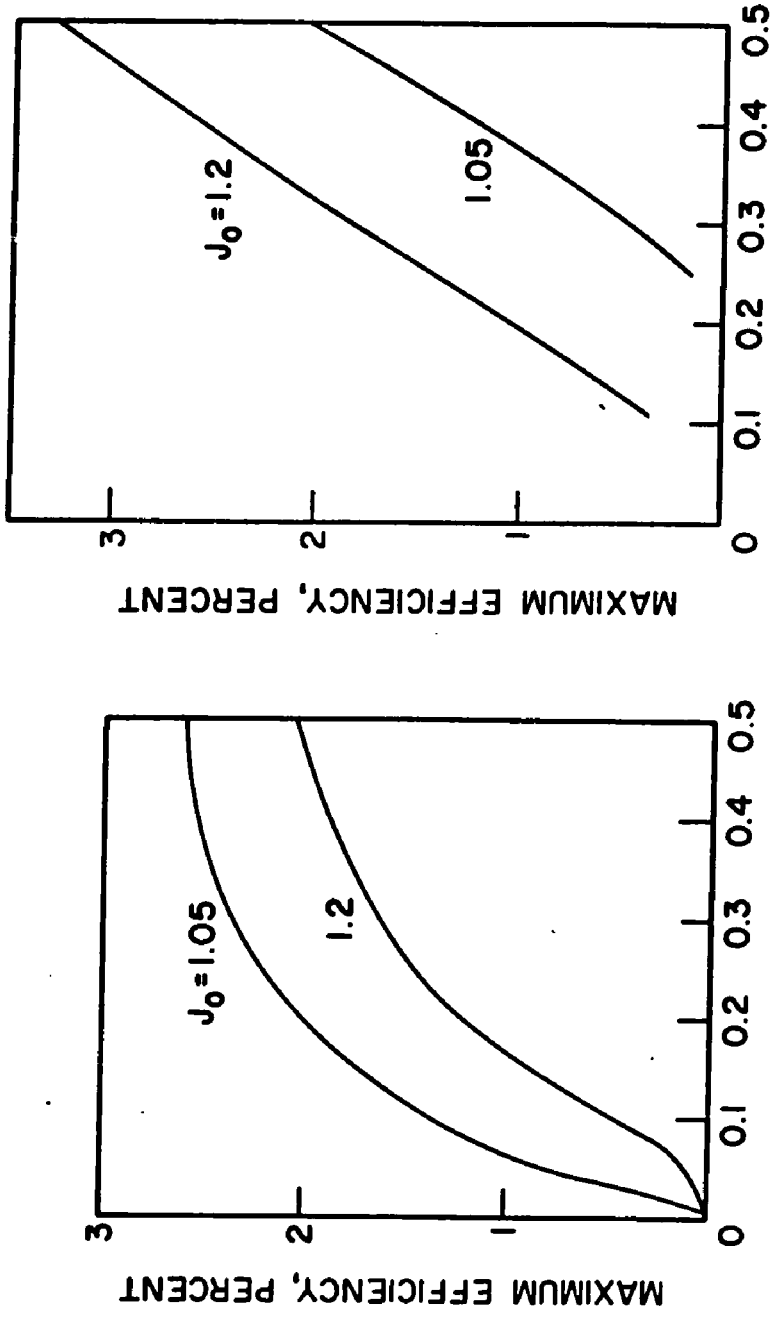
The static-field profile along the length of the GaAs crystal depends on the bias voltage across it or the dc current flowing through it. Consequently, bias conditions influence the differential as well as the absolute mobility of carriers at each point along the crystal length. Thus device performance varies significantly with bias conditions.

Figure 5.10 shows the relationship between best efficiency (for optimum device length) and J_{11} for a crystal of high $n_o \ell$ product (Fig. 5.10a) and for a crystal of low $n_o \ell$ product (Fig. 5.10b). Each case is plotted for two different bias values. The corresponding static-field configurations are shown in Fig. 5.11. Notice that when the



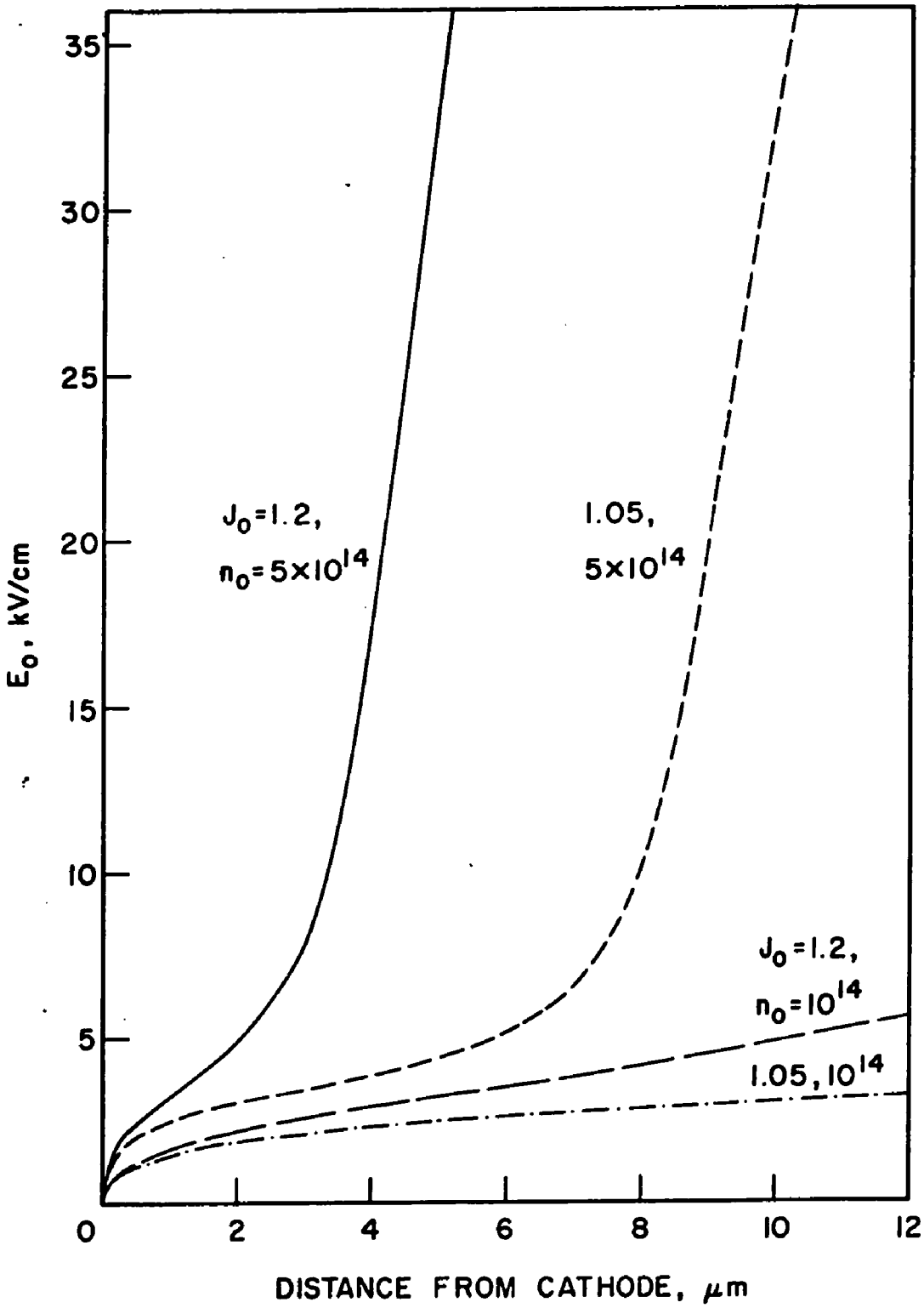
$n_o = 5 \times 10^{14}/cm^3$, $A = 0.7 \times 10^{-4}$ cm^2, Lattice Temperature = 300°K, $J_c = 1.1$

FIG. 5.9 CONDUCTANCE AND SUSCEPTANCE OF A 10-μm DIODE VS. FREQUENCY.



Lattice Temperature = 300°K

FIG. 5.10 MAXIMUM EFFICIENCY VS. J_{11} AT 10 GHz WITH DIFFUSION EFFECTS NEGLECTED.



Lattice Temperature = 300°K

FIG. 5.11 STATIC ELECTRIC FIELD VS. DISTANCE FROM THE CATHODE FOR J_{11} = 0.001 WITH DIFFUSION EFFECTS NEGLECTED.

static-field distortion is initially low, efficiency increases with increase of bias current. This is the case of Fig. 5.10b. However, the opposite is true when the static-field distortion is initially large (Fig. 5.10a).

The reason for this behavior can be understood by examining the static-field profiles shown in Fig. 5.11. Because the differential mobility is negative only in the electric field range from the threshold to approximately 15 kV/cm, the parts of the crystal which are above 15 kV/cm or below threshold are passive. Such a region exists near the cathode and another one may exist near the anode depending on whether the electric field there is high enough. At low bias levels, the passive region near the anode is nonexistent (Fig. 5.11) and the length of the passive cathode region is significant. An increase in bias reduces the length of the passive cathode region, and if the bias is still low enough, the passive anode region does not appear. Also, the electric field along most of the device goes toward the middle of the negative-differential mobility region of the v-E characteristic. These factors cause an increase in efficiency. On the other hand, when a large static-field distortion is present, the passive cathode region is small and there is a significant region near the anode which is passive (Fig. 5.11). An increase in bias causes an increase in the length of the anode passive region without affecting the length of the cathode region, causing a reduction in efficiency.

The preceding discussion indicates that the efficiency, as well as the negative-resistance magnitude, must go through a maximum as the bias is increased from a small value to a large value. This indeed

is the case as shown in Fig. 5.12 where best efficiency and maximum negative resistance are plotted as functions of normalized dc bias current density and for two different values of normalized RF current density. The optimum crystal length was chosen to obtain the maxima. Notice that negative resistance is obtained even for values of bias current below the threshold value of $J_o = 1$. This is possible at large signal levels and such operation will be discussed later in this section.

In practical devices, where the crystal length is fixed, the range of bias current values over which negative resistance is obtained is limited. Figure 5.13 shows the efficiency, resistance and reactance of three crystals of different lengths but with the same material parameters, area, frequency and RF current density as follows:

$n_o = 5 \times 10^{14}$,

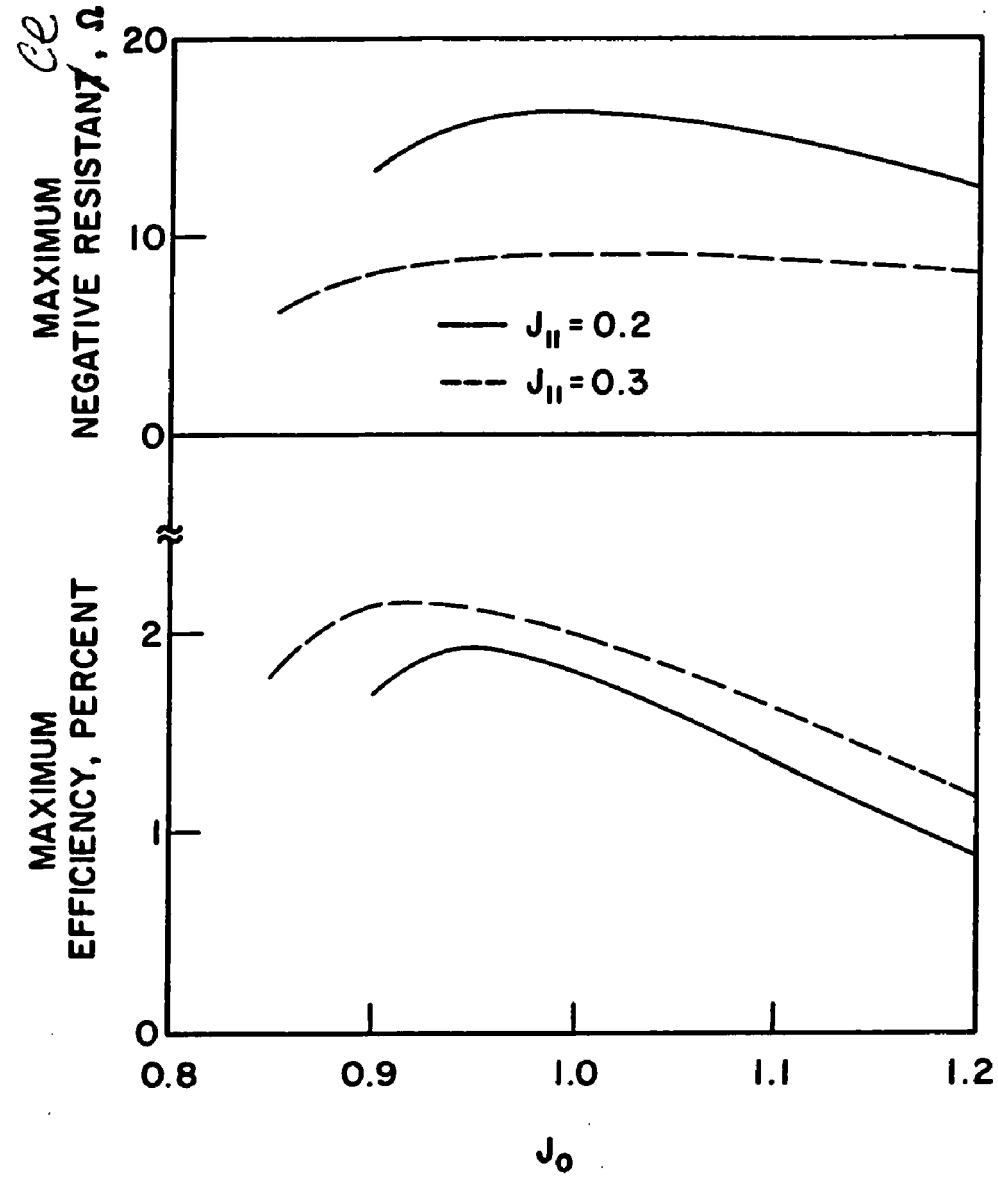
Lattice temperature = 300°K,

Area = 7×10^{-4} cm^2,

Frequency = 10 GHz,

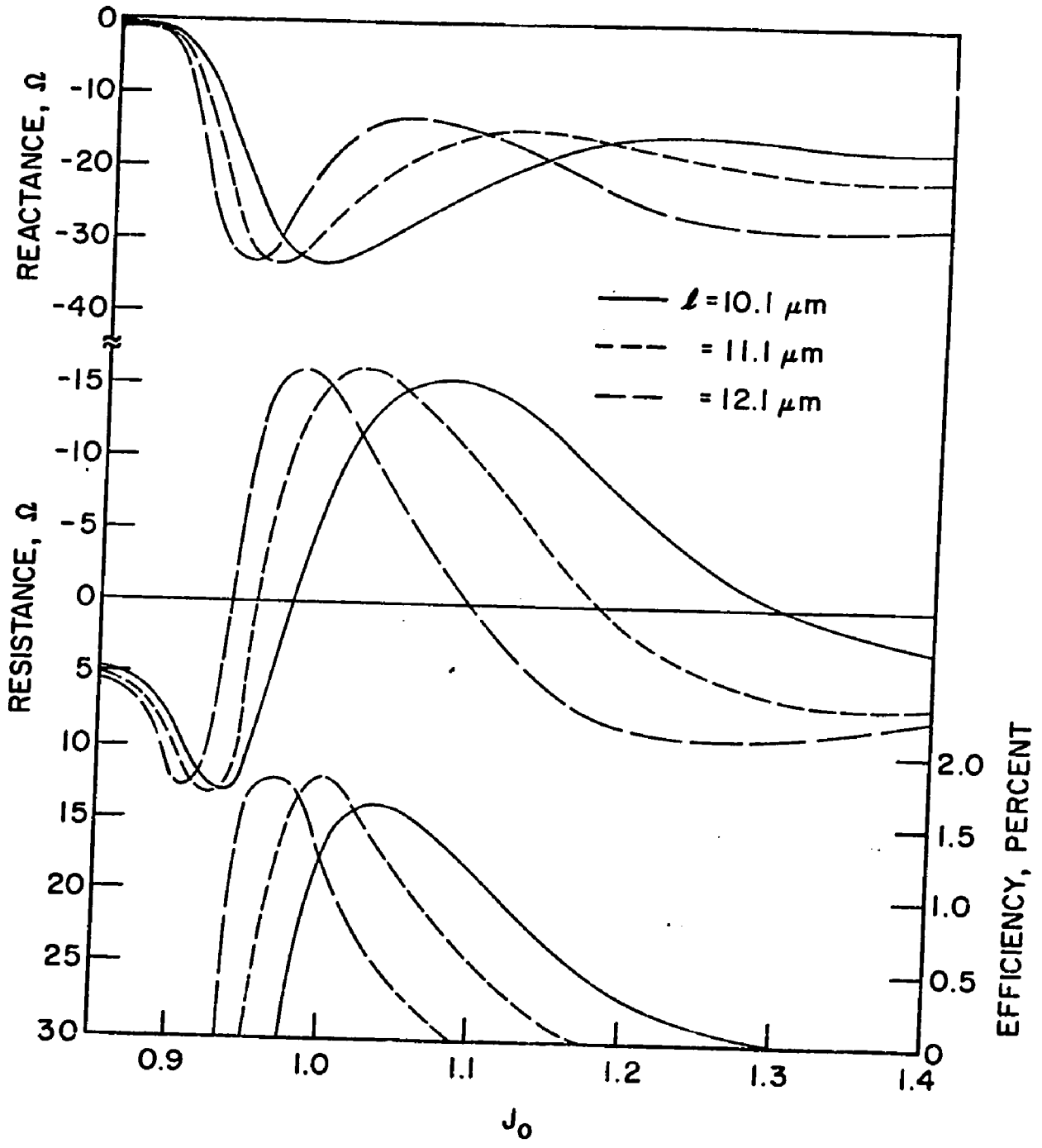
$J_{11} = 0.2$.

Notice that the negative resistance vanishes at very high bias levels. This is because of the large passive region close to the anode. For constant bias current density, the longer the crystal, the longer is this region. This explains why shorter devices continue to exhibit negative resistance at values of J_o greater than those for longer devices (Fig. 5.13). At low values of J_o, however, the negative differential mobility region extends to the anode, and the shorter the



$n_o = 5 \times 10^{14}/cm^3$, Lattice Temperature = 300°K

FIG. 5.12 MAXIMUM EFFICIENCY AND NEGATIVE RESISTANCE AT 10 GHz VS. BIAS CURRENT DENSITY.



$n_o = 5 \times 10^{14}/cm^3$, $A = 7 \times 10^{-4}$ cm^2, Frequency = 10 GHz,

Lattice Temperature = 300°K, $J_{11} = 0.2$

FIG. 5.13 EFFICIENCY, RESISTANCE AND REACTANCE OF THREE DIODES OF DIFFERENT LENGTHS VS. J_o.

crystal, the shorter is this region. Thus the shorter devices exhibit a smaller magnitude of negative resistance, or have positive resistance for values of J_o for which longer devices may show negative resistance.

The decrease in the magnitude of negative resistance at high bias voltages should aid circuit stabilization of these devices. Perlman et al.[84] have reported that for devices of relatively high $n_o l$ products, stabilization is attained only above a certain bias voltage which is several times the threshold value. The relationship between the voltage across the crystal and the normalized current density is plotted for the three cases of Fig. 5.13 in Fig. 5.14. Quite naturally, the longer crystals have greater voltage drops across them for the same current density. Considering that negative resistance is initiated at lower values of J_o for longer devices, it is interesting to note that the maximum voltage at which negative resistance is obtained for the three crystals turns out to be the same. In fact if the data of Fig. 5.13 are replotted as functions of voltage, as in Fig. 5.15, the three sets of curves are almost superimposed on one another. In other words, for devices designed to operate at a single frequency and in a constant voltage bias circuit, there is a certain tolerance allowable in the crystal length.

However, the minimum bias voltage at which negative resistance appears does depend on the signal strength. Figures 5.16a and 5.16b show the negative resistance and reactance, respectively, of a 10.1-μm long crystal with the area of cross section, doping density and frequency of operation the same as those of Fig. 5.15 and operated at room temperature. The curves are plotted for different values of J_{11}. The

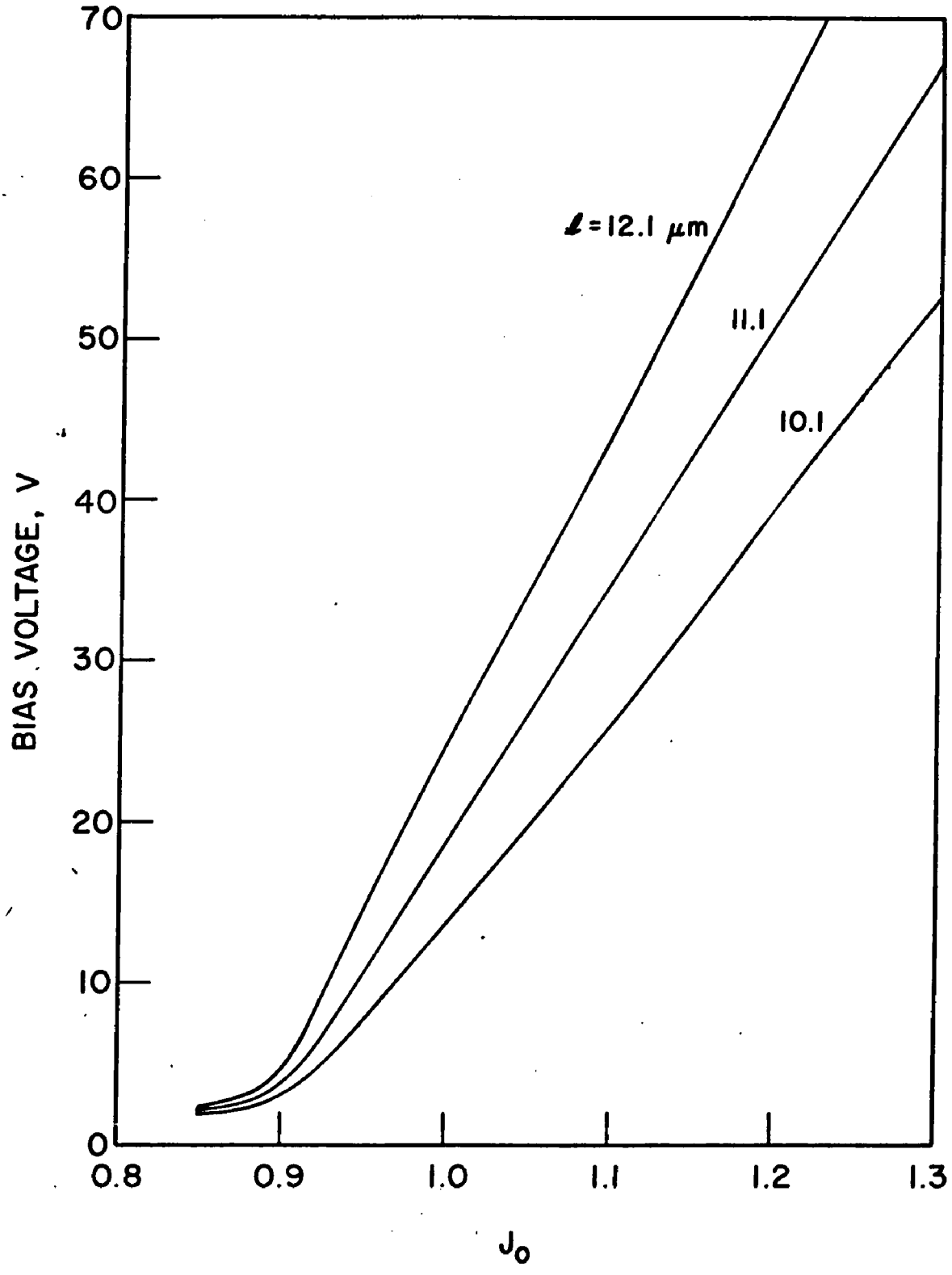


FIG. 5.14 BIAS VOLTAGE ACROSS THE DIODE VS. J_o FOR THE THREE DIODES AND OPERATING CONDITIONS OF FIG. 5.13.

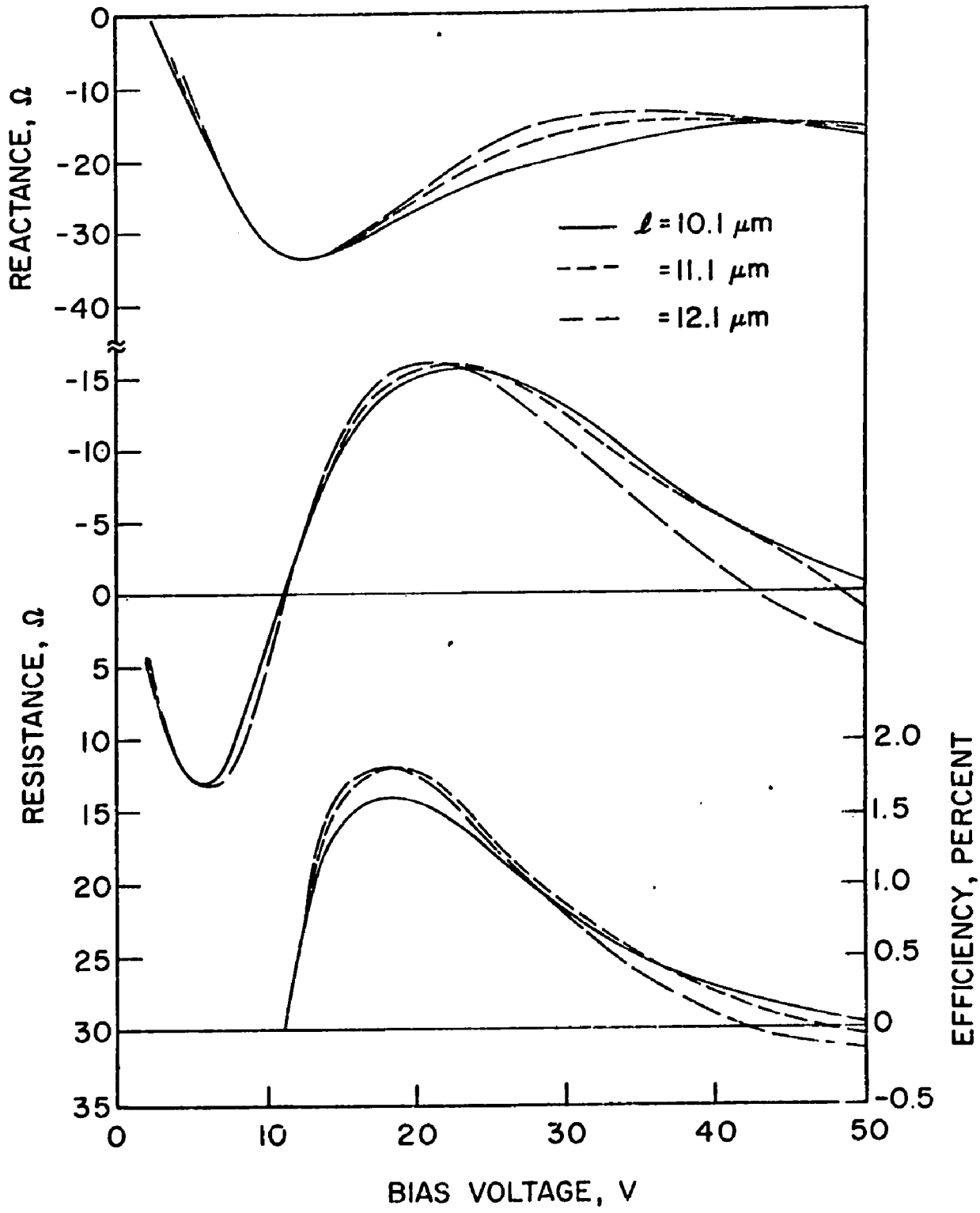
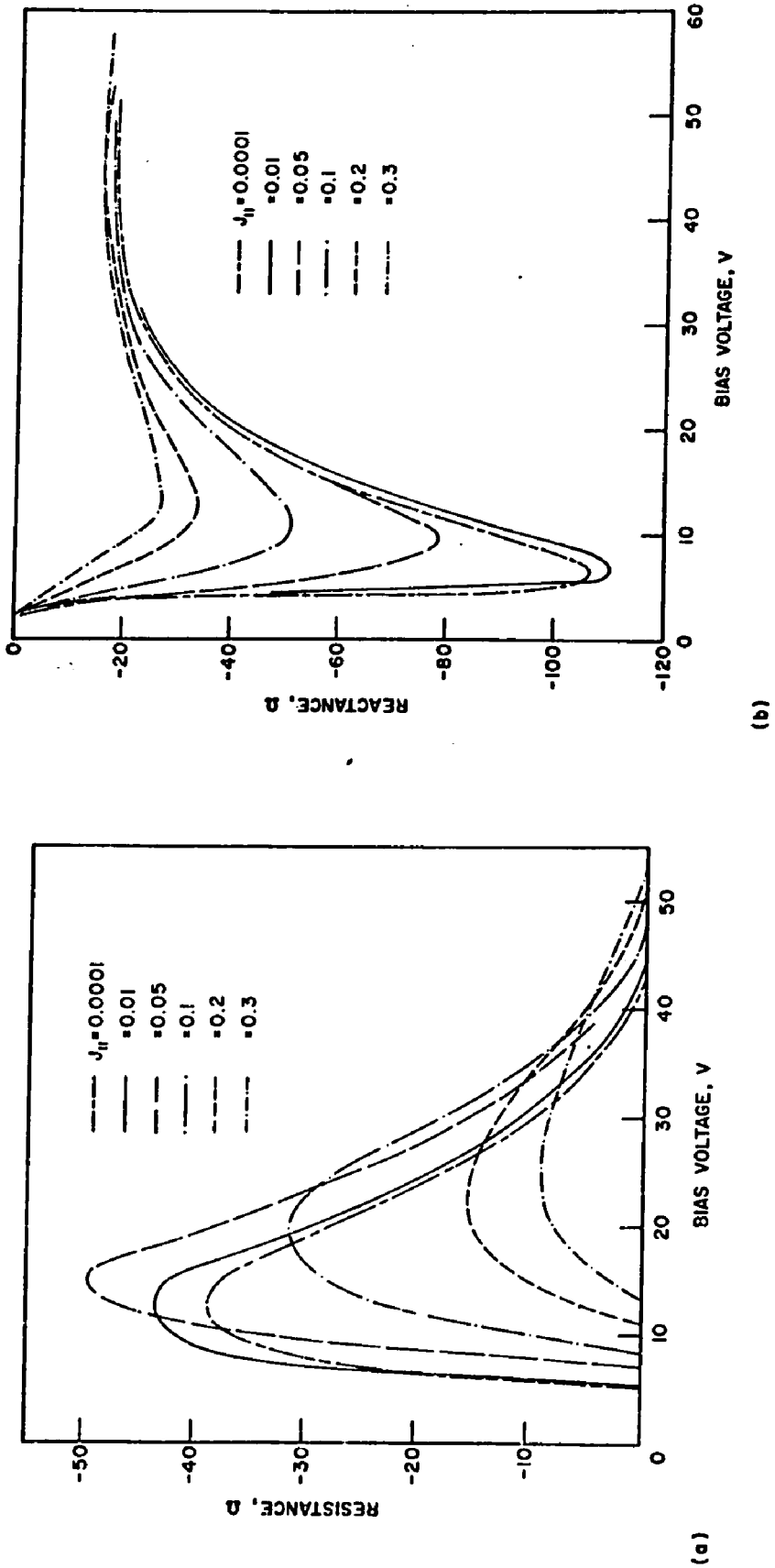


FIG. 5.15 THE DATA OF FIG. 5.13 VS. BIAS VOLTAGE.



$n_o = 5 \times 10^{14}/cm^3$, $A = 7 \times 10^{-4}\ cm^2$, Lattice Temperature = 300°K

FIG. 5.16 RESISTANCE AND REACTANCE OF A 10.1-μm DIODE AT 10 GHz VS. BIAS VOLTAGE.

corresponding values of dc to RF conversion efficiency are plotted in Fig. 5.17. The higher the signal level, the greater is the minimum bias voltage at which the negative resistance appears. The maximum of the negative resistance goes through a peak as the RF current density is increased from a small value. An examination of Fig. 5.16a shows that, for a constant bias voltage, the negative resistance also goes through a maximum as J_{11} is varied, just as it does for constant J_o as discussed previously (Fig. 3.8).

The "peaking" of negative-resistance magnitude when J_{11} is varied is seen more clearly in Figs. 5.18a and 5.18b where the resistance and reactance of the device of Fig. 5.16 are plotted as functions of J_{11} for different bias voltages. The peak of the negative-resistance magnitude occurs at low values of J_{11} at low bias voltages and at higher values of J_{11} at higher bias voltages. In fact, the value of J_{11} at which this occurs for relatively low bias voltages is so small that this effect may not be observed under usual experimental conditions. It should be more evident at high biases. In fact, the peaking is quite evident at higher bias values in the experimental study of TE amplifiers by Sene and Rosenbaum.[81] Here a region of "gain expansion" is observed as the RF input power is increased. At larger RF input power the usual "gain compression" (or reduction of gain) is observed.

It was pointed out earlier in this section that negative resistance can be obtained at bias current densities below threshold. This occurs only for large RF signal levels. In Chapter III it was shown that static-field distortion is high when the RF current density is

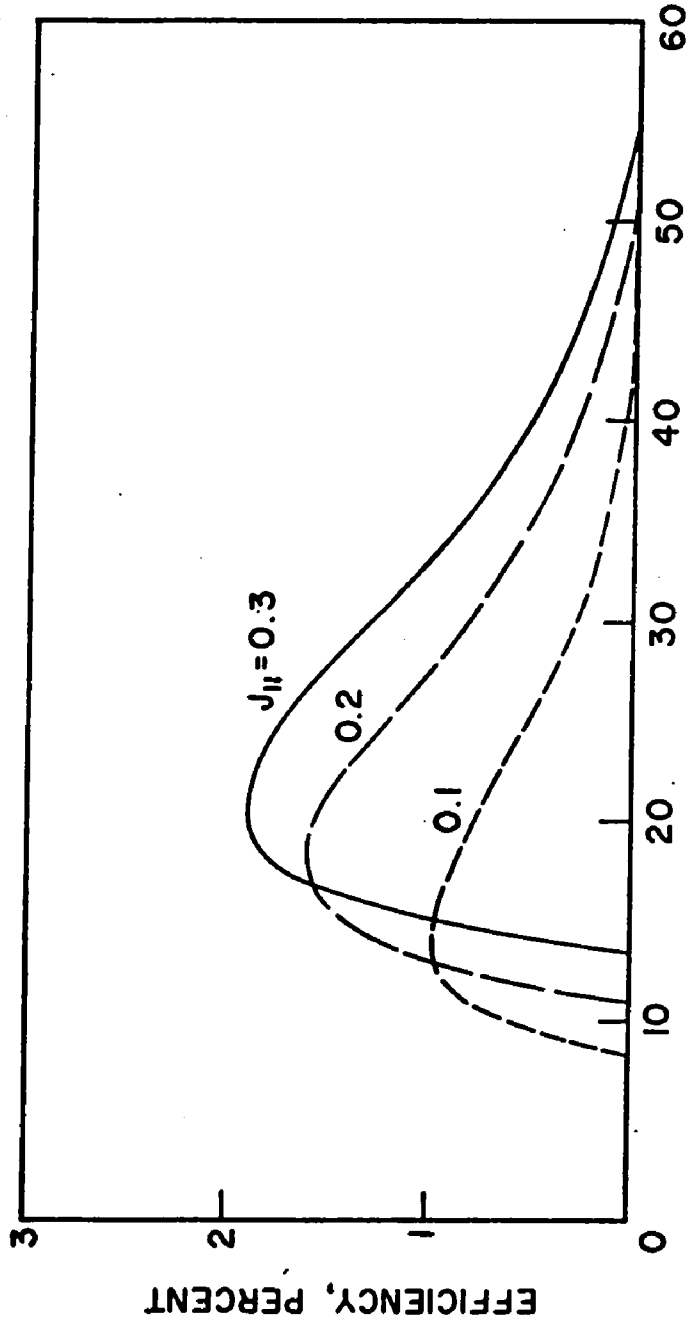
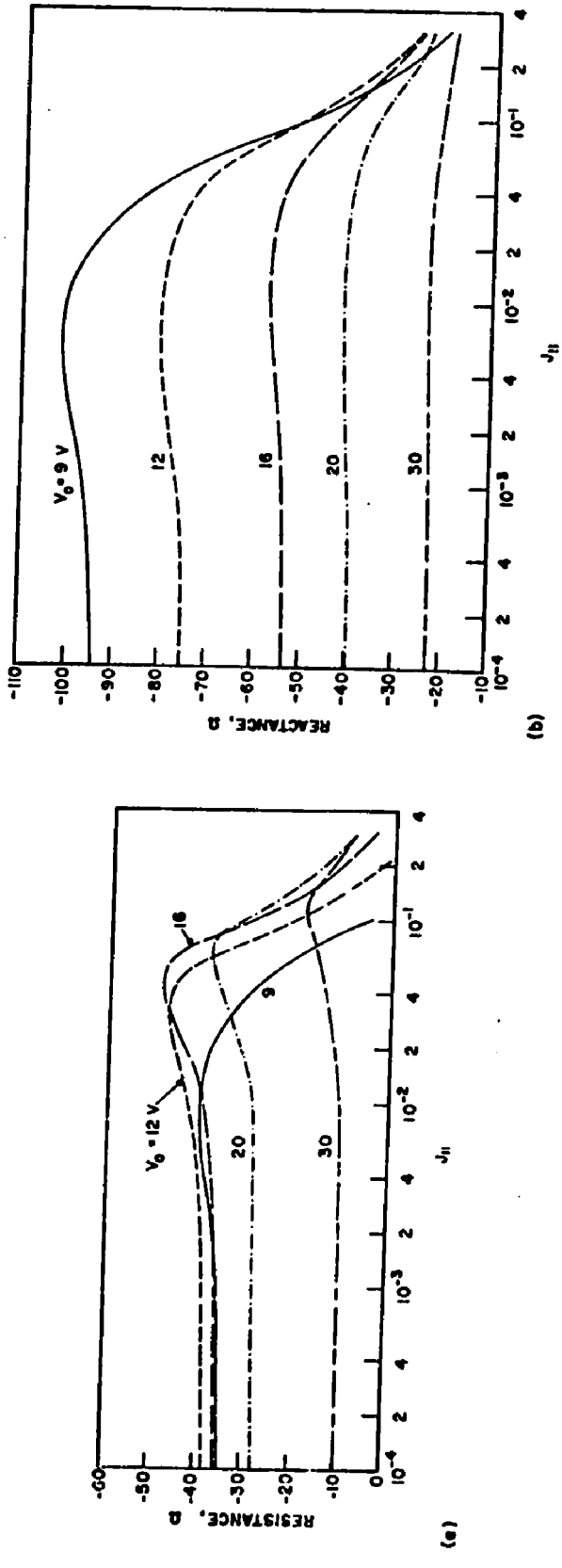


FIG. 5.17 RF EFFICIENCY VS. BIAS VOLTAGE FOR THE DIODE AND OPERATING CONDITIONS OF FIGS. 5.16a AND b.



Frequency = 10 GHz, $n_o = 5 \times 10^{14}/cm^3$, $A = .7 \times 10^{-4}$ cm^2, Lattice Temperature = 300°K

FIG. 5.18 RESISTANCE AND REACTANCE VS. J_{11} FOR A 10.1-μm DIODE AT DIFFERENT BIAS VOLTAGES.

large (Fig. 3.9). This is caused by an excess space-charge accumulation resulting from the nonlinearity of the device. If the device is biased at a current density slightly below $J_o = 1$, then in the small-signal case the electric field stays below threshold all along the length of the crystal as shown in Fig. 5.19 for $J_{11} = 0.0001$. The figure also shows the electric-field profiles for large values of J_{11}. For the same dc current density $J_o = 0.95$, the static field in the crystal increases as J_{11} is increased until enough of the crystal length is in the negative differential mobility region for the overall RF resistance to become negative. This occurs for $J_{11} = 0.17$ for a crystal length of 12.1 μm and for $J_{11} = 0.205$ for a crystal length of 11.1 μm. This is shown in Fig. 5.20 where the negative resistance, reactance and efficiency are plotted as functions of the normalized current density for the same material parameters, frequency and J_o as those of Fig. 5.19. The preceding argument shows that if the device current is kept constant, i.e., if the device is biased with a constant-current dc source below threshold, it may exhibit negative resistance at large signal levels but positive resistance at small signals.

The magnitude of negative resistance is greater for small values of J_{11} for the longer crystal (12.1 μm). This is because when J_{11} is small, the field near the anode is not high enough to be in the passive region and the longer crystal has a longer active region. At high values of J_{11}, however, the field near the anode is high and a passive anode region exists. The longer device then has a longer passive region and its negative resistance thus has a smaller magnitude (Fig. 5.20).

Figure 5.21 shows plots of bias voltage vs. normalized RF current density for a constant value of $J_o = 0.95$ for the two diodes considered

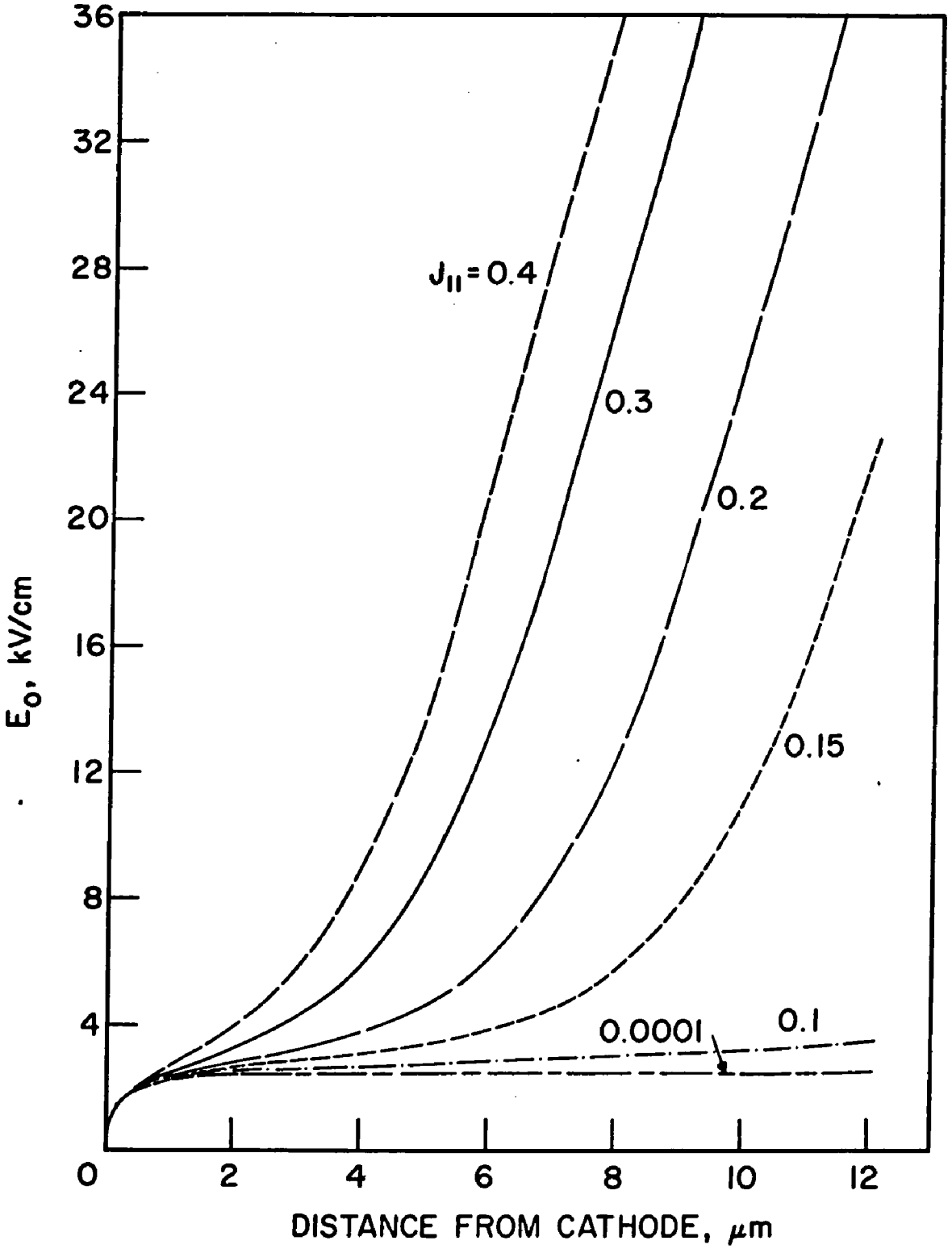
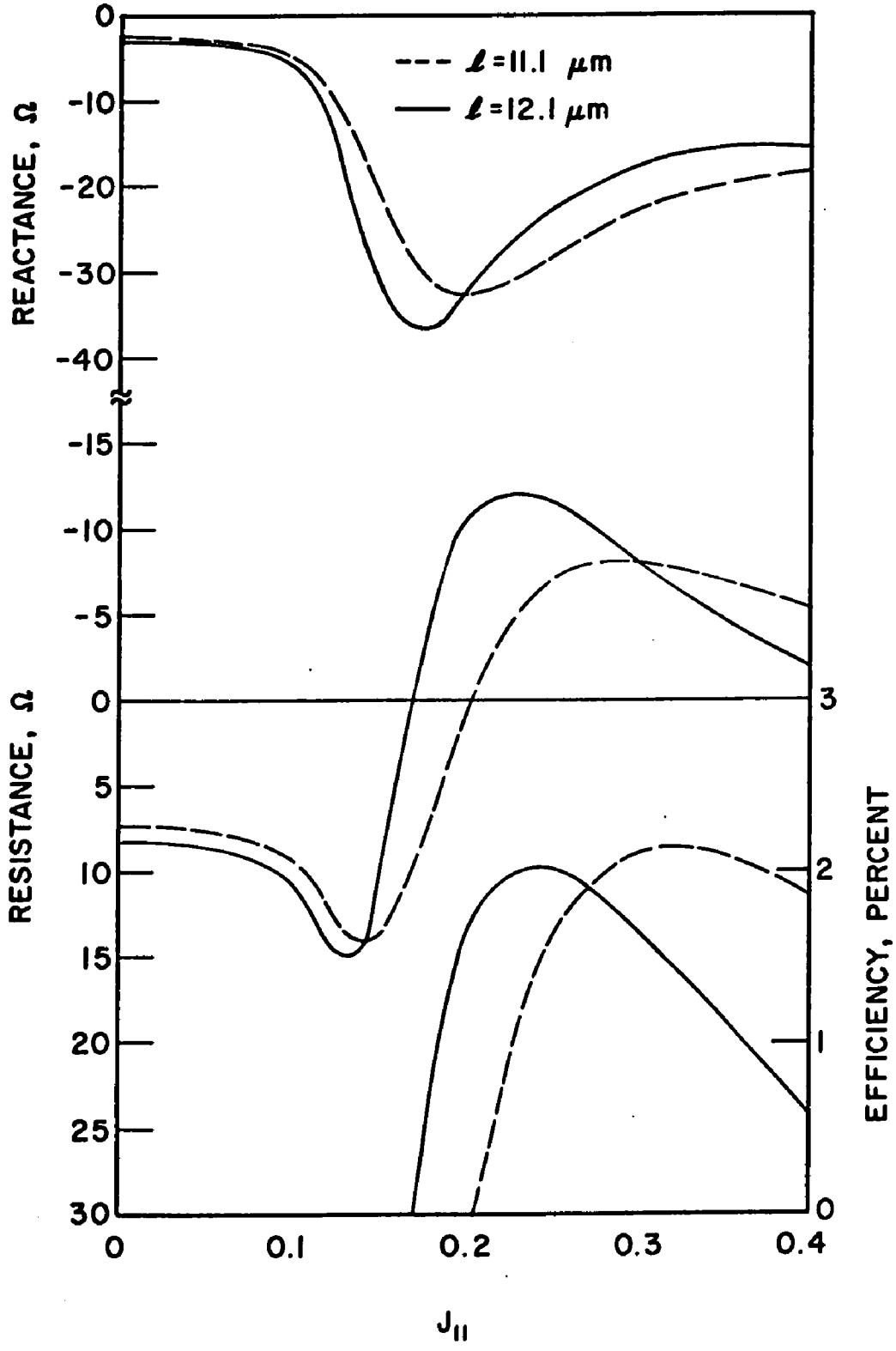


FIG. 5.19 STATIC ELECTRIC FIELD VS. DISTANCE FROM THE CATHODE FOR DIFFERENT VALUES OF J_{11} AND FOR J_o = 0.95.



$n_o = 5 \times 10^{14}/cm^3$, $A = 7 \times 10^{-4}$ cm^2, Lattice Temperature = 300°K,

Frequency = 10 GHz

FIG. 5.20 RF EFFICIENCY, RESISTANCE AND REACTANCE OF TWO DIODES OF DIFFERENT LENGTHS VS. RF CURRENT DENSITY.

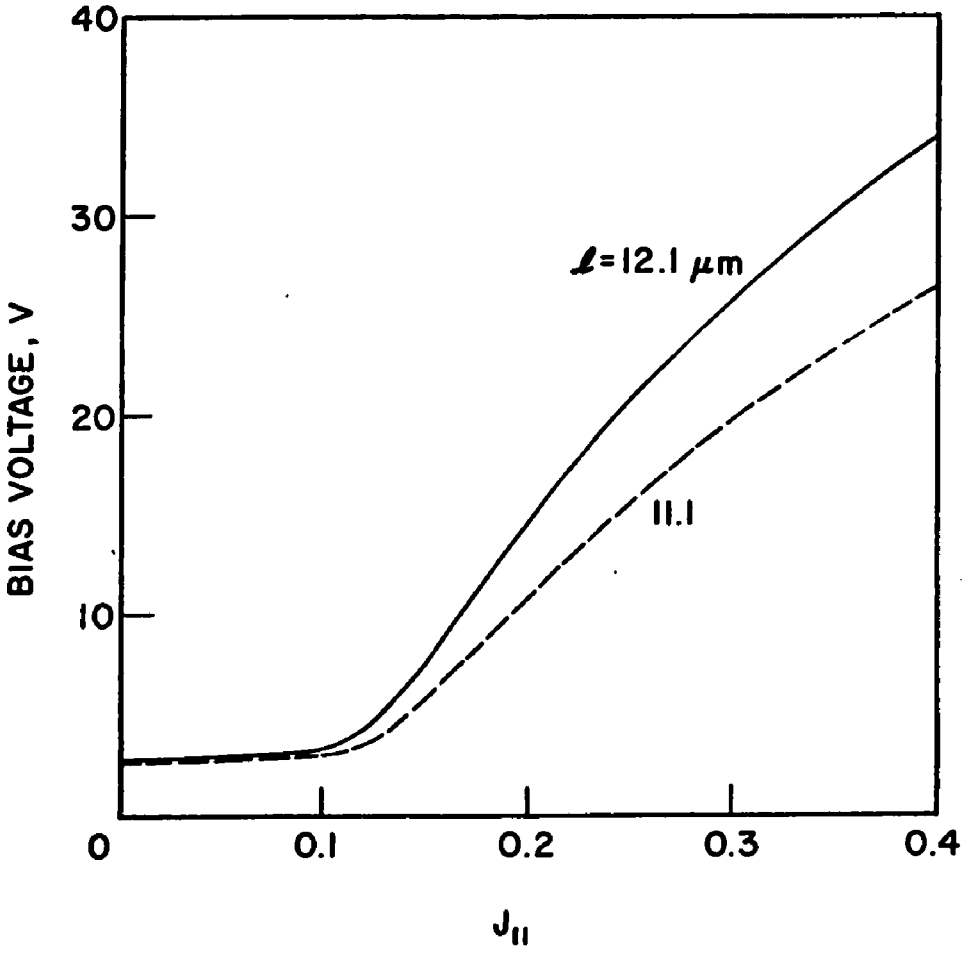


FIG. 5.21 BIAS VOLTAGE VS. J_{11} FOR THE DIODES AND OPERATING CONDITIONS OF FIG. 5.20.

in Fig. 5.20. There is no appreciable increase in the bias voltage until J_{11} increases beyond the value of $J_{11} = 0.1$. This is a restatement of the fact established earlier (Fig. 3.9) that the static-field distortion does not increase appreciably for small J_{11} as J_{11} is increased. It increases rapidly when J_{11} is large.

Figure 5.21 clearly illustrates that a device with a low $n_o \ell$ product may exhibit a dc current less than threshold value above threshold bias voltage. This is another way of saying that a "current drop" occurs due to large RF signal levels.

5.4 Summary

Plots of resistance and reactance of a stabilized TE device as a function of frequency show that bandwidths greater than an octave are achievable with these devices. The bandwidth is seen to decrease as the bias is increased. Because of the change in the length of the passive cathode region with bias, the negative-resistance frequency region shifts downward as the bias is increased. This shift in frequency is less marked if the passive cathode region is eliminated by the injection-limited cathode in which the cathode electric field is above the threshold value.

It is possible to get negative resistance over two octaves or more when a diode is operated at low bias voltages. However such performance is limited to relatively small signal levels.

When the static-field distortion is initially low, the magnitude of negative resistance and the dc to RF conversion efficiency increase as the bias is increased. The converse is true when the static-field distortion is initially high. The magnitude of negative resistance and

efficiency thus goes through a peak as the bias is varied. At very high biases the RF resistance becomes positive for a fixed frequency and device length. This indicates that higher bias voltages aid stabilization of the devices.

The minimum bias at which RF negative resistance appears depends on the magnitude of RF current density. The larger the RF current, the greater is the bias voltage at which this happens. For constant device parameters and frequency, the diode RF resistance becomes positive when the bias voltage is increased beyond a certain limit. This limit is higher at larger signal levels.

When the bias voltage is kept constant, the magnitude of the negative resistance goes through a peak as the RF signal level is increased from a small value. This peak occurs at a relatively small signal level when the bias is low and occurs at higher signal levels at large bias values. This causes a "gain expansion" as RF drive power is increased for a TE amplifier.

It is possible to obtain negative resistance at large signal levels even when the bias current is below the threshold value of $J_o = 1$. However, in these cases the bias voltage is well above threshold. For constant frequency and a bias current less than threshold value, the negative resistance appears at relatively smaller signal levels for longer crystals.

CHAPTER VI. TEMPERATURE EFFECTS IN STABILIZED TRANSFERRED-ELECTRON DEVICES

6.1 Introduction

The relationship between the average carrier velocity and the electric field in GaAs is influenced considerably by the lattice temperature. The relationship for three different temperatures was shown in Fig. 2.1. An increase in lattice temperature reduces both the low-field mobility and the negative differential mobility. This affects the static as well as the RF characteristics of TE devices. The changes in behavior of the TE devices when the lattice temperature is changed or when it varies along the length of the GaAs crystal are discussed in this chapter.

Section 6.2 treats the effect of lattice temperature variation as that of change in the peak-to-valley ratio (i.e., the ratio between the maximum average electron velocity to the velocity at high electric fields) of the velocity-field characteristic. Small-signal calculations are presented to show the effect of this ratio on device small-signal properties.

Variation in the peak-to-valley ratio, or the negative differential mobility affects the space-charge accumulation pattern in the crystal. This influences the static-field distortion and changes the current-voltage relationship of the device. In fact the nature of the relationship between current and voltage is characteristic of the peak-to-valley ratio. These effects are considered in Section 6.3.

The effect of lattice temperature on large-signal RF characteristics is discussed in Section 6.4. Calculations based on the present analysis are presented to show the changes in device resistance and reactance,

efficiency and large-signal saturation effects. The implication of these effects with regard to the circuit stabilization of the devices is considered.

In practice, lattice temperature gradients are likely to exist in these devices as a result of nonuniform electric field distribution and because heat sinking is usually done only at one end of the crystal. The effect of such gradients on the dc to RF conversion efficiency is discussed in Section 6.5. The possibility of increasing the efficiency through the control of temperature gradients is also considered.

Except where stated, diffusion effects are included in the results presented in this chapter. As already discussed in Chapter II, the diffusion coefficient is taken to be constant as a function of lattice temperature. Since most of the material in use presently is epitaxially grown with shallow donors, n_o is also taken to be constant as a function of lattice temperature.

6.2 Relationship Between Device Small-Signal Properties and the Shape of the v-E Curve

Perhaps the most significant change in the material properties as a result of lattice temperature variation occurs in the peak-to-valley ratio of the velocity-field characteristic. It is clear from Fig. 2.1 that the peak-to-valley ratio changes with temperature mainly because of the change in the peak velocity, since the change in velocity at high electric fields is relatively small. Thus in order to understand the effects of changes in the lattice temperature, small-signal impedance calculations were made using the different piecewise linear velocity-field characteristics of

Fig. 6.1. In the figure, the peak velocity is varied to obtain different peak-to-valley ratios from 1.5 to 5.0. The negative differential mobility changes accordingly and the corresponding values are shown. Diffusion effects are neglected for simplicity.

Computations were made for a crystal of ℓ = 10 μm, $n_o = 5 \times 10^{14}/cm^3$ and area = 7×10^{-4} cm^2 over a band of frequencies and the maximum negative resistance obtained (around 10 GHz) is plotted against the peak-to-valley ratio in Fig. 6.2 for a value of J_o equal to 1.1. Maximum value of negative resistance in the frequency band is chosen so that transit angle effects are unimportant for the following discussion. Although a direct decrease in the magnitude of negative resistance with a decrease in the peak-to-valley ratio might be expected, it did not always occur. Instead, the maximum negative resistance was not greatly affected by changes in the peak-to-valley ratio unless the ratio was small. The reason for this behavior can be explained with the aid of the lower part of Fig. 6.2 which shows the values of L_n, the length of the active region, and L_a, the length of the passive anode region. The passive cathode region is not considered since its length does not change appreciably. A large peak-to-valley ratio results in a large slowing down of charge carriers with a consequent large static-field distortion. This leads to a smaller length L_n of the active region and a longer passive region (L_a). A decrease in the peak-to-valley ratio increases the length of the active regions (L_n) and decreases the length of the passive region (L_a). This compensates for the reduced negative differential mobility until lower values of peak-to-valley ratio occur. Thus a significant increase in lattice temperature above room temperature may be necessary to reduce the magnitude of the negative resistance by means of a change in the v-E curve.

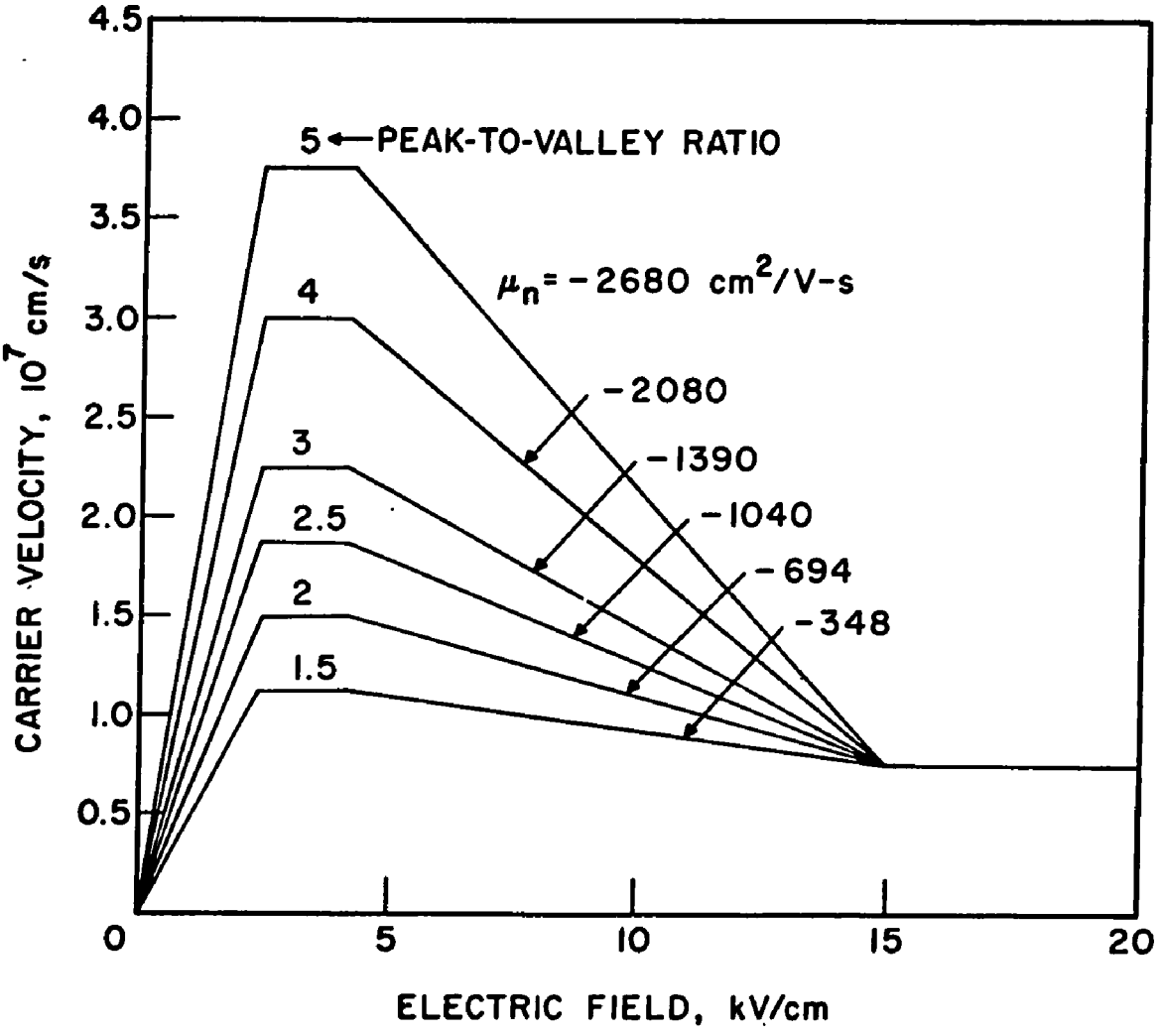


FIG. 6.1 VELOCITY-FIELD RELATIONSHIPS USED FOR SMALL-SIGNAL DIFFUSION-FREE STUDY.

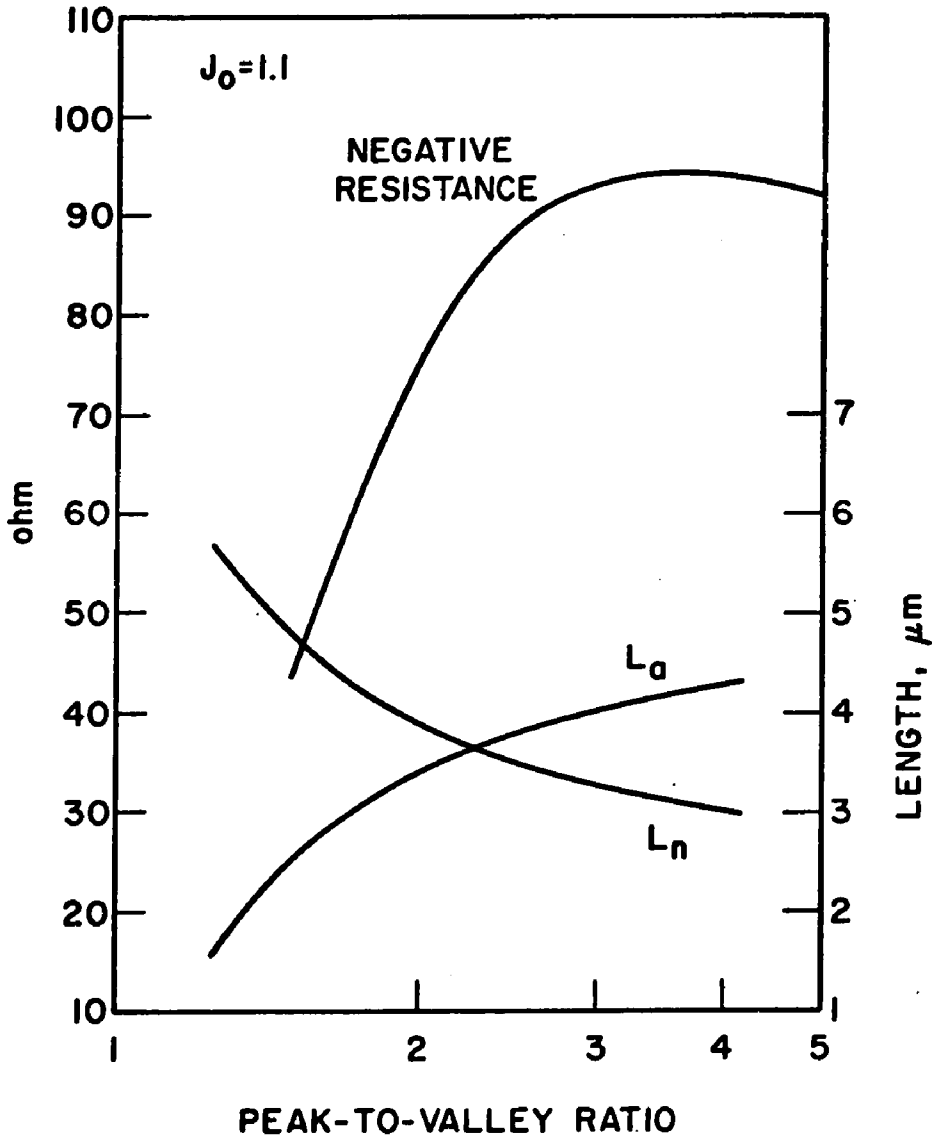


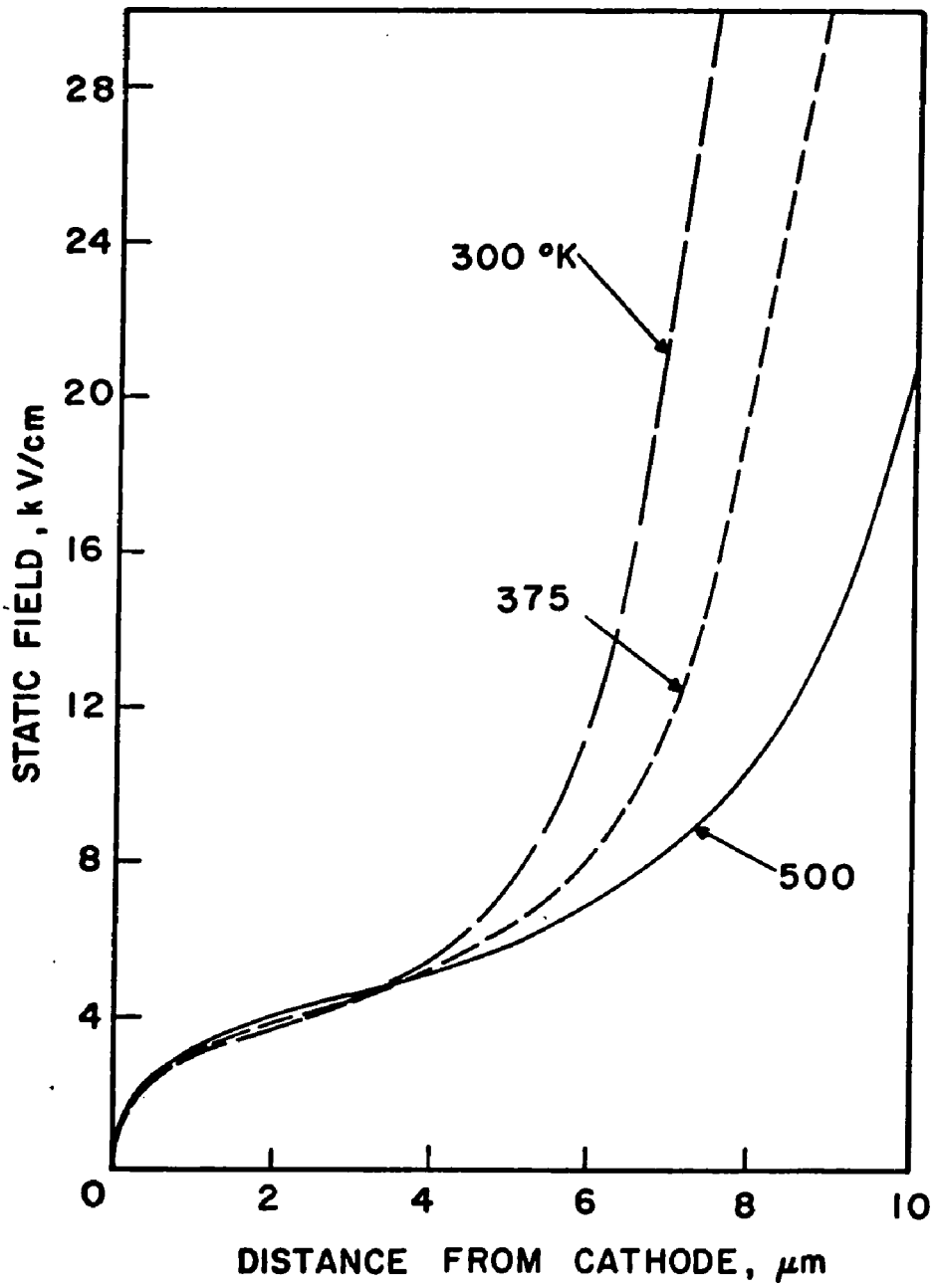
FIG. 6.2 DIFFUSION-FREE SMALL-SIGNAL CALCULATIONS OF MAXIMUM NEGATIVE RESISTANCE, AND LENGTHS OF ACTIVE (L_n) AND PASSIVE REGIONS (L_a) IN A DEVICE 10 μm LONG, WITH $n_o = 5 \times 10^{14}/cm^3$ AND AREA = 7×10^{-4} cm^2. VELOCITY-FIELD RELATIONSHIPS OF FIG. 6.1 WERE USED.

6.3 Effect of Change in Lattice Temperature on the Static Characteristics of TE Devices

It was stated in the last section that a high peak-to-valley ratio results in a greater static-field distortion. This is illustrated in Fig. 6.3 where static electric field is plotted vs. distance from the cathode for $n_o = 5 \times 10^{14}/cm^3$. These curves were calculated by applying the large-signal analysis including diffusion effects for the analytical forms of v-E characteristics shown in Fig. 2.1 for 300°K, 375°K and 500°K. In each case the current is 10 percent above the threshold value. At lower temperatures the peak-to-valley ratio is relatively high and the static-field distortion is accordingly high.

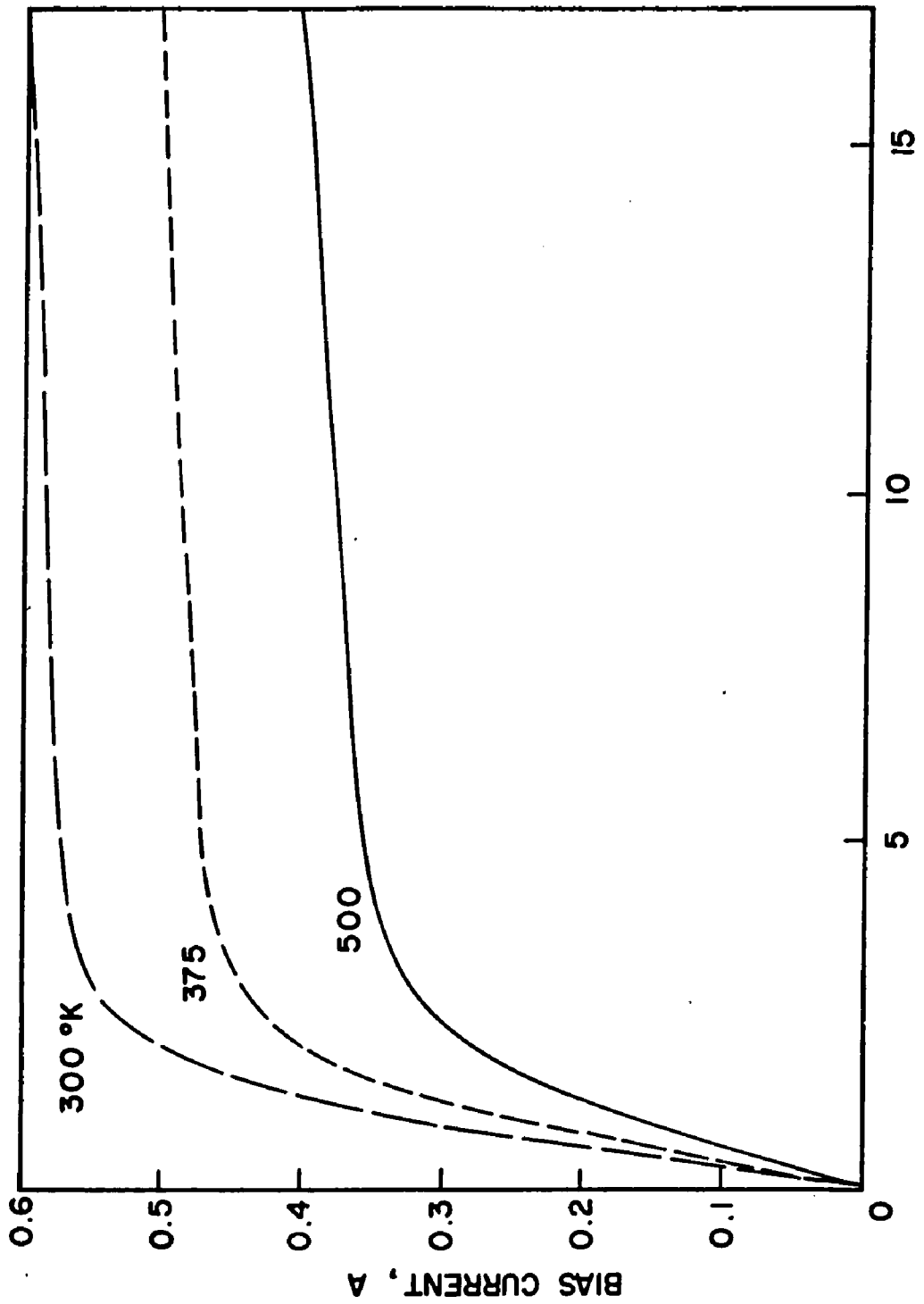
It should be noted in Fig. 6.3 that the magnitude of the normalizing current is different in each of the three cases depending upon the peak velocity. But the fact remains that even if the peak velocity were kept constant and the velocity at high fields was varied, the static-field distortion would be higher for higher peak-to-valley ratios.

It was shown in Section 3.3 that when a diode is biased with a constant dc voltage supply, a buildup of negative resistance oscillations or injection of a relatively large RF signal leads to a drop in the average bias current. In addition to this current drop, Perlman et al.[46] have observed that in CW devices additional current drop occurs at high bias voltages due to heating of the crystal lattice. Such change in device current with lattice temperature can be seen in Fig. 6.4 where the device dc current is plotted as a function of bias voltage for small ac signals and a crystal length of 10.1 μm, $n_o = 5 \times 10^{14}/cm^3$ and area = 3.5×10^{-4} cm^2. The three curves are for lattice temperatures of 300°K, 375°K and 500°K as



$n_o = 5 \times 10^{14}/cm^3$, Frequency = 10 GHz, $J_o = 1.1$, $J_{ii} = 0.001$

FIG. 6.3 STATIC ELECTRIC FIELD VS. DISTANCE FROM THE CATHODE AT THREE LATTICE TEMPERATURES.



ℓ = 10.1 μm, $n_o = 5 \times 10^{14}/cm^3$, Area = 3.5×10^{-4} cm^2, Frequency = 10 GHz, $J_{11} = 0.0001$

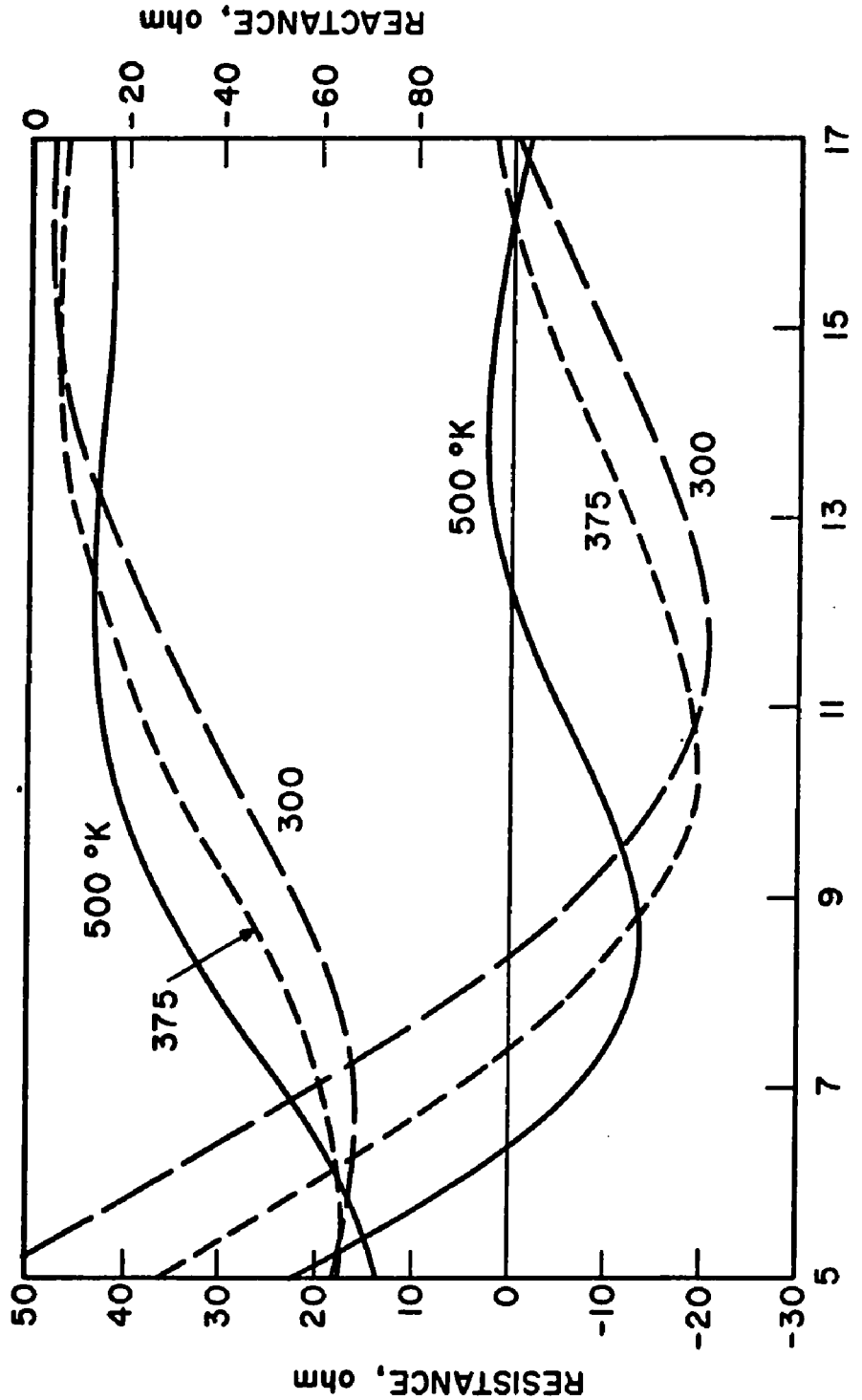
FIG. 6.4 BIAS CURRENT VS. BIAS VOLTAGE FOR A DIODE AT DIFFERENT LATTICE TEMPERATURES.

indicated. At lower temperatures the average carrier velocity is high and the device current is relatively high for a constant bias voltage. The current decreases at higher temperatures. Such curves can be used to estimate the thermal resistance of a device. If the difference in bias current when a device is operated pulsed or CW is known, the increase in lattice temperature can be estimated from curves of the kind shown in the figure. The thermal resistance can then be calculated by dividing the increase in temperature by the dc power dissipated in the CW case.

It may be pointed out that the slope of the current vs. voltage relationship is quite small above the threshold voltage. This is because a slight increase in current causes a great increase in the static-field distortion leading to a large increase in voltage drop across the crystal. If the peak-to-valley ratio or the average negative differential mobility were small, the increase in static-field distortion would be small and the slope of the current vs. voltage curve would be correspondingly large. If, on the other hand, the peak-to-valley ratio were substantially greater than the values in Fig. 2.1, the slope would be even smaller. Thus, the slope of the current voltage relationship is characteristic of the peak-to-valley ratio for the material.

6.4 Effect of Lattice Temperature on the Large-Signal Properties of Stabilized TE Devices

The large-signal resistance and reactance of a diode are shown as functions of frequency in Fig. 6.5 at three different temperatures. The device and operating parameters are ℓ = 10.1 μm, area = 7 x 10^{-4} cm^2 and J_{11} = 0.15. The bias is approximately 16 V. J_o was adjusted for each



$n_o = 5 \times 10^{14}/cm^3$, Bias Voltage = 16 V, Length = 10.1 μm, $A = 7 \times 10^{-4}$ cm^2, $J_{11} = 0.15$

FIG. 6.5 IMPEDANCE VS. FREQUENCY AT DIFFERENT LATTICE TEMPERATURES WITH DIFFUSION EFFECTS INCLUDED.

calculation to obtain this voltage. The increase in temperature is seen to reduce the magnitude of maximum negative resistance and also the frequency at which it occurs. The behavior of the maximum negative resistance magnitude is more or less similar to that shown in Fig. 6.2. The downward shift in the frequency band where negative resistance occurs is due to an overall lowering of carrier velocity at higher temperatures.

A comparison of small- and large-signal resistance and reactance of the crystal of Fig. 6.5 is shown in Figs. 6.6, 6.7 and 6.8 for lattice temperatures of 300°K, 375°K and 500°K, respectively. The bias voltage is 16 V in each case. Two important features may be discerned: (1) The frequency of maximum negative resistance increases as the signal level is increased. This effect is not noticeable at 500°K for $J_{11} = 0.15$. (2) The magnitude of negative resistance decreases with increase in J_{11} at relatively low temperatures, the decrease being more marked at 300°K than at 375°K. The opposite is true at 500°K. These two effects are explained as follows:

1. This can be understood by looking at the static-field profile inside the crystal at small and large signal levels as shown in Figs. 6.9 and 6.10 for 300°K and 500°K, respectively. The signal frequency is chosen to be the one at which negative resistance is near maximum in each case (Figs. 6.6 and 6.8, respectively). These figures are different from Fig. 3.9 in that the voltage drop across the crystal is kept constant whereas in the latter the static current was kept constant. Therefore, the average electric field must be the same at both the small as well as the large signal levels. The change in static-field profile with

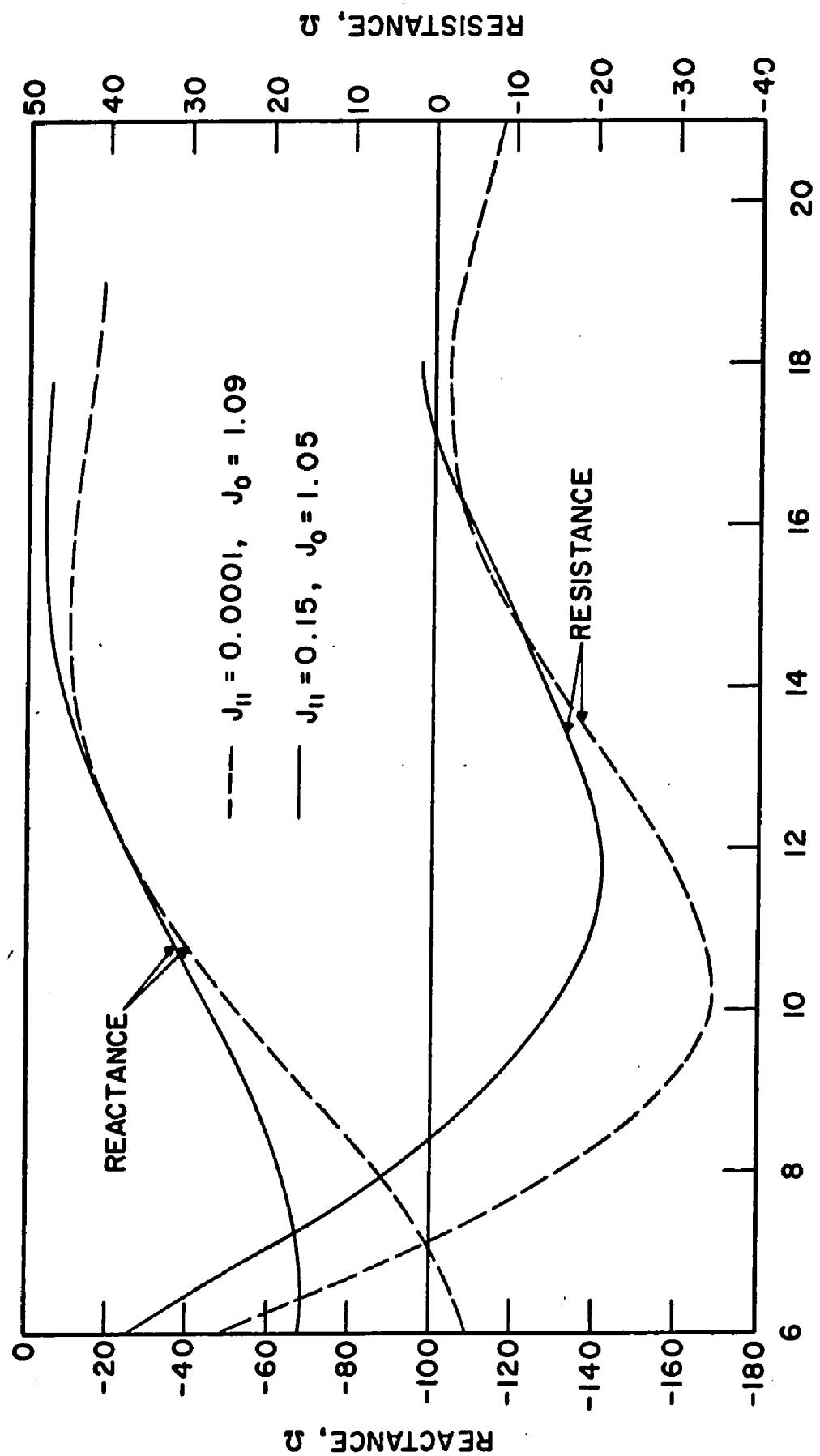
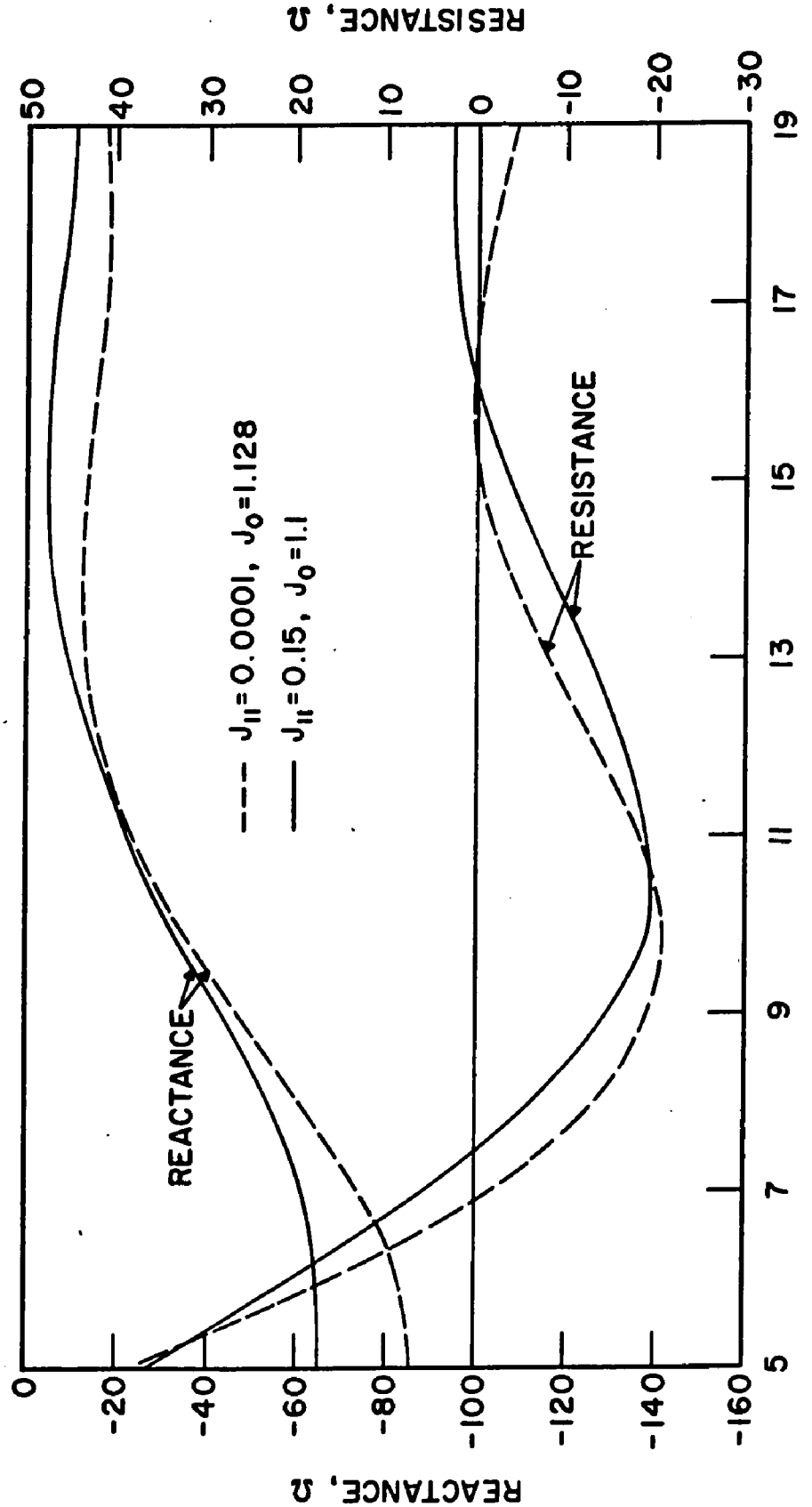


FIG. 6.6 SMALL- AND LARGE-SIGNAL RESISTANCE AND REACTANCE OF A DIODE VS. FREQUENCY WITH LATTICE TEMPERATURE = 300 °K.

l = 10.1 μm, $n_o = 5 \times 10^{14}/cm^3$, Area = 7×10^{-4} cm^2, Bias Voltage = 16 V



ℓ = 10.1 μm, n_o = 5 x 10^{14}/cm^3, Area = 7 x 10^{-4} cm^2, Bias Voltage = 16 V

TEMPERATURE = 375°K.

FIG. 6.7 SMALL- AND LARGE-SIGNAL RESISTANCE AND REACTANCE OF A DIODE VS. FREQUENCY WITH LATTICE

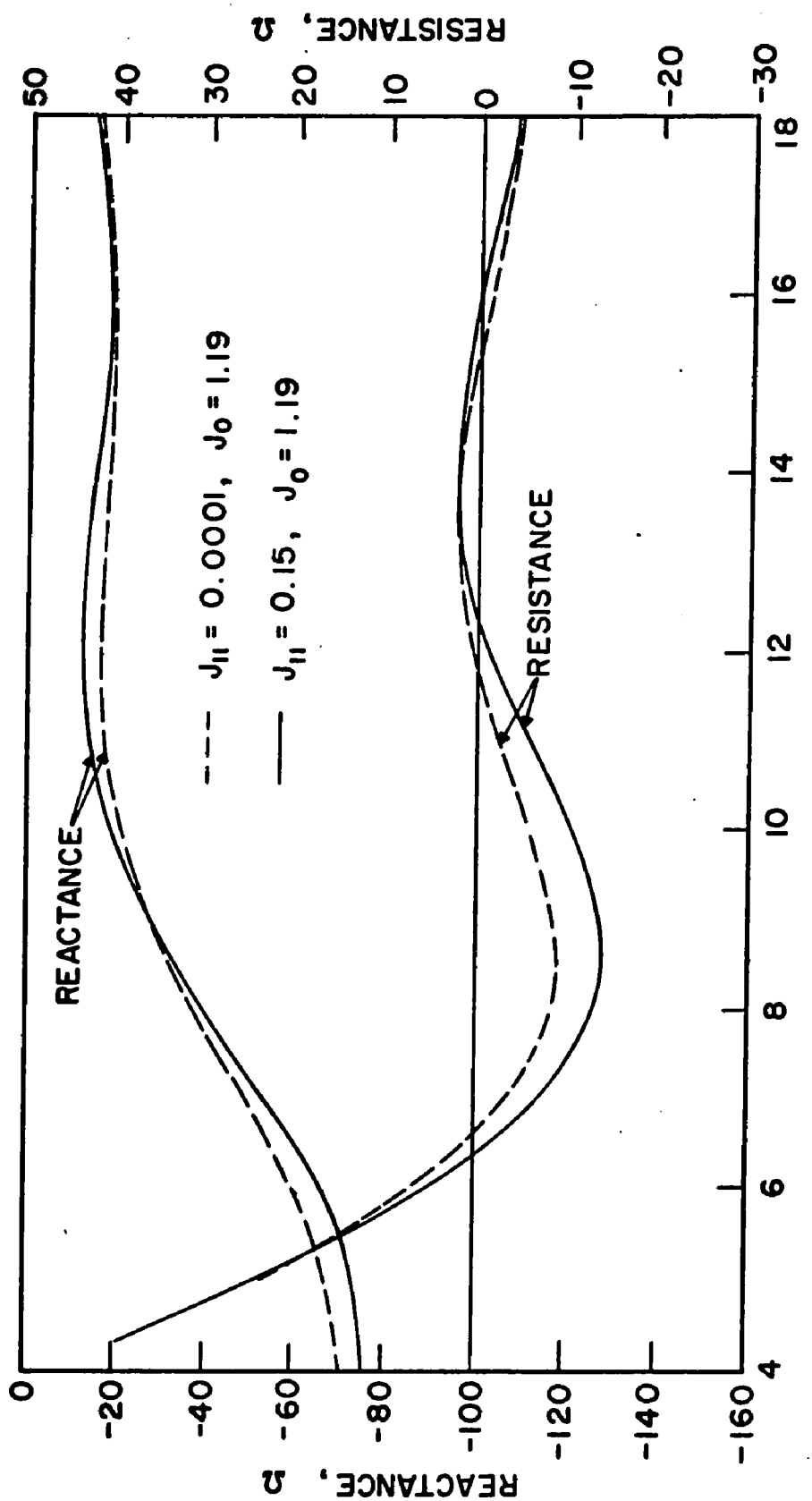


FIG. 6.8 SMALL- AND LARGE-SIGNAL RESISTANCE AND REACTANCE OF A DIODE VS. FREQUENCY WITH LATTICE TEMPERATURE = 500°K.

l = 10.1 μm, n_o = 5 x 10^{14}/cm^3, Area = 7 x 10^{-4} cm^2, Bias Voltage = 16 V

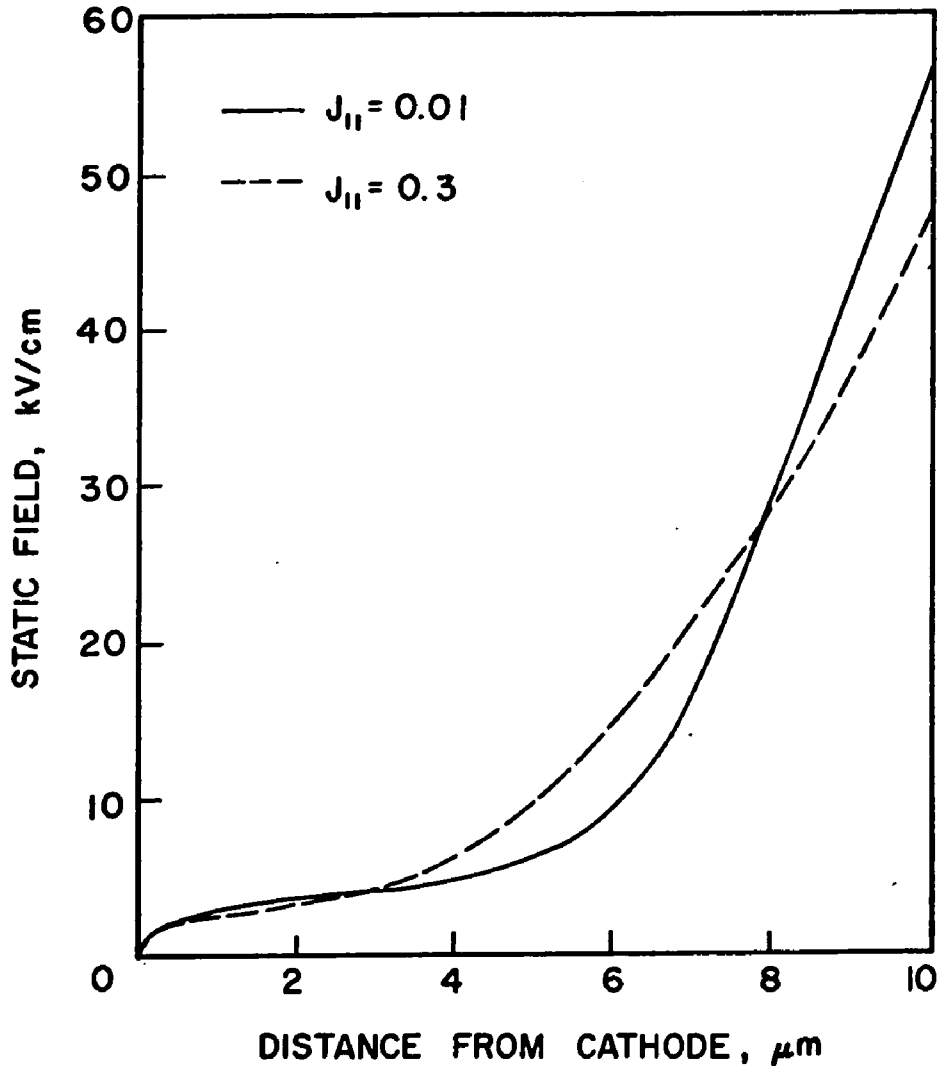


FIG. 6.9 STATIC ELECTRIC FIELD VS. DISTANCE AT SMALL AND LARGE RF SIGNALS IN THE CRYSTAL OF FIGS. 6.5 THROUGH 6.8 WITH LATTICE TEMPERATURE = 300°K, SIGNAL FREQUENCY = 11 GHz AND BIAS VOLTAGE = 16 V.

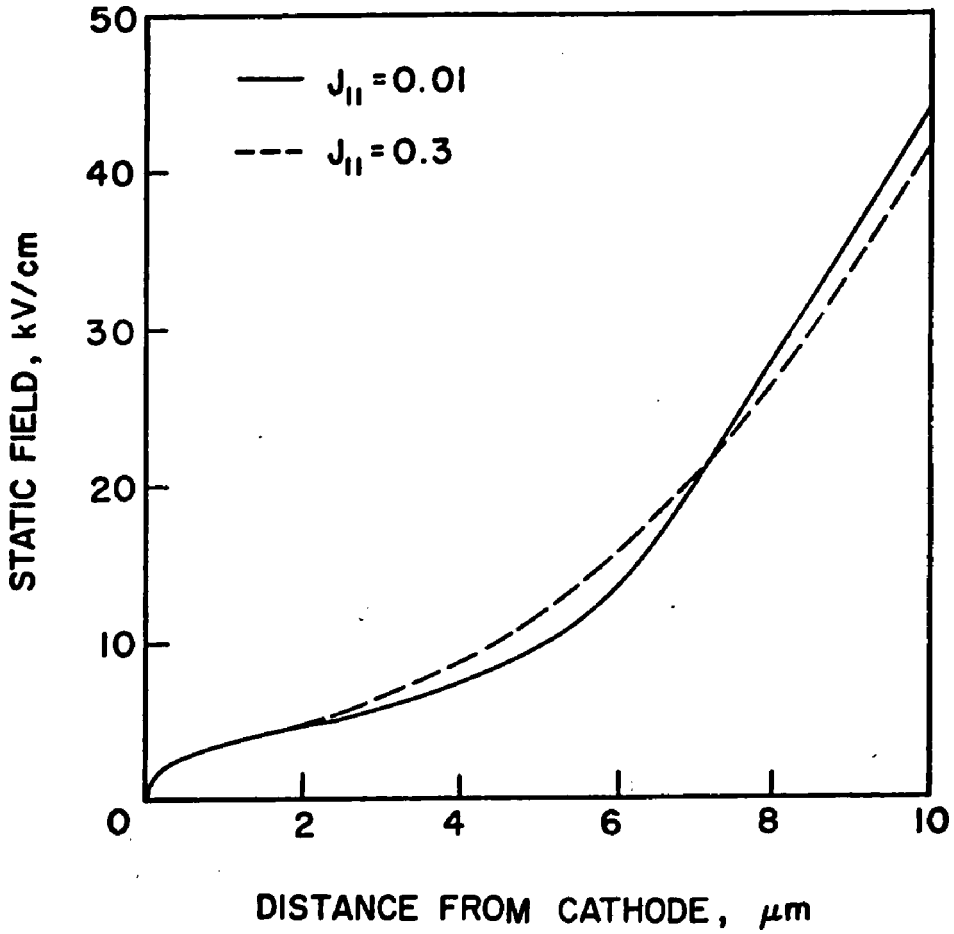


FIG. 6.10 STATIC ELECTRIC FIELD VS. DISTANCE AT SMALL AND LARGE RF SIGNALS IN THE CRYSTAL OF FIGS. 6.5 THROUGH 6.8 WITH LATTICE TEMPERATURE = 500°K, SIGNAL FREQUENCY = 9 GHz AND BIAS VOLTAGE = 16 V.

increase in signal level is such as to shorten the active region ($E_{th} < E_o < \sim 15$ kV/cm) in the crystal at the higher value of J_{11}. Thus, the upward shift in the negative resistance frequencies can be explained. At 500°K the change in the length of the active region is appreciably smaller and therefore the frequency band of negative resistance stays about the same.

2. It was shown in Figs. 3.8 and 5.18a that the magnitude of negative resistance at first increases and then decreases with J_{11}. Figure 6.11a shows this for three values of lattice temperature and for the device of Figs. 6.5 through 6.10. The bias is again kept constant at 16 V by adjusting J_o at each point on the curves. The maximum of the negative resistance occurs at larger values of J_{11} for higher lattice temperatures. This explains the above-mentioned observation. Notice that these calculations have been made at frequencies where the negative resistance is nearly a maximum in each case (see Figs. 6.6 through 6.9).

The reactance values corresponding to the results of Fig. 6.11a are shown in Fig. 6.11b. Notice that the device "Q" is lower at relatively low temperatures. This, combined with the results of Fig. 6.5, indicates that the bandwidth obtainable in these devices is likely to decrease at higher temperatures.

Dc to RF conversion efficiency values corresponding to the data of Figs. 6.11a and 6.11b are shown in Fig. 6.12. The efficiency is seen to be lower at higher lattice temperatures.

The resistance and reactance values for a case similar to that of Figs. 5.16a and 5.16b are shown in Fig. 6.13. The difference is that in Fig. 6.13 the lattice temperature is higher (375°K). The peak of the

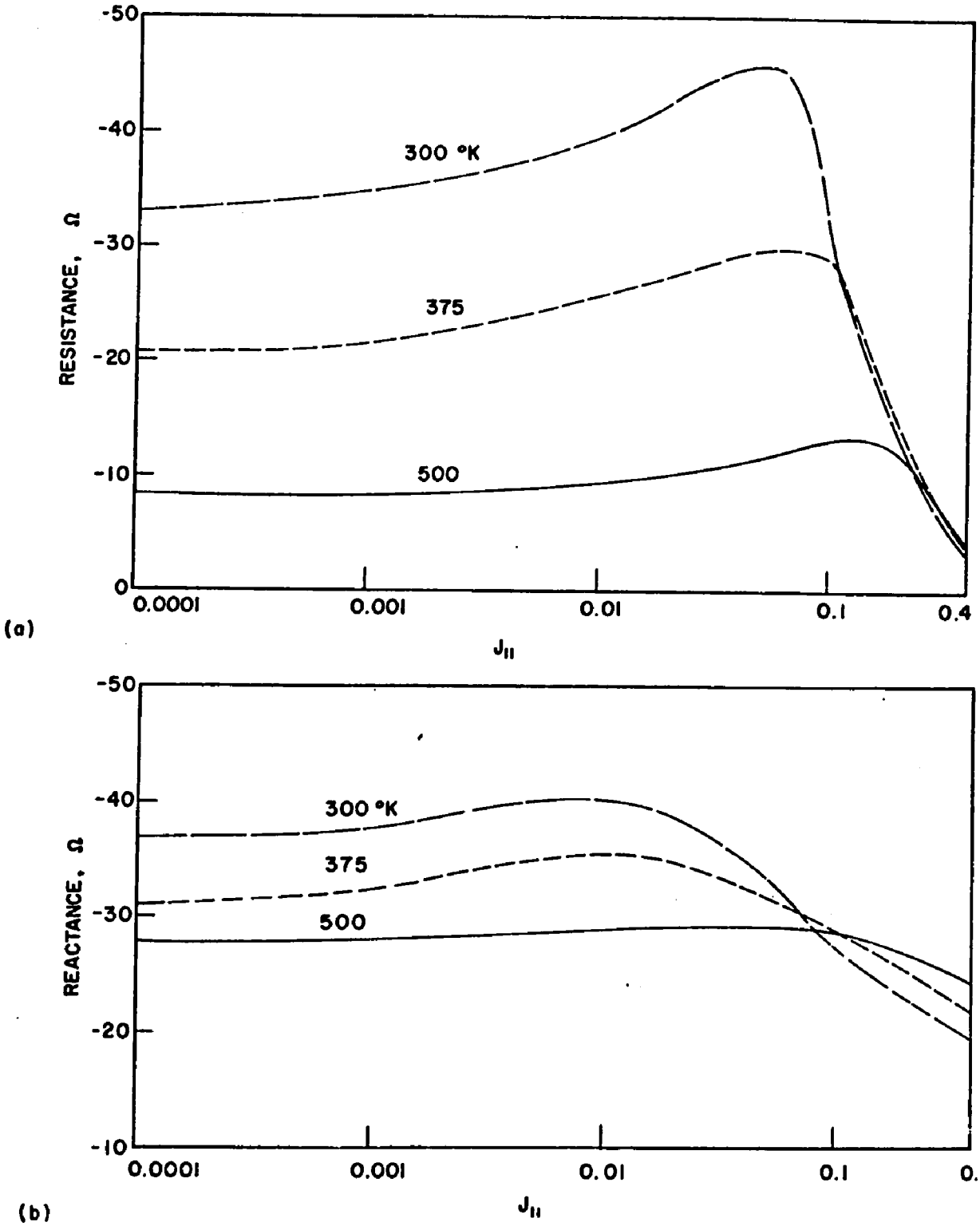


FIG. 6.11 RF RESISTANCE AND REACTANCE VS. J_{11} AT THREE DIFFERENT LATTICE TEMPERATURES FOR THE DIODE OF FIGS. 6.5 THROUGH 6.10. THE BIAS VOLTAGE IS 16 V, AND THE SIGNAL FREQUENCY IS 11 GHz AT 300°K, 10 GHz AT 375°K AND 9 GHz AT 500°K.

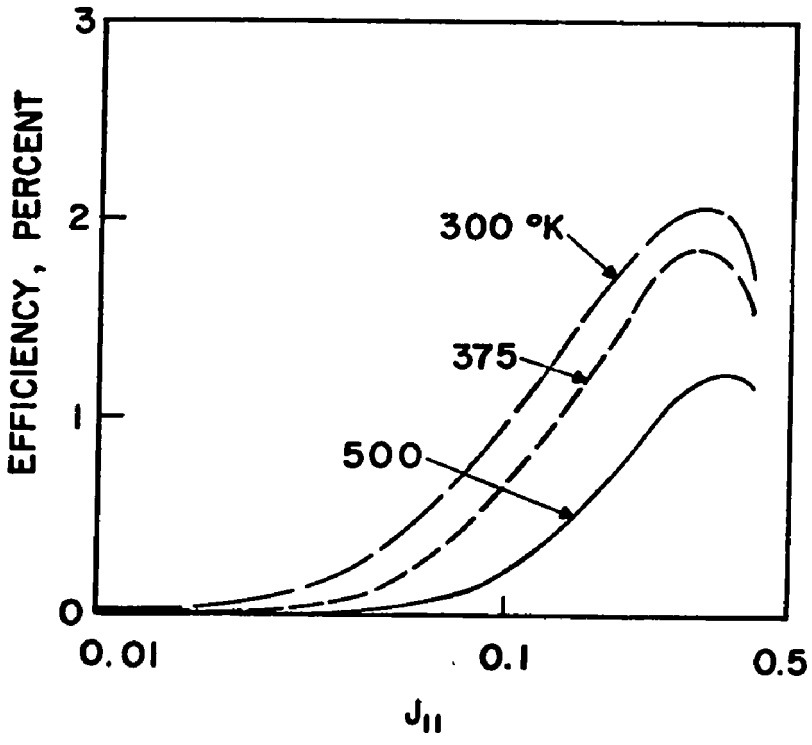


FIG. 6.12 Dc TO RF CONVERSION EFFICIENCY VS. J_{11} CORRESPONDING TO THE DATA OF FIG. 6.11a.

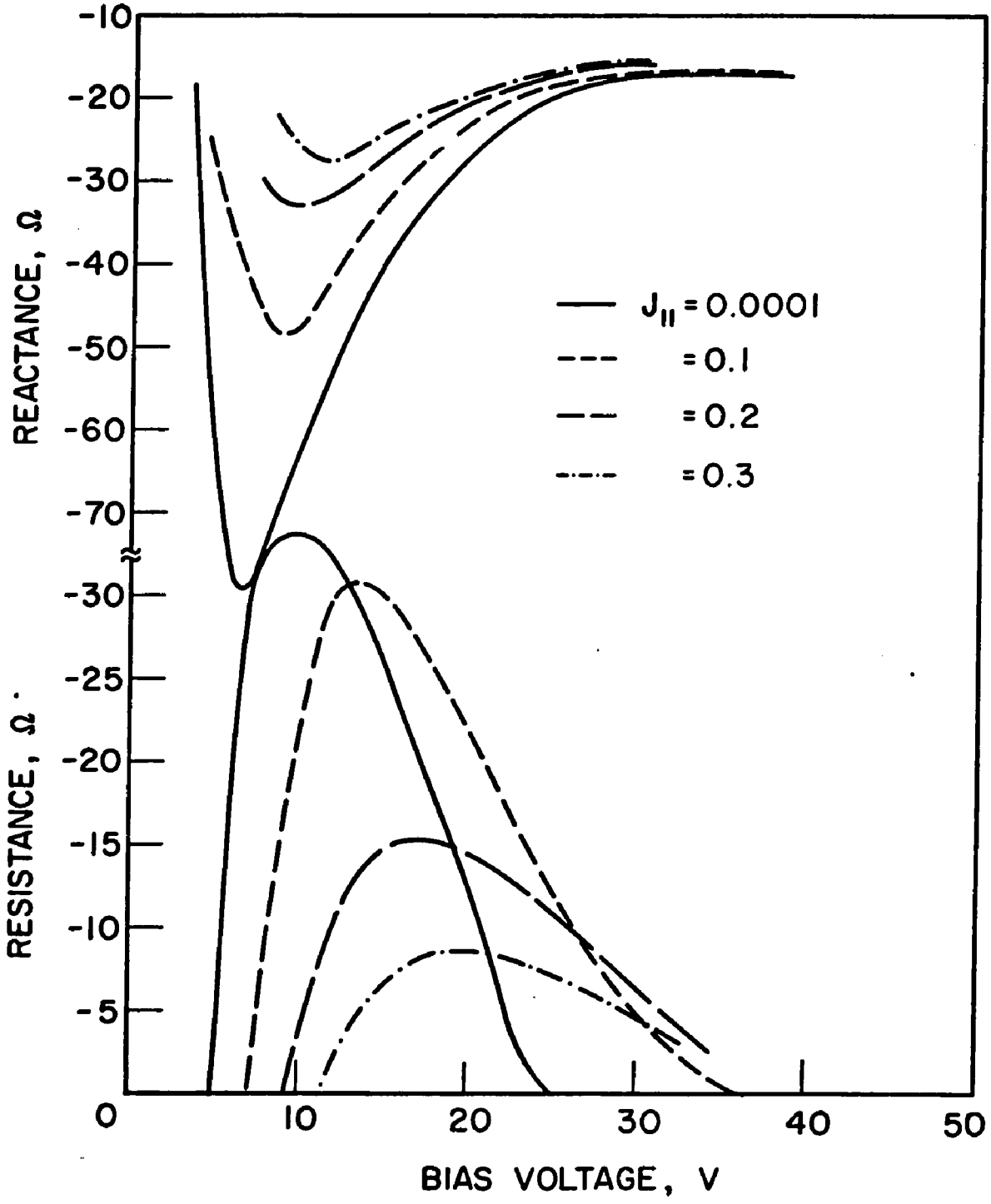


FIG. 6.13 RF RESISTANCE AND REACTANCE OF THE DIODE OF FIGS. 6.5 THROUGH 6.12 VS. BIAS VOLTAGE WITH LATTICE TEMPERATURE = 375°K.

negative resistance occurs at a lower bias voltage when the temperature is relatively high. This behavior, along with the overall reduction in negative resistance magnitudes at higher temperatures, aids circuit stabilization of these devices when they are operated CW at extremely high bias values.

The values of dc to RF conversion efficiency corresponding to the data of Fig. 6.13 are shown in Fig. 6.14 for different J_{11}. When compared with the results at 300°K (Fig. 5.17) these values are lower; a result similar to that of Fig. 6.12.

6.5 Variation of Lattice Temperature Along the Length of the GaAs Crystal

An increase in static-field distortion causes an increase in dc power dissipation in the crystal. This tends to reduce the dc to RF conversion efficiency of stabilized GaAs devices. The static-field distortion occurs in GaAs because the average carrier velocity is smaller at high electric fields and since the electric field increases monotonically from the cathode to the anode, the charge carriers have a small average velocity near the anode compared to the point where the electric field is near threshold. This difference in velocity causes charge accumulation to occur near the anode in order to satisfy the condition of continuity of current. If the region of the crystal near the anode were cooled to a lower temperature in comparison to the region near the cathode, the velocity of the charge carriers near the anode would be increased and this would lead to a reduced space-charge accumulation and consequently a smaller static-field distortion. The same dc result can be obtained by heating the whole crystal thereby reducing the peak-to-valley

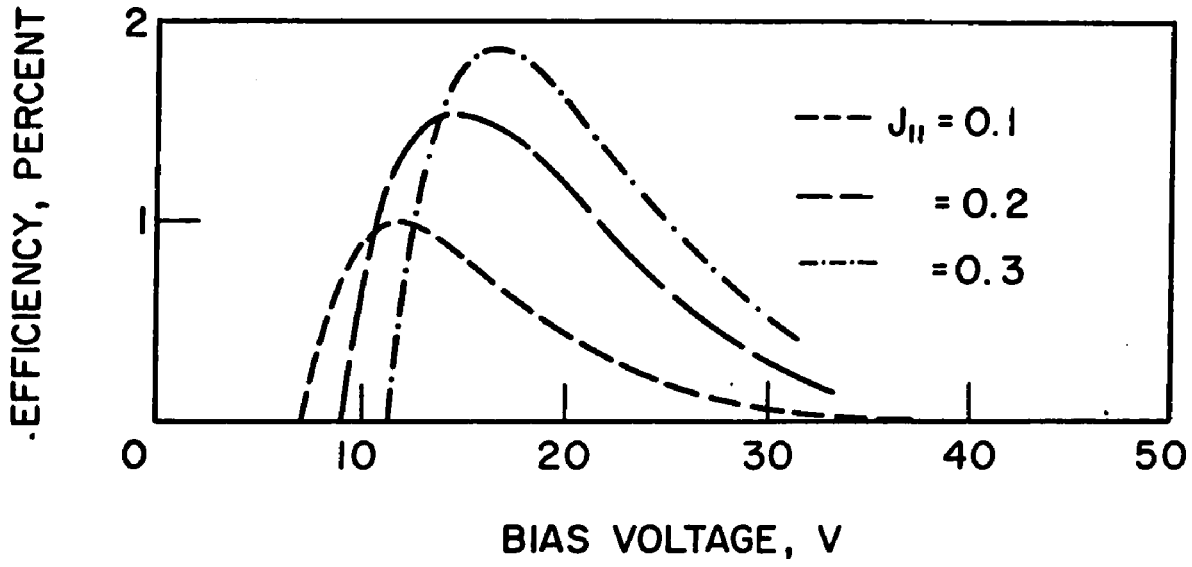


FIG. 6.14 Dc TO RF CONVERSION EFFICIENCY VS. BIAS VOLTAGE CORRESPONDING TO THE DATA OF FIG. 6.13.

ratio. The situation is not the same, however, when RF behavior is considered. In the dc case the field varies only in space, whereas when RF is considered there is also a fluctuation of electric field with respect to time. Thus it is likely that different effects are obtained when there are lattice temperature gradients with temperature decreasing away from the cathode rather than when the whole crystal lattice is heated.

A study of the effects of gradients in lattice temperature can be made by assuming the parameters a_1, a_2 and E_n of the velocity-field characteristic to be dependent on x, the distance from the cathode. For simplicity, a linear dependence for these constants with respect to the lattice temperature was assumed. If the temperature varies linearly with distance from the cathode then a_1, a_2 and E_n will also vary in the same fashion. Thus, if these constants corresponding to the lattice temperature T_1 at the cathode are a_{11}, a_{21} and E_{n1}, and those for temperature T_2 at the anode are a_{12}, a_{22} and E_{n2}, then for any distance x from the cathode the velocity-field characteristic will be determined by the following parameters:

$$a_1 = a_{11} + \frac{a_{12} - a_{11}}{\ell} x \ ,$$

$$a_2 = a_{21} + \frac{a_{22} - a_{21}}{\ell} x \ ,$$

$$E_n = E_{n1} + \frac{E_{n2} - E_{n1}}{\ell} x \ . \qquad (6.1)$$

Notice that the electric field is normalized with respect to E_n and the latter appears inside the differential sign in Eqs. 2.31, 2.32 and 2.33.

Since the value of E_n varies only slightly with respect to temperature, it was taken as a constant for the purpose of differentiation.

Figure 6.15 shows the best efficiency obtained for temperature variation from 300°K to 375°K for a distance of 10 μm starting from the cathode. Also shown is the crystal length at which the best efficiency occurs. The case for uniform lattice temperature is included for comparison. All the curves are for a normalized RF current density of $J_{11} = 0.3$. For all three cases of Fig. 6.15, J_{11} was normalized with respect to J_{th} at 300°K. Thus the absolute value of RF current density is the same in all three cases. It is seen from the figure that the efficiency for the case where lattice temperature decreases from the cathode to the anode is higher than the efficiency for uniform lattice temperature. On the other hand, for the case where the anode is at a higher temperature than the cathode, the efficiency is lower.

In order to optimize the efficiency for the cases of Fig. 6.15, efficiency was calculated for different values of J_{11}. The values of the dc current density at which the maxima occur in Fig. 6.15 were chosen for the calculations. The results are shown in Fig. 6.16 and again it is found that the efficiency can be improved if the anode is kept at a lower temperature than the cathode.

Figure 6.17 shows the voltage drop from the cathode to a point 11.1 μm away from the cathode for the two directions of lattice temperature gradient. While the RF current density magnitude is the same in both cases, the dc current density (abscissa) is normalized with respect to J_{th} (Eq. 3.1) corresponding to the respective cathode temperature. The

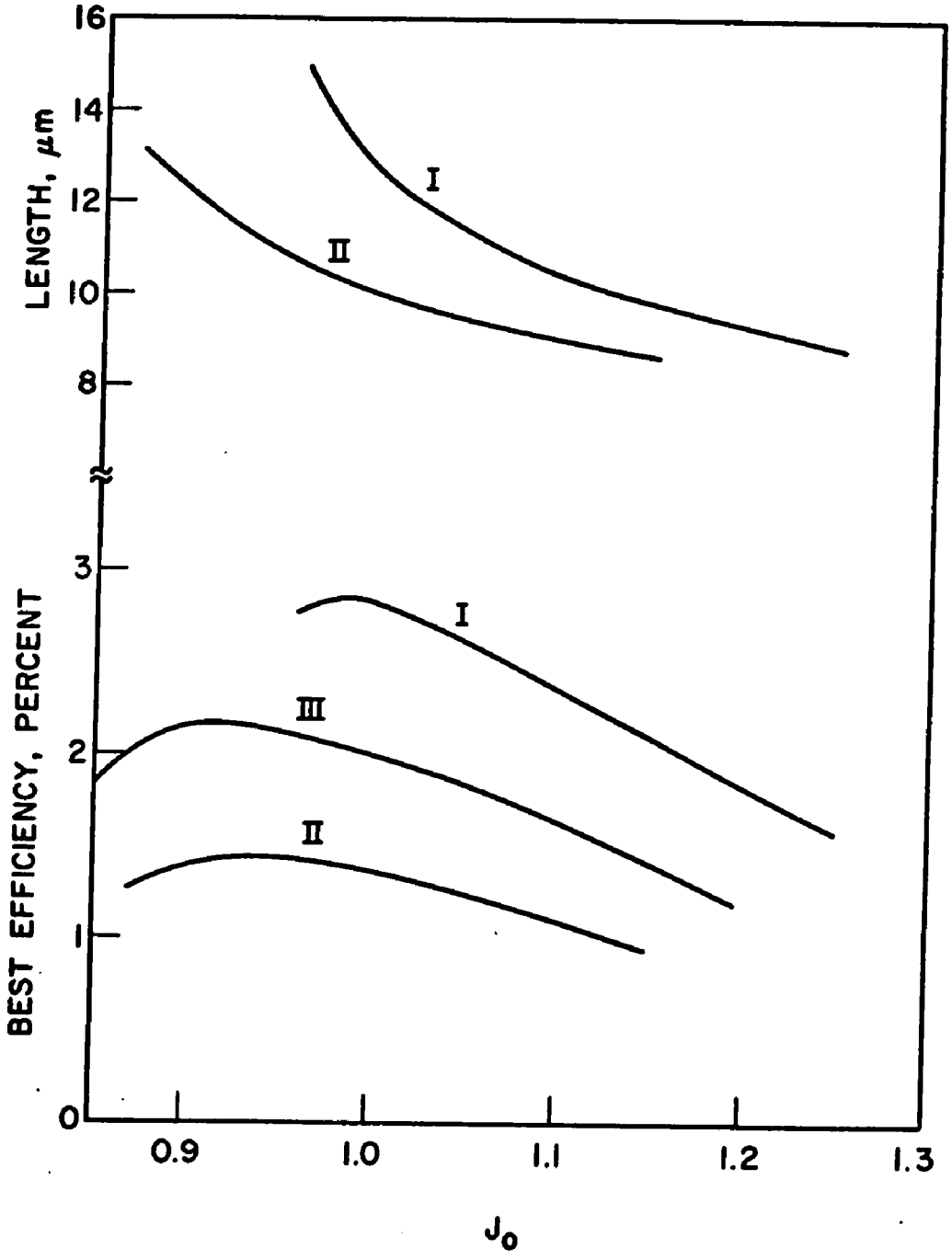


FIG. 6.15 BEST EFFICIENCY AND THE CRYSTAL LENGTH AT WHICH IT OCCURS VS. NORMALIZED dc CURRENT DENSITY. [n_o = 5 x $10^{14}/cm^3$, FREQUENCY = 10 GHz AND J_{11} = 0.3 FOR T_1 = 375°K, T_2 = 300°K (CURVES I); T_1 = 300°K, T_2 = 375°K (CURVES II); UNIFORM LATTICE TEMPERATURE = 300°K (CURVE III)]

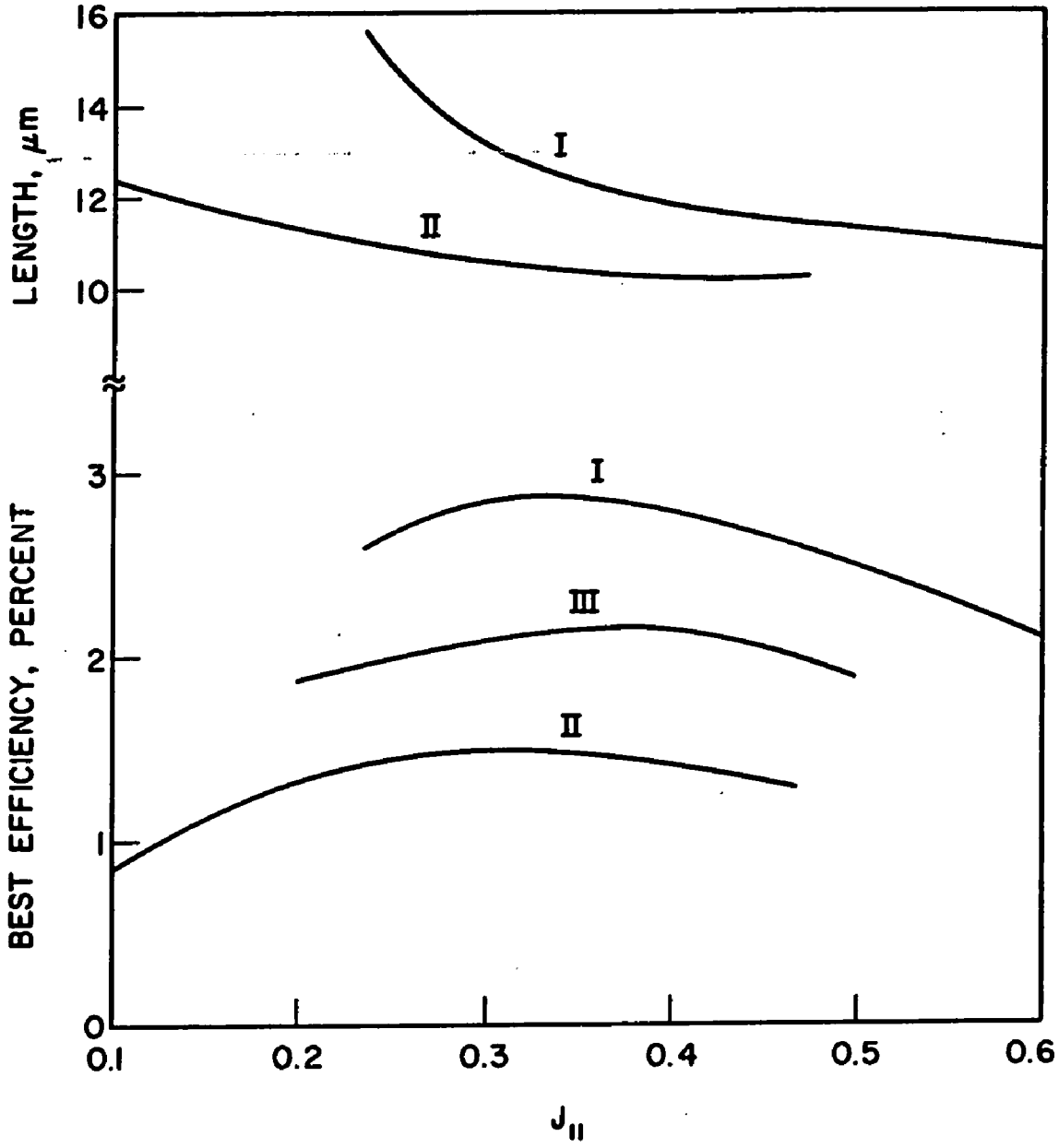


FIG. 6.16 BEST EFFICIENCY AND THE CRYSTAL LENGTH AT WHICH IT OCCURS VS. NORMALIZED RF CURRENT DENSITY. [$n_o = 5 \times 10^{14}/cm^3$, FREQUENCY = 10 GHz FOR $T_1 = 375°K$, $T_2 = 300°K$, $J_o = 0.99$ (CURVES I); $T_1 = 300°K$, $T_2 = 375°K$, $J_o = 0.95$ (CURVES II); UNIFORM LATTICE TEMPERATURE = 300°K, $J_o = 0.92$ (CURVE III)]

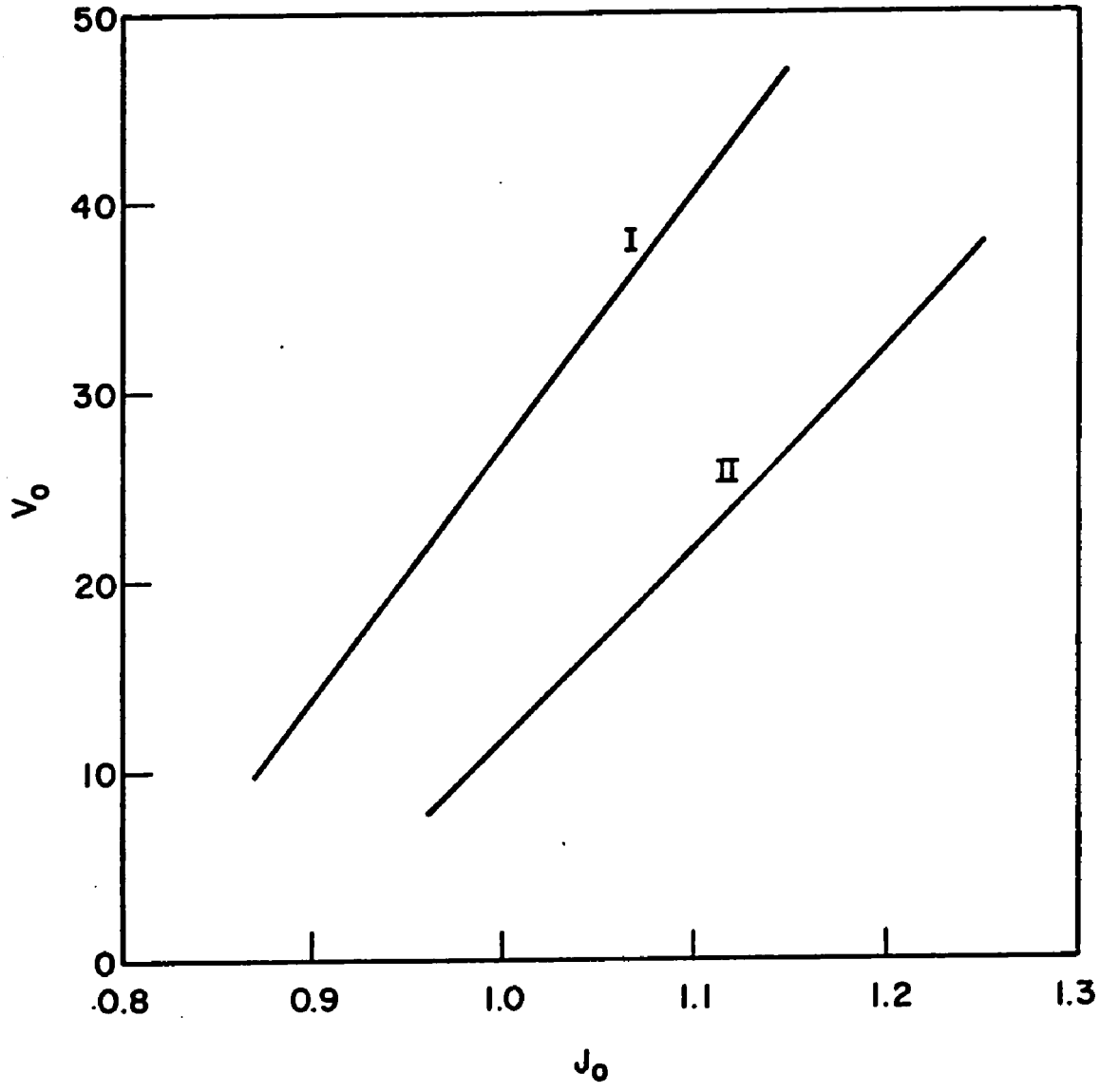


FIG. 6.17 BIAS VOLTAGE VS. NORMALIZED dc CURRENT DENSITY FOR A CRYSTAL OF LENGTH 11.1 μm. [n_o = 5 x $10^{14}/cm^3$, FREQUENCY = 10 GHz AND J_{11} = 0.3 FOR T_1 = 300°K, T_2 = 375°K (CURVE I); T_1 = 375°K, T_2 = 300°K (CURVE II)]

voltage drop for the case where the temperature increases toward the anode is greater because of the greater space-charge accumulation caused by the considerable slowing down of electrons at higher temperatures.

Figure 6.18 shows efficiency vs. bias voltage for a GaAs crystal 11.1 μm long. Results are shown for both of the directions of lattice temperature gradient and are for the same magnitude of normalized RF current density as the case for Fig. 6.15. This figure again shows that the efficiency can be improved considerably if the anode can be kept colder than the cathode.

Unfortunately, because of the higher electric field near the anode, the heat dissipation is higher in that region leading to higher temperatures. It would therefore be desirable to reduce the static-field distortion. The possibility of making the electric field nearly uniform by using a nonohmic cathode has been discussed by Yu et al.[55] Another possible technique involving the control of doping density profile will be discussed in the next chapter.

Whether or not a uniform or nearly uniform electric field can be achieved, it appears that heat sinking the anode rather than the cathode (as is presently done in commercial devices) would help improve the efficiency. This conclusion is supported by the experimental observations of Perlman et al.[46] who have measured efficiency for both directions of bias voltage.

6.6 Summary

It has been shown that an increase in peak-to-valley ratio increases the static-field distortion. Therefore the magnitude of maximum negative

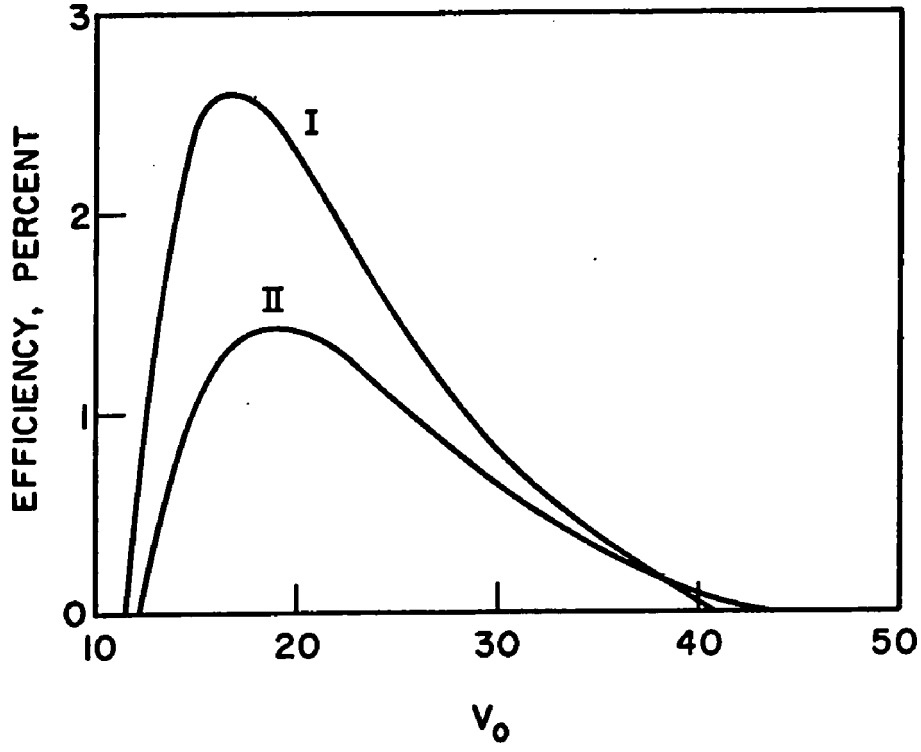


FIG. 6.18 EFFICIENCY VS. BIAS VOLTAGE FOR A CRYSTAL OF LENGTH 11.1 μm. [$n_o = 5 \times 10^{14}/cm^3$, $J_{11} = 0.3$ FOR $T_1 = 375°K$, $T_2 = 300°K$ (CURVE I); $T_1 = 300°K$, $T_2 = 375°K$ (CURVE II)]

resistance does not necessarily decrease with a decrease in peak-to-valley ratio. High operating temperatures may be necessary for significant reduction of the magnitude of negative RF resistance which aids stabilization of the TE device.

An increase in lattice temperature causes a decrease in the (average) dc current flowing through the diode for a constant bias voltage. From the difference in static current when the device is operated pulsed or CW, an estimate of the change in lattice temperature can be obtained from the theoretical current voltage characteristics. From this the thermal resistance of a diode can be calculated.

An increase in lattice temperature causes a reduction in the frequencies of negative resistance because of an overall slowing down of charge carriers. There is also a reduction in the width of this frequency band, along with an increase in the device "Q." The last two factors would lead to smaller bandwidths at higher temperatures.

An increase in signal level causes an increase in the frequencies of negative resistance due to a shortening of the active region. This effect is not noticeable at relatively high temperatures (~500°K).

The peak of negative resistance as a function of bias voltage is reached at lower voltages for higher lattice temperatures. This aids circuit stabilization of the devices at higher bias voltages when they are operated CW.

For uniform lattice temperatures, the dc to RF conversion efficiency is reduced by heating of the lattice. The efficiency is considerably greater when the anode is at a lower temperature than the cathode compared to the case when the cathode is colder or when the lattice temperature is uniform.

CHAPTER VII. INFLUENCE OF THE IONIZED DONOR DENSITY ON THE PERFORMANCE OF STABILIZED TRANSFERRED-ELECTRON DEVICES

7.1 Introduction

In all of the calculations presented in the previous chapters, the ionized donor density has been taken to be $0.5 \times 10^{15}/cm^3$. This was done in order to study the influence of other device parameters and operating conditions on the characteristics of these devices. The effect of the value of ionized donor density on their performance will now be considered. In most cases the effects of diffusion are small, so diffusion has been neglected except where stated.

In the past, several attempts have been made to stabilize "supercritically doped" ($n_o \ell > 10^{12}/cm^2$) TE devices.[21-24,44-47] Such attempts imply a certain advantage in using GaAs crystals with high $n_o \ell$ values, or simply large n_o values when operation in a particular frequency band is considered. This aspect is considered in Section 7.2, where a comparison of diode performance is made for different values of n_o but with the same crystal length or operating frequency. Device characteristics, such as RF impedance, dc to RF conversion efficiency and large-signal bandwidth are examined in detail. The effect of n_o on the static I-V characteristic is also shown. In Section 7.3 the effect of a gradient in ionized donor density on the dc to RF conversion efficiency is discussed.

7.2 Uniform Donor Density

Figure 7.1 shows the relationship between normalized static current density and the dc voltage across the crystal for two different lengths and

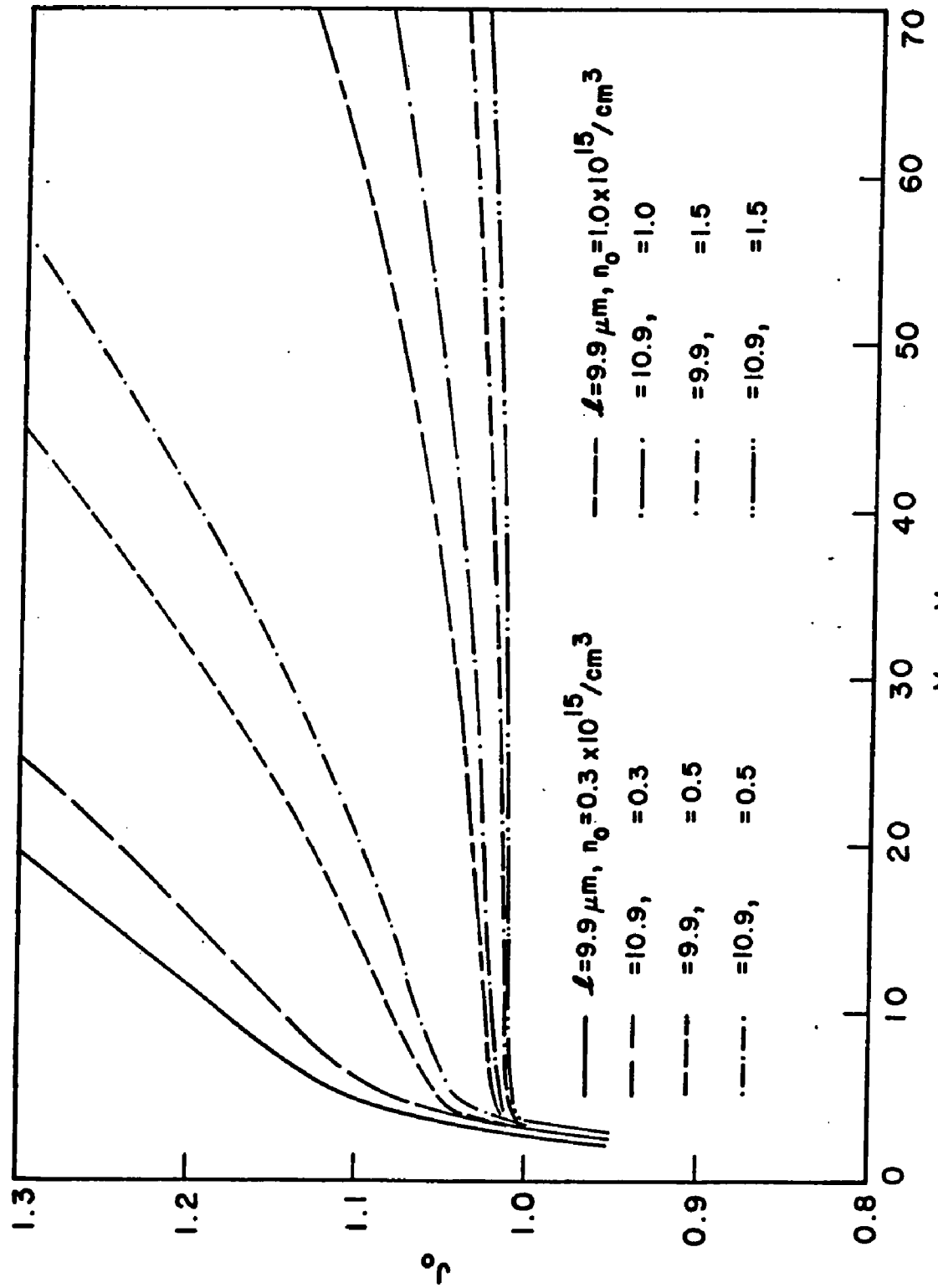


FIG. 7.1 THE RELATIONSHIP BETWEEN NORMALIZED CURRENT DENSITY AND BIAS VOLTAGE FOR THE SMALL-SIGNAL CASE WITH DIFFUSION EFFECTS NEGLECTED. (J_{11} = 0.0001 AND LATTICE TEMPERATURE = 375°K)

for four different values of ionized donor density. The results are for a small-signal (RF) case at a constant temperature of 375°K. The corresponding large-signal results are shown in Fig. 7.2. It should be noted here that all of the curves converge to the origin, since $V_o = 0$ when $J_o = 0$, irrespective of crystal length or donor density. At low donor densities, and if the length is not too great compared to the values shown in the figure, the current-voltage relationship is almost ohmic in nature. At higher donor densities, the current-voltage characteristic stays nearly linear up to a certain value of J_o (nearly 1.0 for $n_o = 1.5 \times 10^{15}/cm^3$ in Fig. 7.1 and 0.8 in Fig. 7.2). Beyond that value a slight fractional increase in J_o causes a relatively large increase in V_o. This happens when the static field in the crystal starts to increase beyond the threshold value, at first near the anode and then along most of the crystal. Parts of the crystal are now biased in the negative differential mobility region of the v-E characteristic and this leads to a slowing down of the charge carriers and consequent space-charge accumulation. Because of the large donor density, space-charge accumulation increases rapidly with a small fractional increase in J_o and leads to a rapid increase in static field, which in turn results in a large voltage drop across the crystal. On the other hand when n_o is small, a fractional increase in J_o causes only a small increase in space-charge accumulation and consequently a small increase in voltage. For a material with a relatively large peak-to-valley ratio (or a lower lattice temperature) the deviation from ohmic behavior would be greater than that shown in Fig. 7.1 because of greater space-charge accumulation.

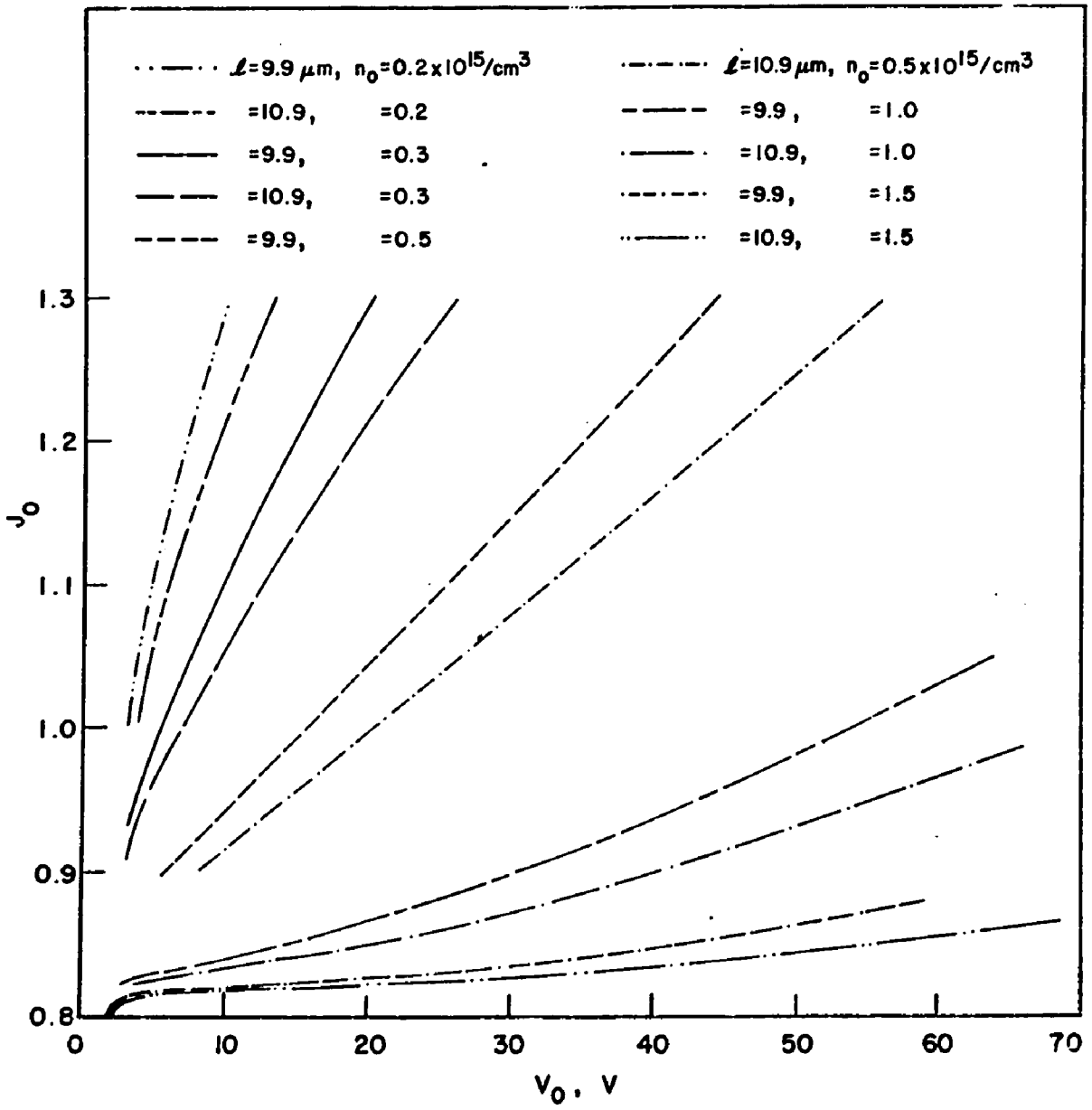


FIG. 7.2 THE RELATIONSHIP BETWEEN NORMALIZED CURRENT DENSITY AND BIAS VOLTAGE FOR THE LARGE-SIGNAL CASE WITH DIFFUSION EFFECTS NEGLECTED. (J_{11} = 0.3, LATTICE TEMPERATURE = 375°K AND FREQUENCY = 10 GHz)

It was shown in Section 3.3 that a decrease in static current occurs when a signal of large amplitude is injected into a GaAs crystal biased with a constant voltage supply. This can be seen clearly by comparing the small- and large-signal cases of Figs. 7.1 and 7.2, respectively. The figures show that for the same normalized value of RF current density, the decrease in current is much greater when the donor density is relatively large. For large n_o, the same normalized value of J_{11} produces much larger RF electric field values than in a case for smaller n_o. Therefore the RF power per unit area is much greater for larger n_o. Thus, for the same value of J_{11}, large-signal effects are stronger when n_o is relatively large.

This discussion shows that the current-voltage relationship of a stabilized TE device is characteristic of the donor density, length and peak-to-valley ratio of the material. In practical devices, the nature of the observed current-voltage relationship will also be affected by any contact or other series resistance external to the crystal. When such a resistance is present, the deviation from ohmic behavior will be smaller and may give the illusion of a lower carrier density or a smaller peak-to-valley ratio.

In order to determine the effect of donor density on the dc to RF conversion efficiency obtainable in these devices, calculations of efficiency were made for fixed J_{11} and frequency as a function of the bias current density J_o. At each bias, the best efficiency was obtained by varying the crystal length. The results are shown in Fig. 7.3 where the best efficiency vs. bias for different values of n_o is plotted. The

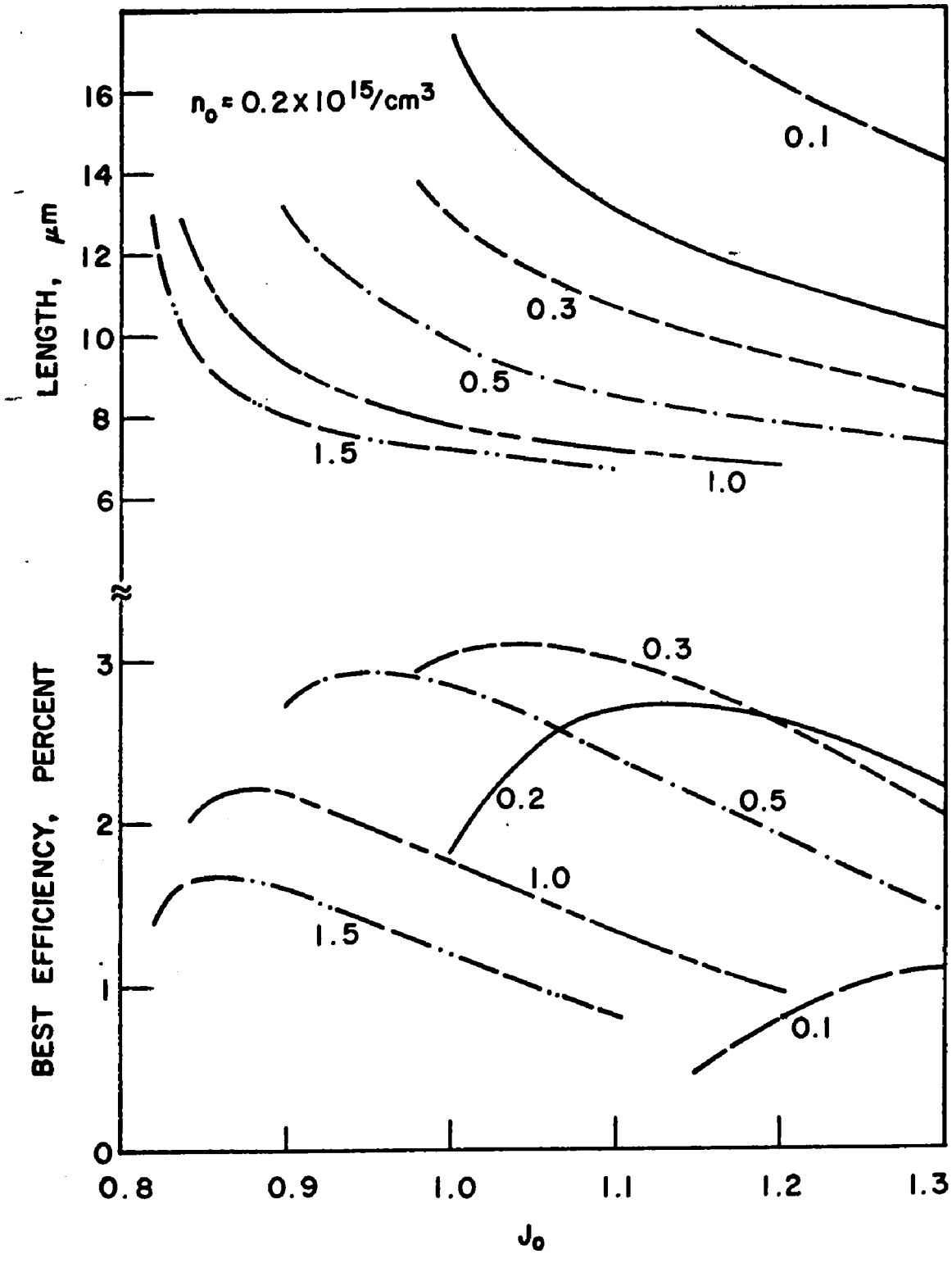


FIG. 7.3 BEST EFFICIENCY VS. J_o FOR CONSTANT $J_{11} = 0.3$ AND THE CRYSTAL LENGTH FOR WHICH IT OCCURS, WITH DIFFUSION EFFECTS NEGLECTED. (LATTICE TEMPERATURE = 375°K AND FREQUENCY = 10 GHz)

length for which this maximum efficiency occurs is also shown in the figure. It may be pointed out that efficiency is independent of area as long as the area is not too large for skin effects to be important and not too small for the growth of space-charge waves to be affected (see Appendix A). Figure 7.3 shows that the efficiency is maximum for an ionized donor density of approximately $0.3 \times 10^{15}/cm^3$.

The calculations of Fig. 7.3 were made for a constant J_{11} of 0.3. The results may be somewhat different if J_{11} is varied. In order to maximize the efficiency for each value of n_o it was calculated as a function of J_{11}. For each n_o, the value of J_o at which the maximum occurs in Fig. 7.3 was chosen for the calculations. The results are shown in Fig. 7.4. These results indicate that the optimum value (for best efficiency) of n_o at 10 GHz is approximately $0.2 \times 10^{15}/cm^3$ and it occurs for a very large value of J_{11} (approximately 0.6). In real devices where diffusion effects exist and where lattice temperature, donor density and area may not be uniform, the optimum value of n_o is expected to be 0.2 or $0.3 \times 10^{15}/cm^3$.

The previous discussion shows that for X-band operation at 375°K, the efficiency of these devices is maximum for a donor density of approximately 0.2 or $0.3 \times 10^{15}/cm^3$. The corresponding $n_o \ell$ product is well below $10^{12}/cm^2$.

Figures 7.5 and 7.6 show the resistance and reactance of TE devices with different values of n_o but with the same length of 9.9 μm and the same dc resistance at low voltages (approximately 2.5 Ω). This resistance is kept the same by choosing the area proportional to the inverse of the

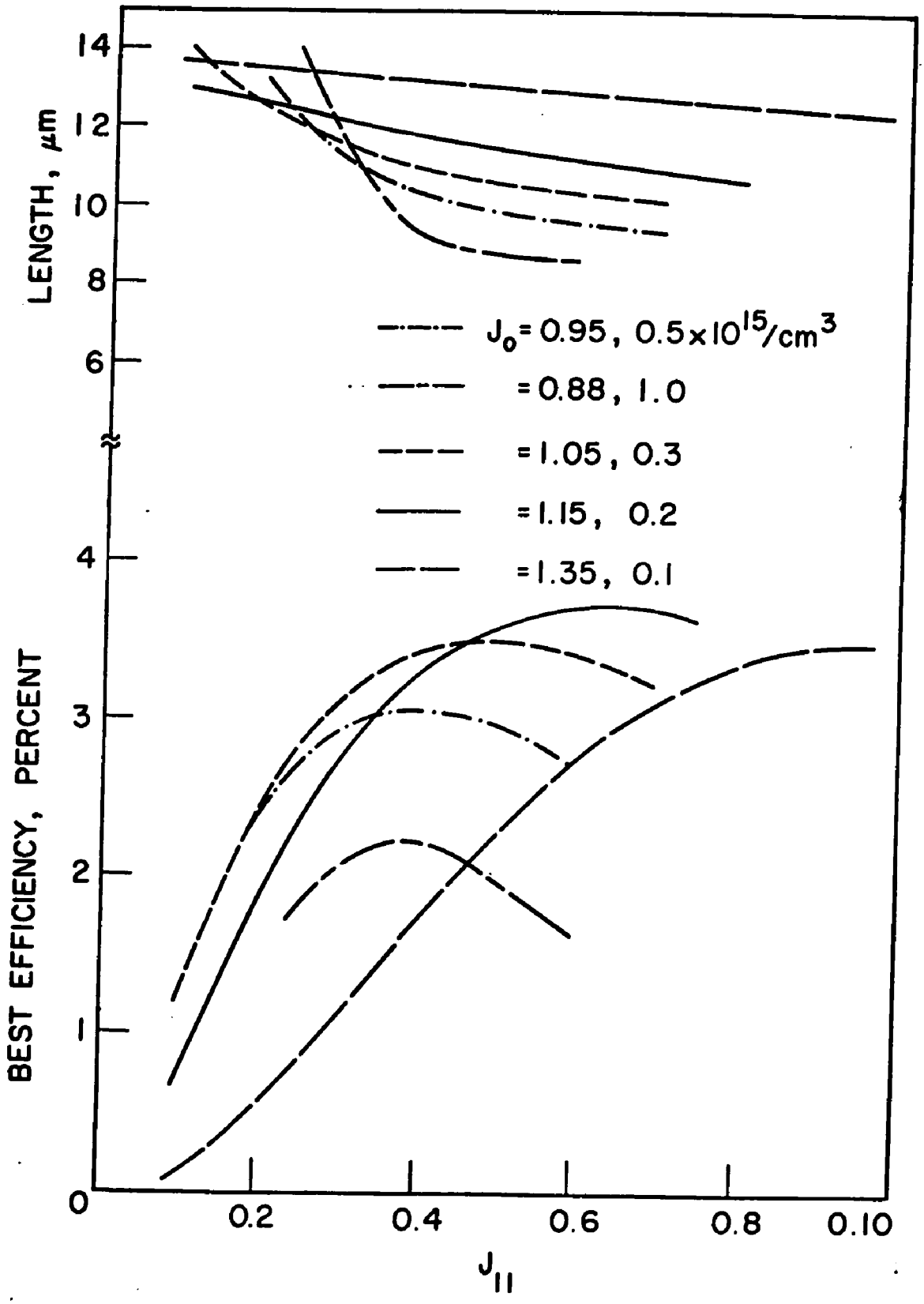


FIG. 7.4 BEST EFFICIENCY AND OPTIMUM CRYSTAL LENGTH VS. J_{11} FOR CONSTANT J_o WITH DIFFUSION EFFECTS NEGLECTED. (FREQUENCY = 10 GHz AND LATTICE TEMPERATURE = 375°K)

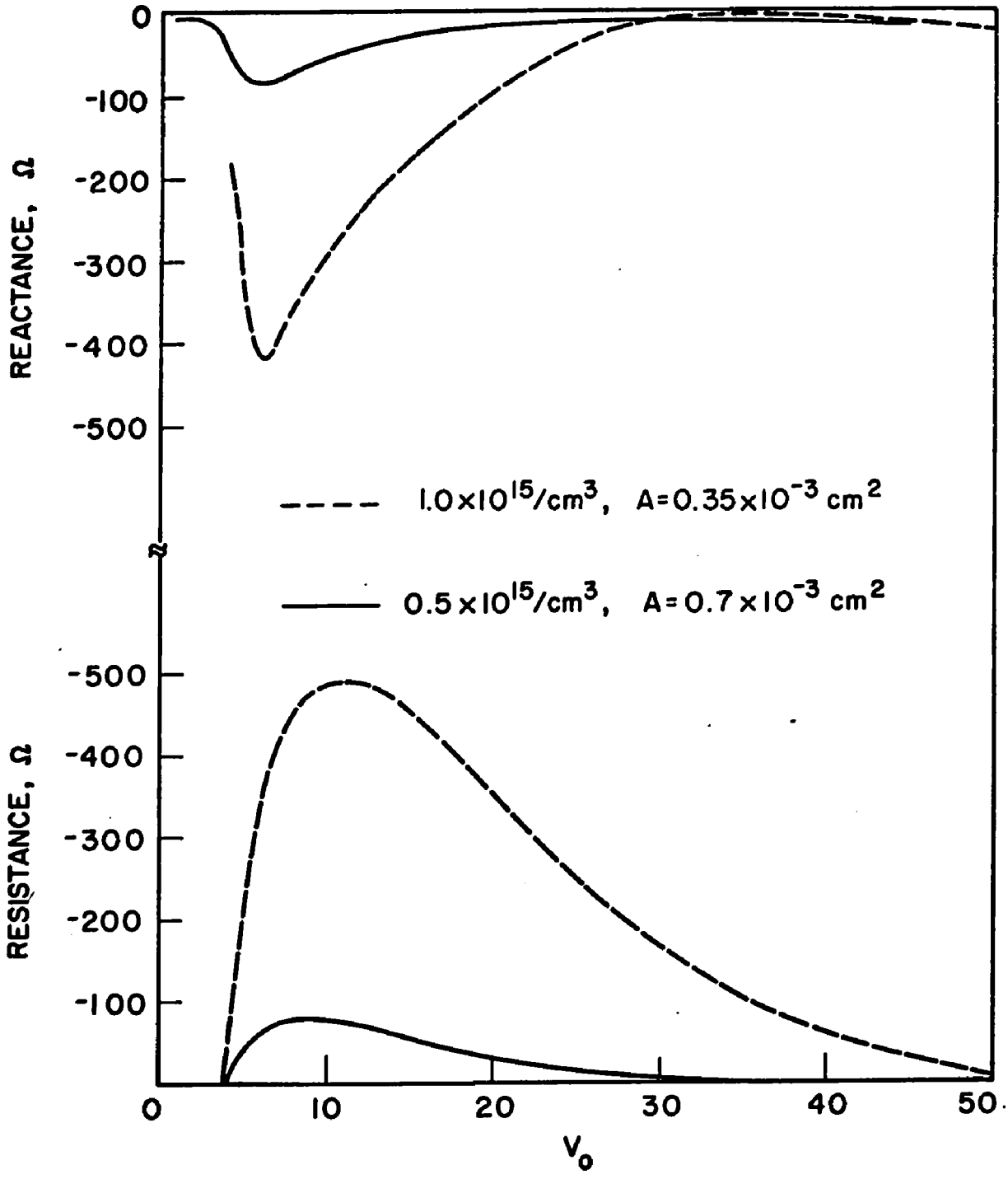


FIG. 7.5 RESISTANCE AND REACTANCE VS. BIAS VOLTAGE FOR TWO DIFFERENT VALUES OF n_o WITH DIFFUSION EFFECTS NEGLECTED. (LATTICE TEMPERATURE = 375°K, FREQUENCY = 10 GHz, ℓ = 9.9 μm AND J_{11} = 0.0001)

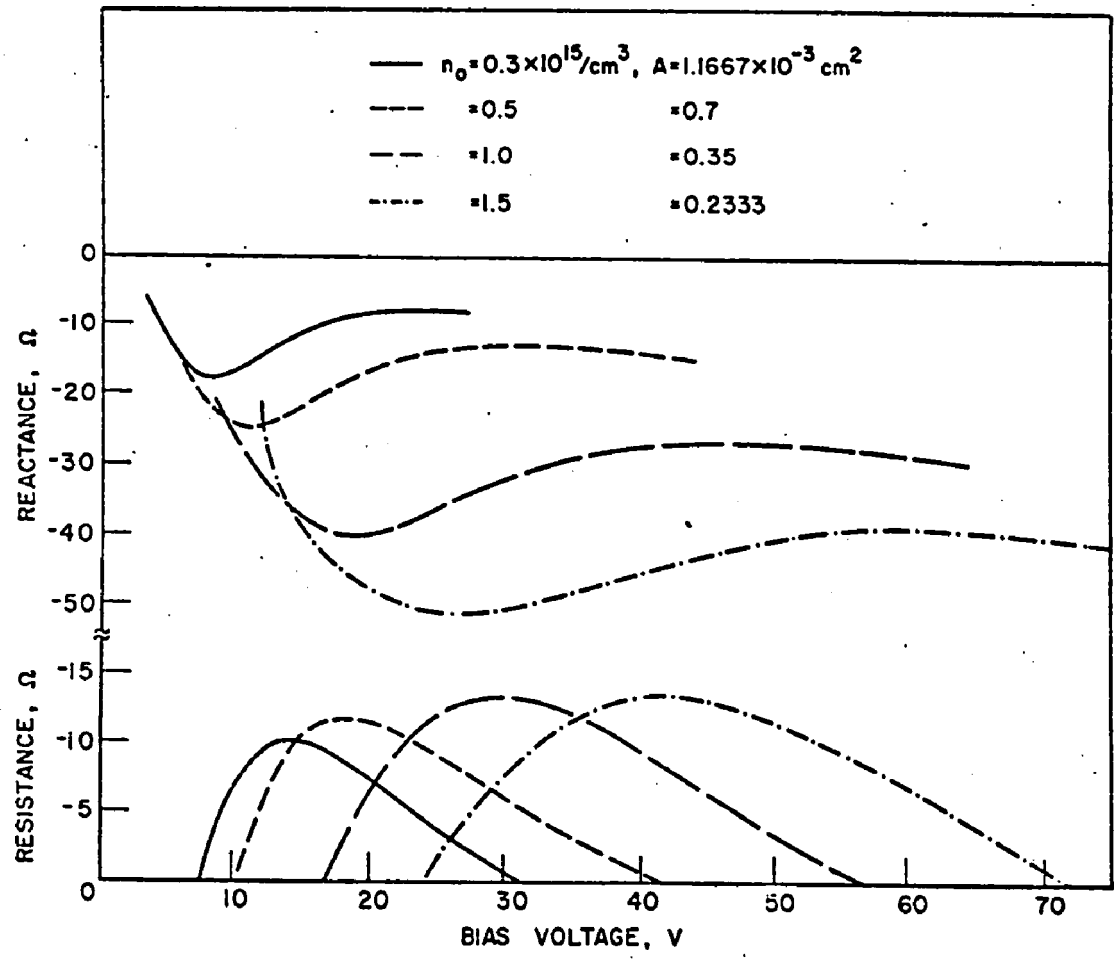


FIG. 7.6 LARGE-SIGNAL (J_{11} = 0.3) RESISTANCE AND REACTANCE FOR DIFFERENT n_o, WITH DIFFUSION EFFECTS NEGLECTED. (LATTICE TEMPERATURE = 375°K, FREQUENCY = 10 GHz AND ℓ = 9.9 μm)

value of n_o. The signal frequency is 10 GHz. Figure 7.5 is for small signals and 7.6 is for $J_{11} = 0.3$. For the small-signal case, the maximum negative resistance is seen to be considerably smaller for smaller n_o, but the reactance is correspondingly small so that the device Q is not affected appreciably. At large signals (Fig. 7.6), the devices with low n_o have a greater Q which aids the attainable bandwidth.[83]

For small signals (Fig. 7.5) the minimum bias voltage required for negative resistance is approximately the same for different n_o. For the large-signal case, it is much greater for larger values of n_o. This indicates that for the same J_{11}, devices with lower n_o will operate at lower voltages than devices with higher n_o. This may be partly due to the greater large-signal effects when n_o is high, as already discussed in this section.

The values of dc to RF conversion efficiency corresponding to the results of Fig. 7.6 are shown in Fig. 7.7. Even though the maximum negative resistance is greater for larger n_o values, the efficiency is smaller because of the higher bias voltage at which the maximum occurs. The relative magnitudes of the maximum efficiency are different for different device lengths. If the crystal length is 10.9 μm and the rest of the parameters are the same as those of Fig. 7.6, the efficiency is highest for $n_o = 0.3 \times 10^{15}/cm^3$ for the particular length and frequency assumed in the figure.

In order to assess the bandwidth capabilities of these devices for different donor densities, the resistance and reactance were calculated as functions of frequency for different values of n_o and are shown in Fig. 7.8. The low-field resistance has again been kept the same

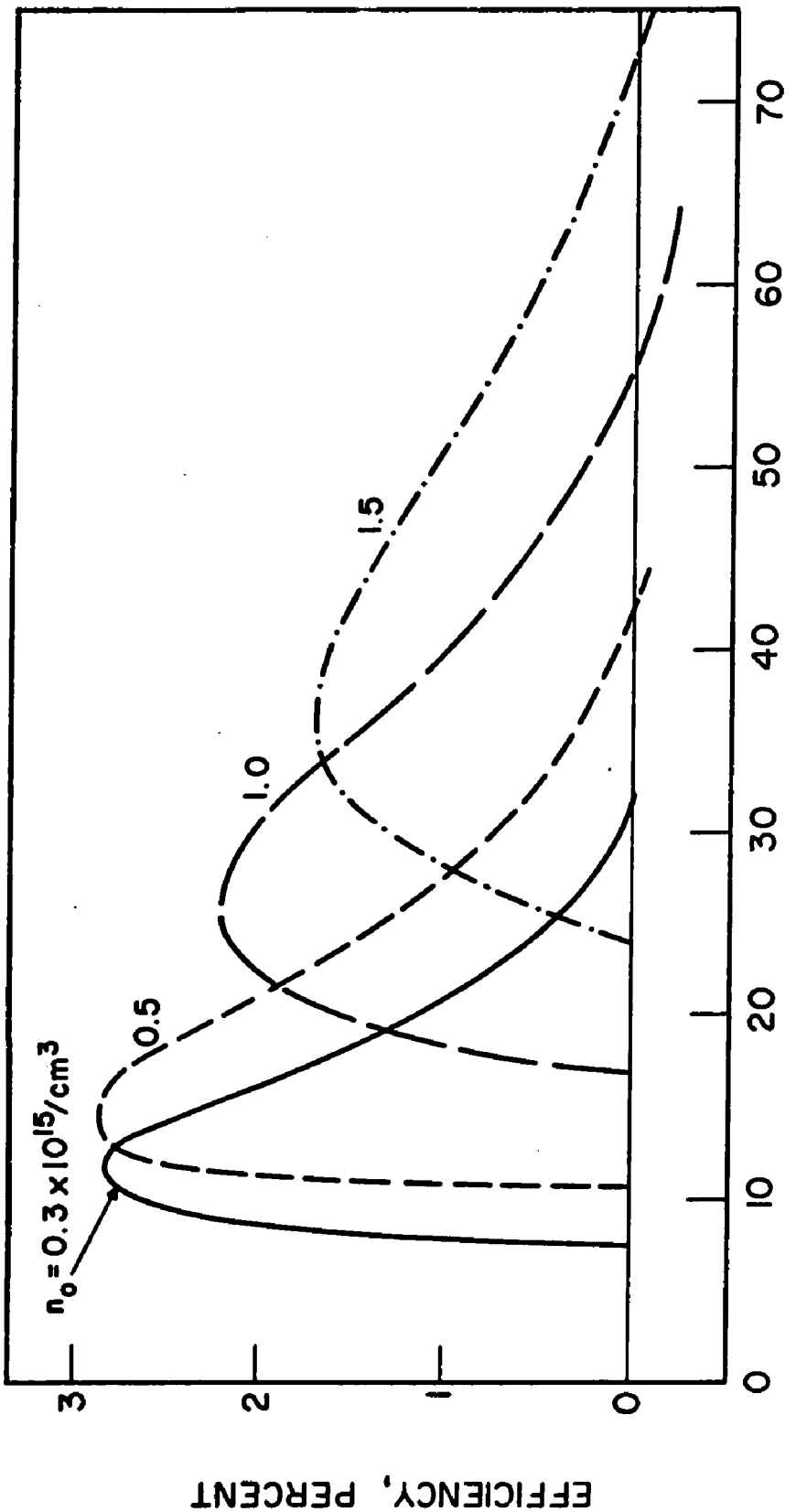


FIG. 7.7 Dc TO RF CONVERSION EFFICIENCY VS. BIAS VOLTAGE CORRESPONDING TO THE DATA OF FIG. 7.6.

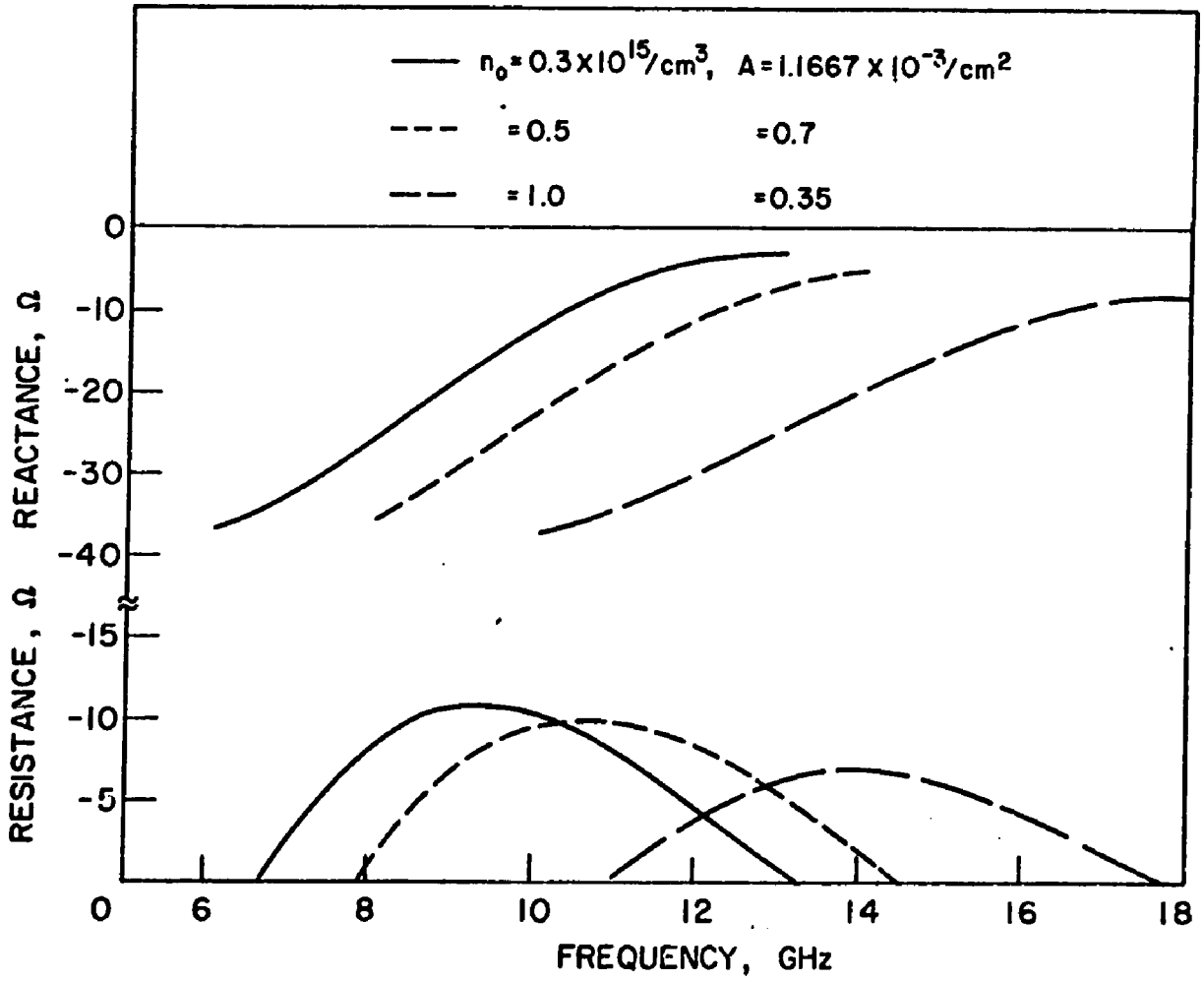


FIG. 7.8 RESISTANCE AND REACTANCE VS. FREQUENCY WITH DIFFUSION EFFECTS NEGLECTED. (CONSTANT BIAS VOLTAGE = 14 V, ℓ = 9.9 μm, J_{11} = 0.3 AND LATTICE TEMPERATURE = 375°K)

(approximately 2.5 Ω) by choosing appropriate values of area. The bias voltage was also kept the same (14 V) for each case by adusting J_o. The rest of the parameters are the same as those of Fig. 7.6. The corresponding values of efficiency are shown in Fig. 7.9. No appreciable change in the width of the large-signal negative resistance region is seen with change in n_o. However, in accordance with the results of Fig. 7.7, the device Q is seen to be smaller for smaller values of n_o. Thus for the range of values of n_o shown in Fig. 7.8, the lower values of n_o should provide the maximum bandwidth in practical devices.[83]

In Fig. 7.8 the negative resistance is seen to occur at higher frequencies for higher n_o. Examination of the static-field profile inside the crystals shown in Fig. 7.10 indicates that the active region ($E_{th} < E_o < \sim 15$ kV/cm) is shorter for higher n_o which leads to higher frequency operation.

In the calculations presented in this chapter so far, diffusion effects have been neglected. In order to see the relative effect of diffusion for different n_o, calculations of efficiency were made as a function of frequency for $n_o = 0.3 \times 10^{15}/cm^3$ and $0.5 \times 10^{15}/cm^3$. The rest of the parameters are the same as those of Fig. 7.9. The results are shown in Fig. 7.11. A comparison of Figs. 7.9 and 7.11 shows that the efficiency is reduced somewhat as expected and the frequencies of negative resistance increase when diffusion effects are included. The effect is similar both qualitatively and quantitatively for both values of n_o.

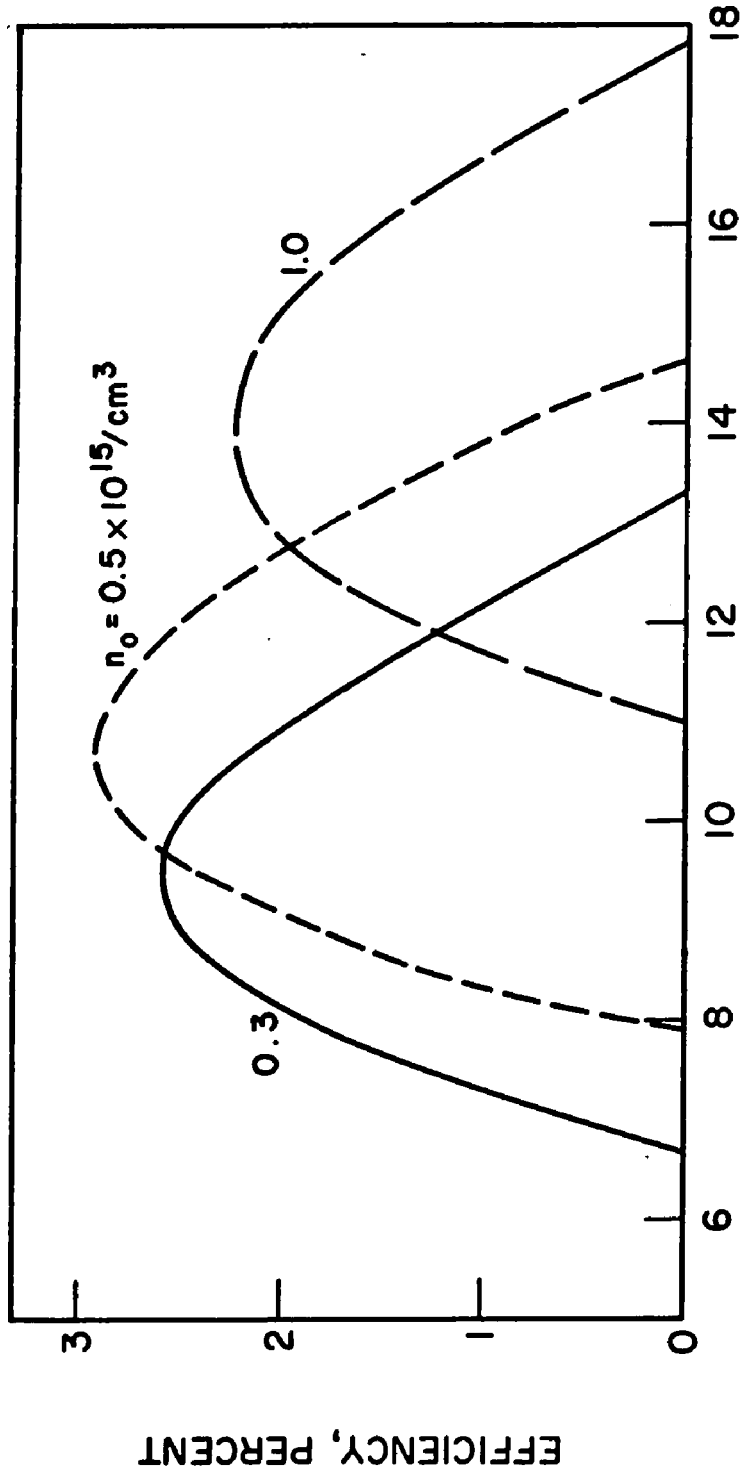


FIG. 7.9 EFFICIENCY VS. FREQUENCY FOR THE CASES OF FIG. 7.8.

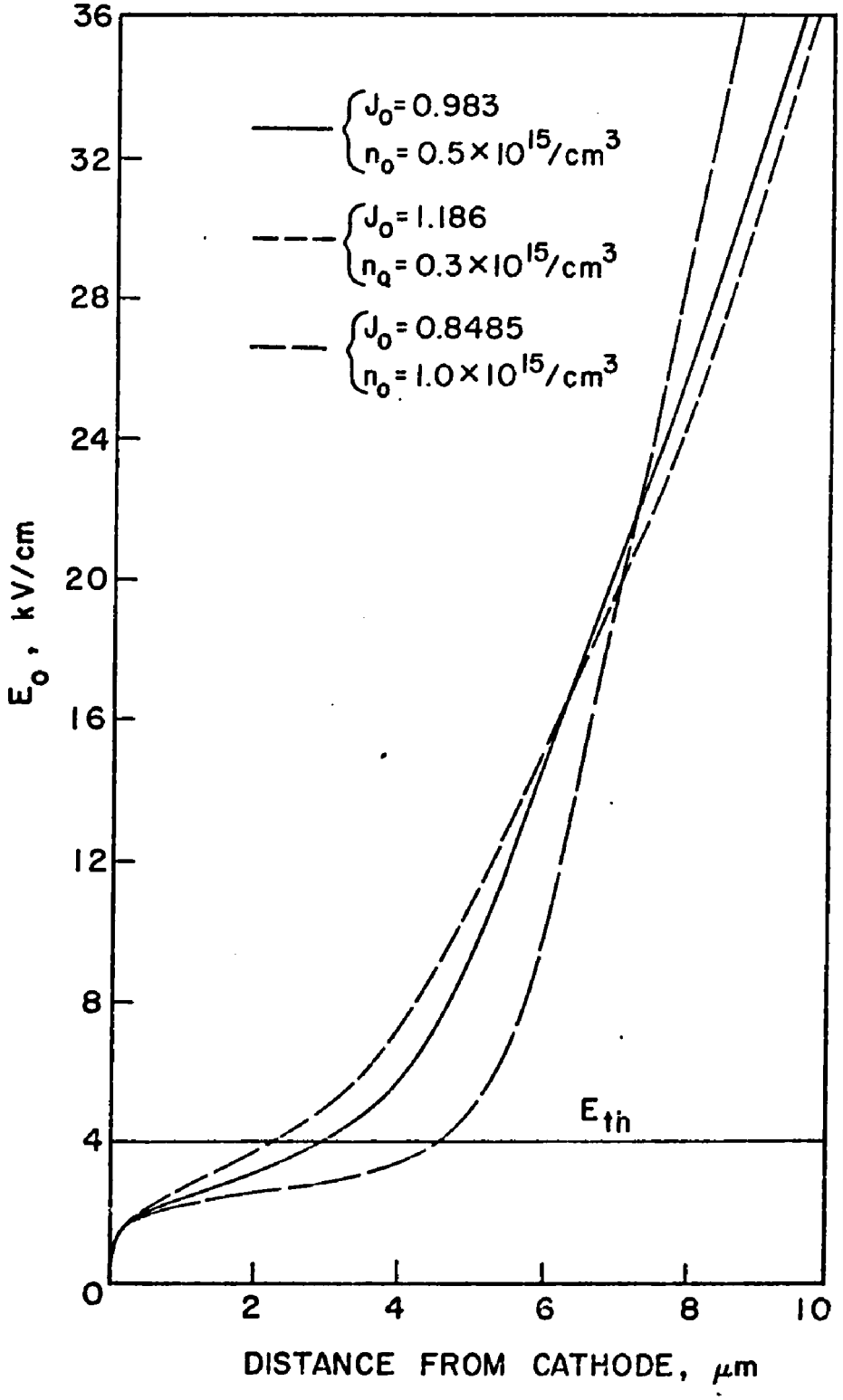


FIG. 7.10 STATIC FIELD VS. DISTANCE FROM THE CATHODE FOR THE CRYSTALS OF FIG. 7.8.

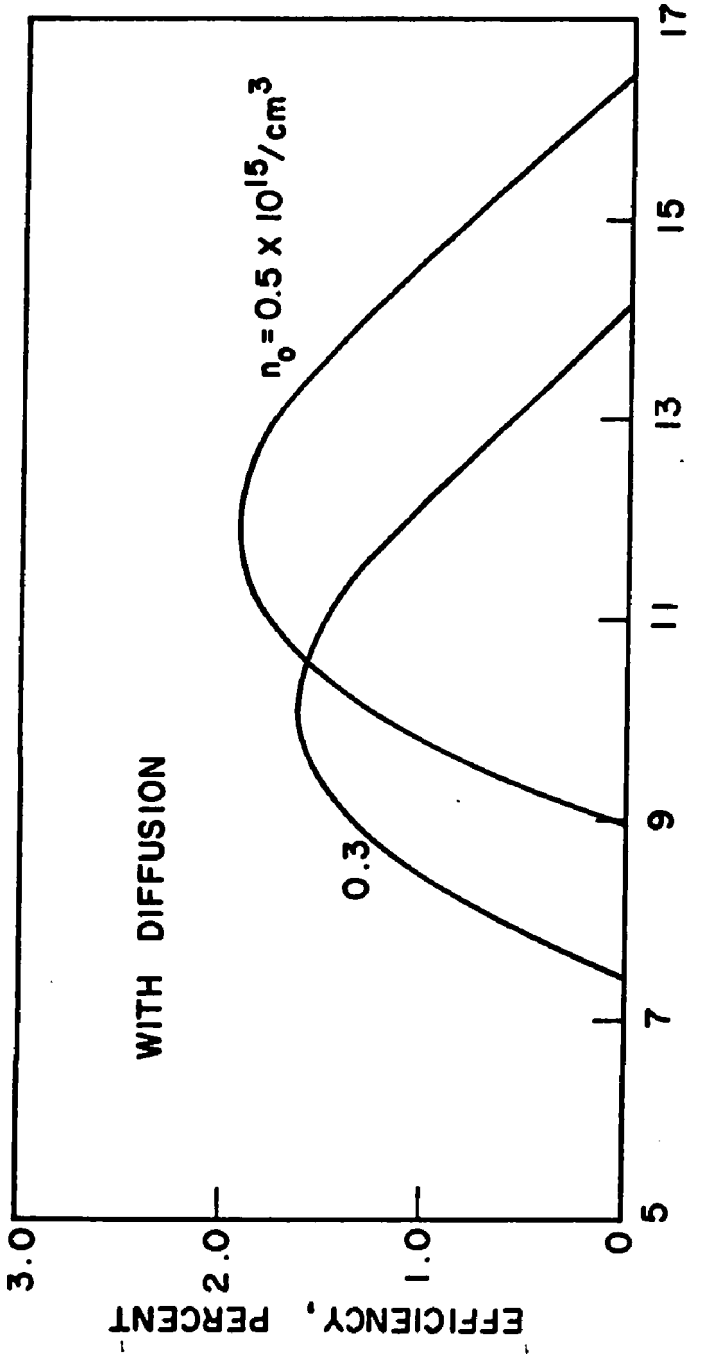


FIG. 7.11 EFFICIENCY VS. FREQUENCY FOR CASES SIMILAR TO THOSE OF FIG. 7.9 EXCEPT DIFFUSION EFFECTS ARE INCLUDED.

7.3 Nonuniform Doping

It was shown in Section 6.5 that the efficiency of a stabilized TE device increases if the anode temperature is lower than the cathode temperature, but in these devices, the electric field near the anode is much higher than the field near the cathode. Thus there is more heat dissipated near the anode than near the cathode and the anode temperature will be higher. This would tend to reduce the efficiency. Therefore, it would be of interest to reduce the field near the anode. Further, the high field near the anode causes the region to be passive and because of the large voltage drop across this region the efficiency of the device is greatly reduced. Thus a reduction of the static-field distortion near the anode would improve the dc to RF conversion efficiency of the device.

The static-field distortion is caused by the accumulation of excess carriers (above n_o) near the anode. If n_o itself is increased near the anode, the excess carrier density will be reduced making the electric field less nonuniform.

Calculations of efficiency were made for GaAs crystals having a nonuniform doping to see if the efficiency can be increased by increasing the doping near the anode. Linear density gradients were considered. The analytical procedure for studying devices with doping density gradients was described in Section 2.4. Figure 7.12 shows the type of doping profile considered and the following parameters are assumed:

$n_{o1} = 0.24 \times 10^{15}/cm^3$,

$n_{o2} = 0.36 \times 10^{15}/cm^3$,

$X_1 = 2.5$ μm and

$X_2 = 11$ μm.

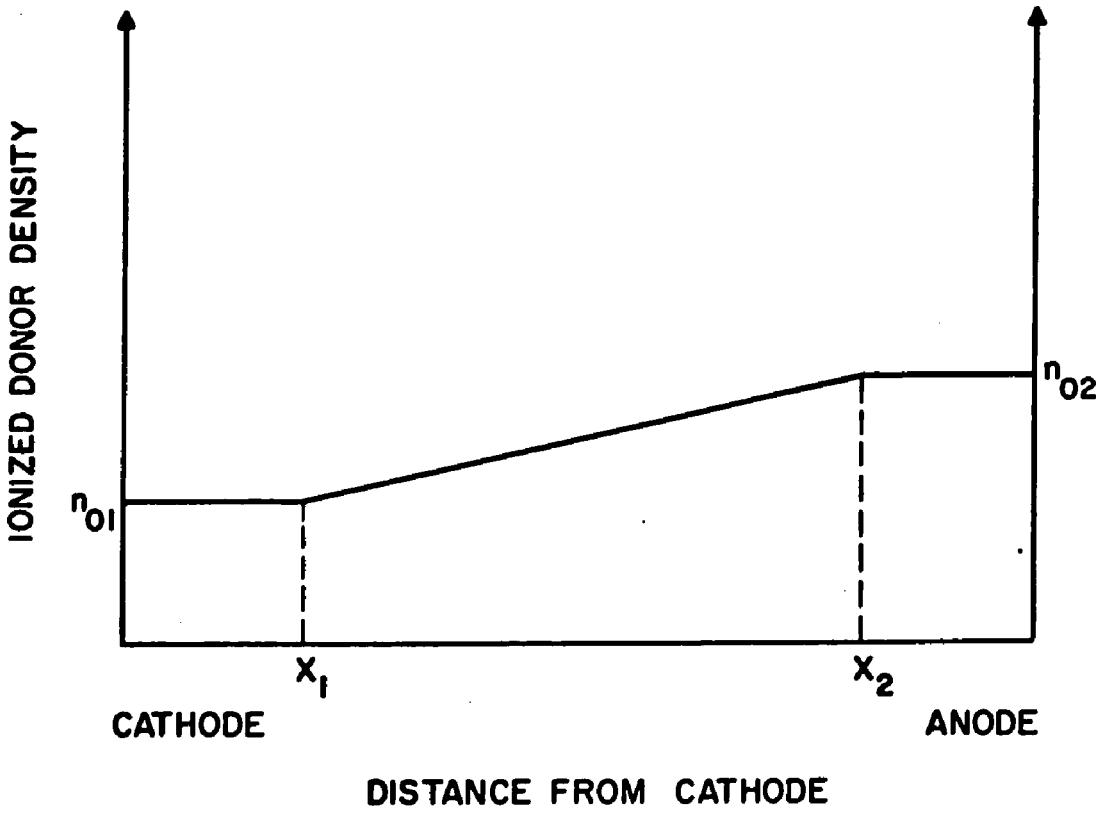


FIG. 7.12 GENERAL NATURE OF THE DOPING PROFILE CONSIDERED.

At each bias the crystal length was varied to get the maximum efficiency for a constant $J_{11} = 0.4$. The results are shown in Fig. 7.13. The length for which the maximum efficiency occurs for each bias is also shown. Corresponding values of efficiency for uniformly doped crystals with $n_o = 0.3 \times 10^{15}/cm^3$ (average of 0.24 and 0.36 x 10^{15}) are included in the figure for comparison. A considerable improvement in efficiency can be seen for the nonuniformly doped crystal.

7.4 Summary

The current-voltage relationship of a stabilized TE device was shown to be characteristic of the donor density as well as the peak-to-valley ratio of the material. The deviation from ohmic behavior is great if n_o is high or if the peak-to-valley ratio is large.

It was also seen that there is an optimum value of n_o (or $n_o \ell$) for which the dc to RF conversion efficiency is the highest. For X-band operation, this value of n_o is approximately 0.2 or $0.3 \times 10^{15}/cm^3$. The corresponding $n_o \ell$ product is below $10^{12}/cm^2$. The large-signal bandwidth of the negative resistance is not affected appreciably by a change in n_o, but the device Q is smaller for lower values of n_o. The efficiency of the devices was shown to be improved if the donor density is increased from the cathode to the anode.

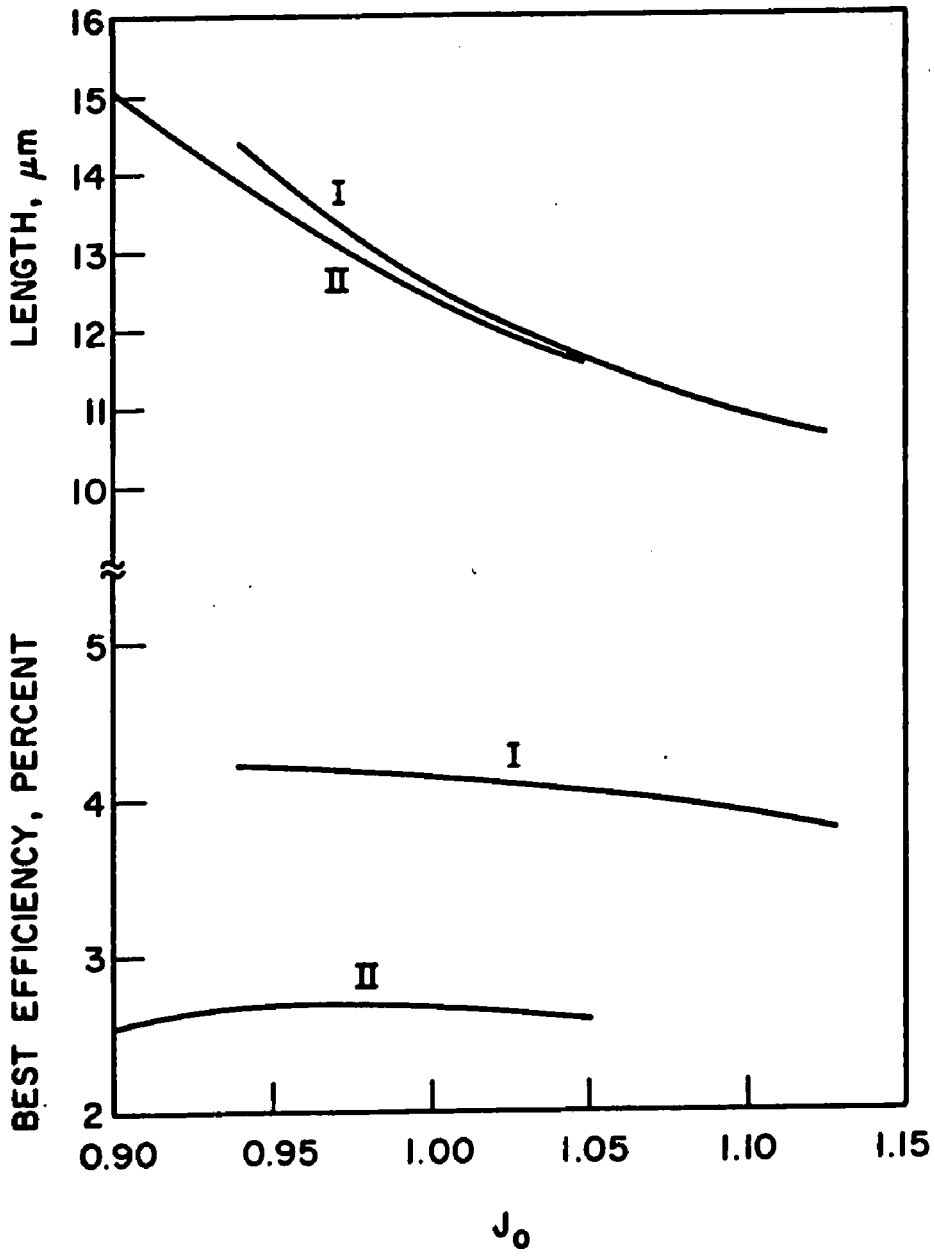


FIG. 7.13 BEST EFFICIENCY AND THE CRYSTAL LENGTH FOR WHICH IT OCCURS VS. NORMALIZED dc CURRENT DENSITY AT ROOM TEMPERATURE AND 10 GHz. [$n_{o1} = 0.24 \times 10^{15}/cm^3$, $n_{o2} = 0.36 \times 10^{15}/cm^3$, $X_1 = 2.5$ μm, $X_2 = 11$ μm (CURVES I); UNIFORMLY DOPED CRYSTAL WITH $n_o = 0.3 \times 10^{15}/cm^3$ (CURVES II)]

CHAPTER VIII. EXPERIMENTAL STUDY OF STABILIZED TRANSFERRED-ELECTRON AMPLIFIERS

8.1 Introduction

A large-signal analysis of stabilized TE devices and numerical calculations of the properties of these devices have been presented in the previous chapters. In order to check the validity of the analysis an experimental study was conducted to observe the characteristics predicted by the analysis. In this chapter the results of the experimental investigation are discussed. Only qualitative comparisons have been made. Most of the data presented here were taken under CW conditions. A constant voltage supply was used to bias the diodes.

The circuit and the diodes used for the study are described in Section 8.2. Section 8.3 discusses large-signal effects, and the effect of lattice heating in CW operation on the current-voltage relationship. The RF characteristics are discussed in Section 8.4. The effect of bias voltage on frequency, on small- and large-signal gain and on the linearity of gain is shown and compared with the theoretical results. The conditions under which gain expansion occurs are also discussed.

8.2 Description of the Circuit and the GaAs Diodes Used for the Experimental Study

A schematic diagram of the circuit used for most of the tests is shown in Fig. 8.1. The diode is mounted in series with the center conductor at the end of a 50-Ω coaxial transmission line. A circulator

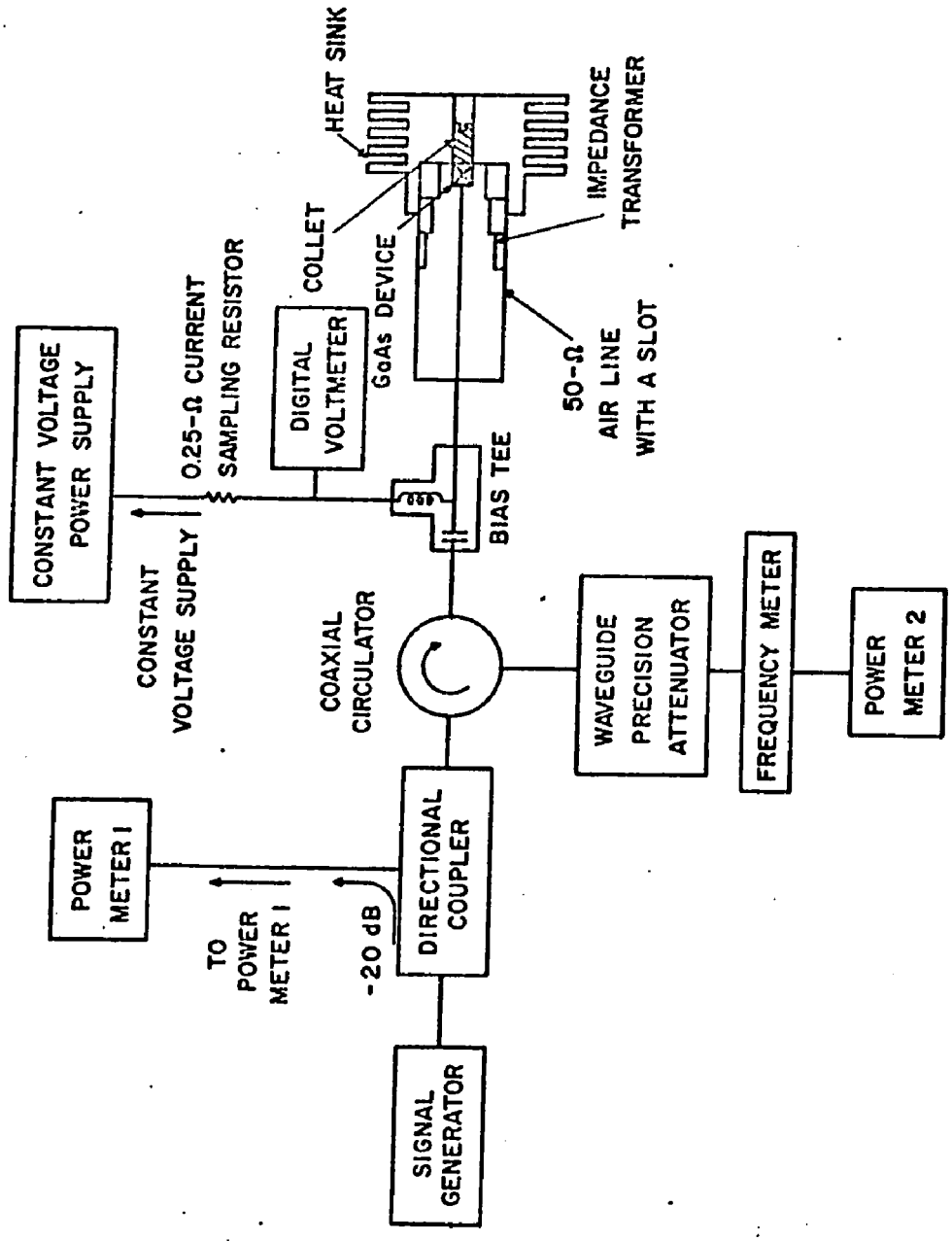


FIG. 8.1 SCHEMATIC DIAGRAM OF THE CIRCUIT USED FOR THE EXPERIMENTAL STUDY OF STABILIZED TE AMPLIFIERS.

separates the input and output signals. The bias current is determined by measuring the voltage across a small (0.25 Ω) resistor inserted in series with the diode, and the bias voltage is measured directly across the diode.

Corrections for circuit loss were made as follows. The coaxial line with the diode was replaced by a short and the variable attenuator in the output arm was adjusted until power meters 1 and 2 gave the same reading. A movable short was used to ensure that the output did not vary appreciably for different positions of the short circuit. The input power to the amplifier was evaluated allowing for circuit loss from the output of the directional coupler to the input of the coaxial line with the diode.

Movable tuning slugs of length $\lambda/4$ (at 10 GHz) were used for the purpose of controlling the circuit impedance presented to the diode. A slot in the transmission line allowed for the adjustment of the position of the slugs. For effective heat sinking, the diode was mounted in a copper collet with the collet gripping the heat sink end of the diode. The collet could be screwed tightly into a larger heat sink with fins. A fan was used to aid the cooling.

Two Chebychev transformers[85] were made to transform the 50-Ω coaxial line impedance to 25 Ω and 10 Ω, respectively. These are henceforth referred to as 25-Ω and 10-Ω transformers. Each transformer had three slugs of length $\lambda/4$ at 10 GHz. The 25-Ω transformer used slugs of characteristic impedance: 40.5 Ω, 30.25 Ω and 25 Ω, and the 10-Ω transformer used slugs of impedance: 30 Ω, 16.3 Ω and 10 Ω.

The transformers were designed to have a bandwidth of approximately 7 GHz for the 25-Ω transformer and approximately 5 GHz for the 10-Ω transformer allowing a maximum theoretical reflection coefficient (with a matched load) of 0.05 and 0.11, respectively. The advantage of testing the diodes in a circuit with nearly constant resistance over a wide frequency band is that the impedance of the diode should be easily discerned qualitatively from the observed gain.

The diodes were all obtained from Monsanto Company. They consist of encapsulated epitaxial n^+nn^+ chips (approximately 0.008-inch square) mounted on the copper studs of the packages. The values of lead inductance and package capacitance given by the supplier are 0.46 nH and 0.26 pF, respectively. Some of the basic characteristics of the crystals are shown in Table 8.1. The values of n_o, ℓ and mobility given in the table are the ones provided by the manufacturer. The thermal resistance given by the supplier is 30°C/W. Diode Nos. 3 through 5 are from the same wafer. In the following sections the diodes will be referred to by the numbers given in the table.

Table 8.1

Device Parameters

Diode No.	n_o (/cm^3)	ℓ (μm)	Resistance at Low Bias (Ω)	Hall Mobility (cm^2/V·s)
1	1.0×10^{15}	11.0	5.8	6300
2	0.9×10^{15}	8.5	5.3	--
3	0.5×10^{15}	14.0	2.7	7060
4	0.5×10^{15}	14.0	2.7	7060
5	0.5×10^{15}	14.0	7.6	7060

8.3 The Current-Voltage Relationship

Figure 8.2 shows bias current as a function of bias voltage for diode No. 3. Current values for both pulsed and CW operation are shown. The diode was mounted in the 50-Ω line with the 10-Ω transformer placed at the diode end. No oscillations were observed at any bias (within the limits shown) in this circuit. The pulsed characteristic is for a pulse width of 0.5 μs and a repetition rate of 1000 pps. The pulse width is smaller than the thermal time constant of the diode since no appreciable change in diode behavior was seen during the pulse.

For the same bias voltage, the bias current is seen to be smaller for dc bias than when the diode is operated with a pulsed bias. This decrease in current is due to an increase in the lattice temperature caused by the dc power dissipation. The decrease in current depends on the amount of dc power dissipated in the diode which is higher, the higher the bias voltage. Thus, the device even shows a negative differential resistance at very low frequencies (below the inverse of the thermal time constant). Clearly this negative resistance is of no consequence at RF frequencies.

By comparison of the pulsed and CW results of Fig. 8.2 the thermal resistance of the diode can be calculated. This can be done by assuming that the low-field mobility of GaAs with n_o in the vicinity of $10^{15}/cm^3$ is roughly inversely proportional to lattice temperature.[72] The value calculated for diode No. 3 is approximately 43°/W.

It was shown in Section 3.3 that when a large signal is injected into a diode, the bias current will decrease if the diode is biased with

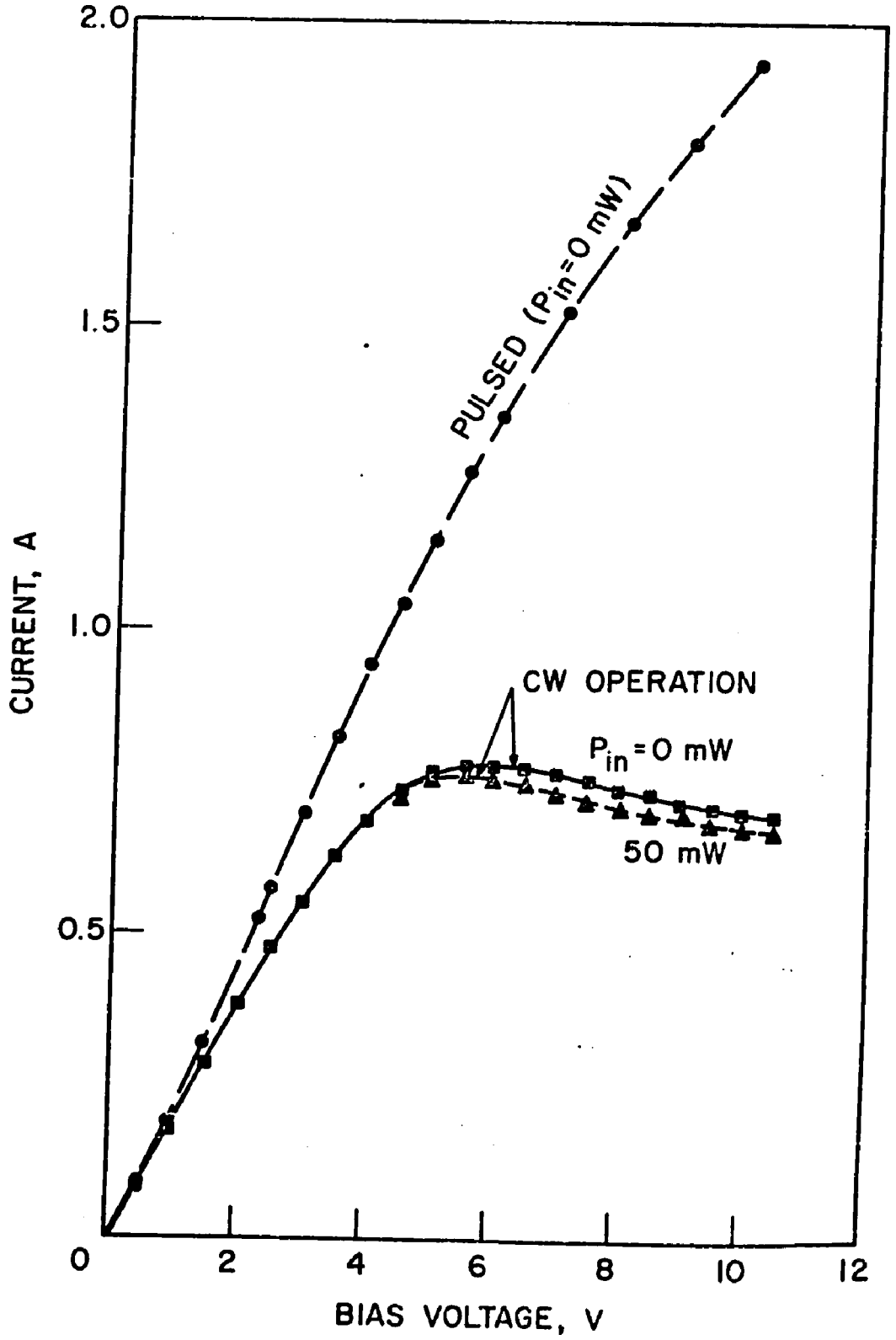


FIG. 8.2 THE RELATIONSHIP BETWEEN BIAS CURRENT AND BIAS VOLTAGE FOR DIODE NO. 3 UNDER PULSED AND CW CONDITIONS. THE 50-mW INPUT POWER IS AT 8.8 GHz. THE 10-Ω IMPEDANCE TRANSFORMER WAS USED.

a constant voltage supply. This is shown in Fig. 8.2 where the CW current-voltage relationship is shown for both zero RF power input and an input power of 50 mW at 8.8 GHz. In accordance with the theoretical result, the dc resistance of the diode increases under the large-signal condition and a decrease in current is observed above the threshold bias. Below the threshold, most of the crystal is biased in the linear range of the v-E characteristic and therefore nonlinear effects are negligible.

Figure 8.3 shows the CW current-voltage relationship for diode No. 1 under stable conditions. The 25-Ω impedance transformer was used. A decrease in current is again seen when 50 mW RF power is injected at 10 GHz. CW current-voltage relationships for diode Nos. 2 and 4 are shown in Fig. 8.4.

8.4 RF Characteristics of Stabilized TE Amplifiers

Figure 8.5 shows RF output power vs. frequency at different values of input power for diode No. 2. The approximate circuit configuration is also shown in the figure. The diode is biased at 9 V (dc). The corresponding power gain vs. frequency is shown in Fig. 8.6 for the same RF input power levels. Gain is observed over a frequency band more than 3.6 GHz wide as expected (e.g., Figs. 5.2 or 5.3). A slight decrease in gain with an increase in RF power over most of the frequency band is seen. No gain expansion is observed except at 11.4 and 11.6 GHz, because the signal strength is not small enough. This point will be discussed in greater detail later in this section.

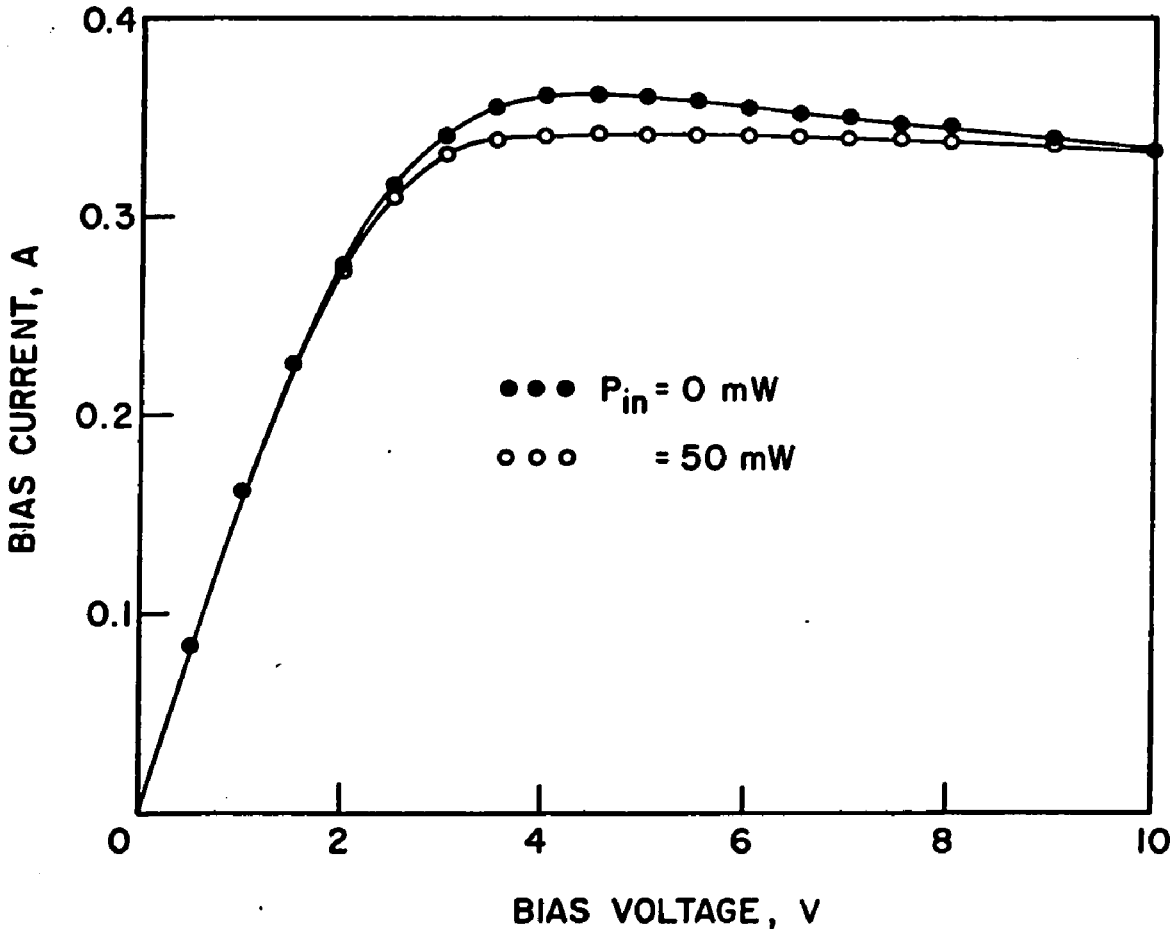


FIG. 8.3 CW CURRENT-VOLTAGE RELATIONSHIPS FOR DIODE NO. 1. THE 50-mW INPUT POWER IS AT 10 GHz. THE 25-Ω IMPEDANCE TRANSFORMER WAS USED.

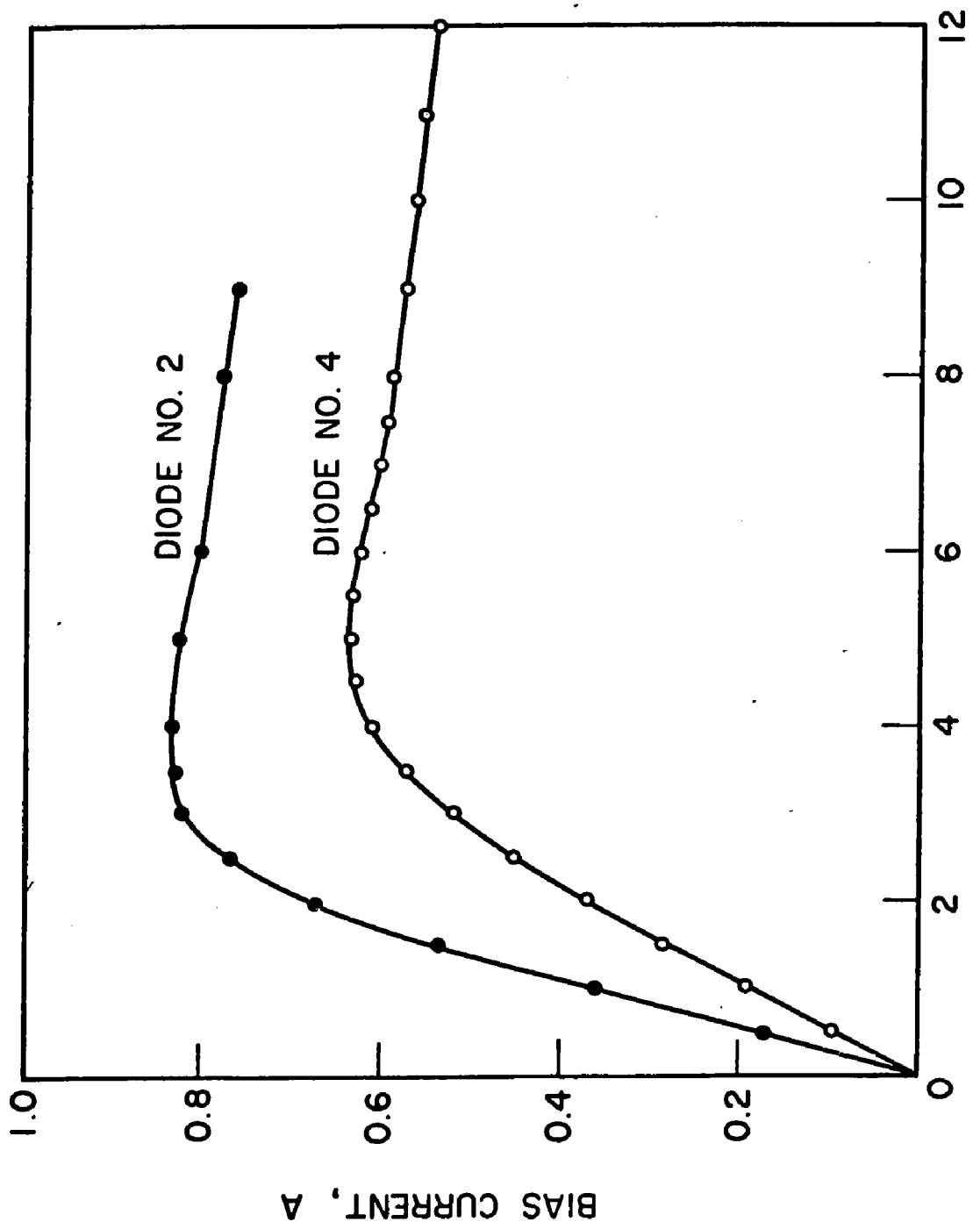


FIG. 8.4 CW CURRENT-VOLTAGE RELATIONSHIPS FOR DIODE NOS. 2 AND 4.

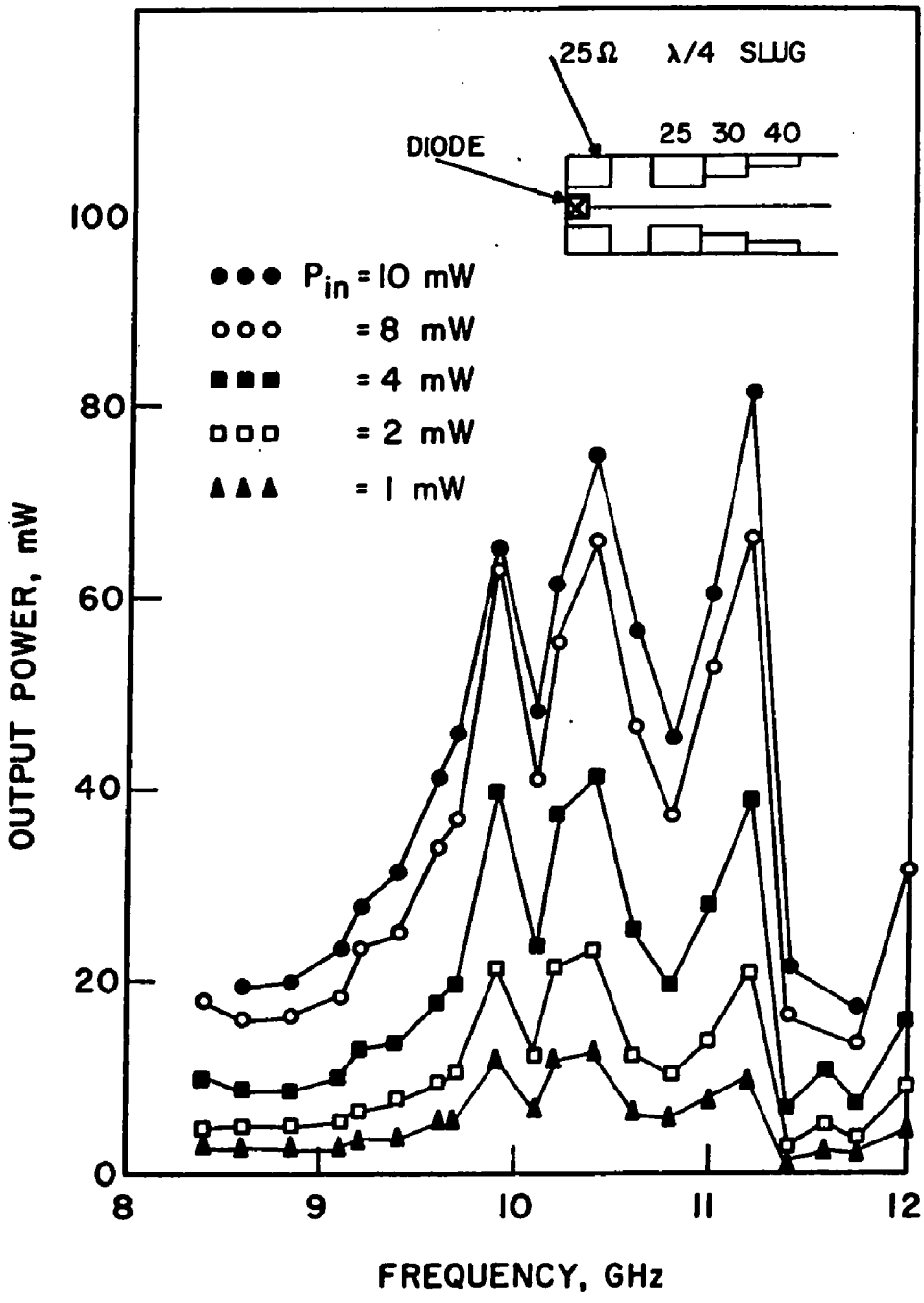


FIG. 8.5 OUTPUT POWER VS. FREQUENCY FOR DIODE NO. 2 FOR DIFFERENT INPUT POWERS. (BIAS VOLTAGE = 9 V)

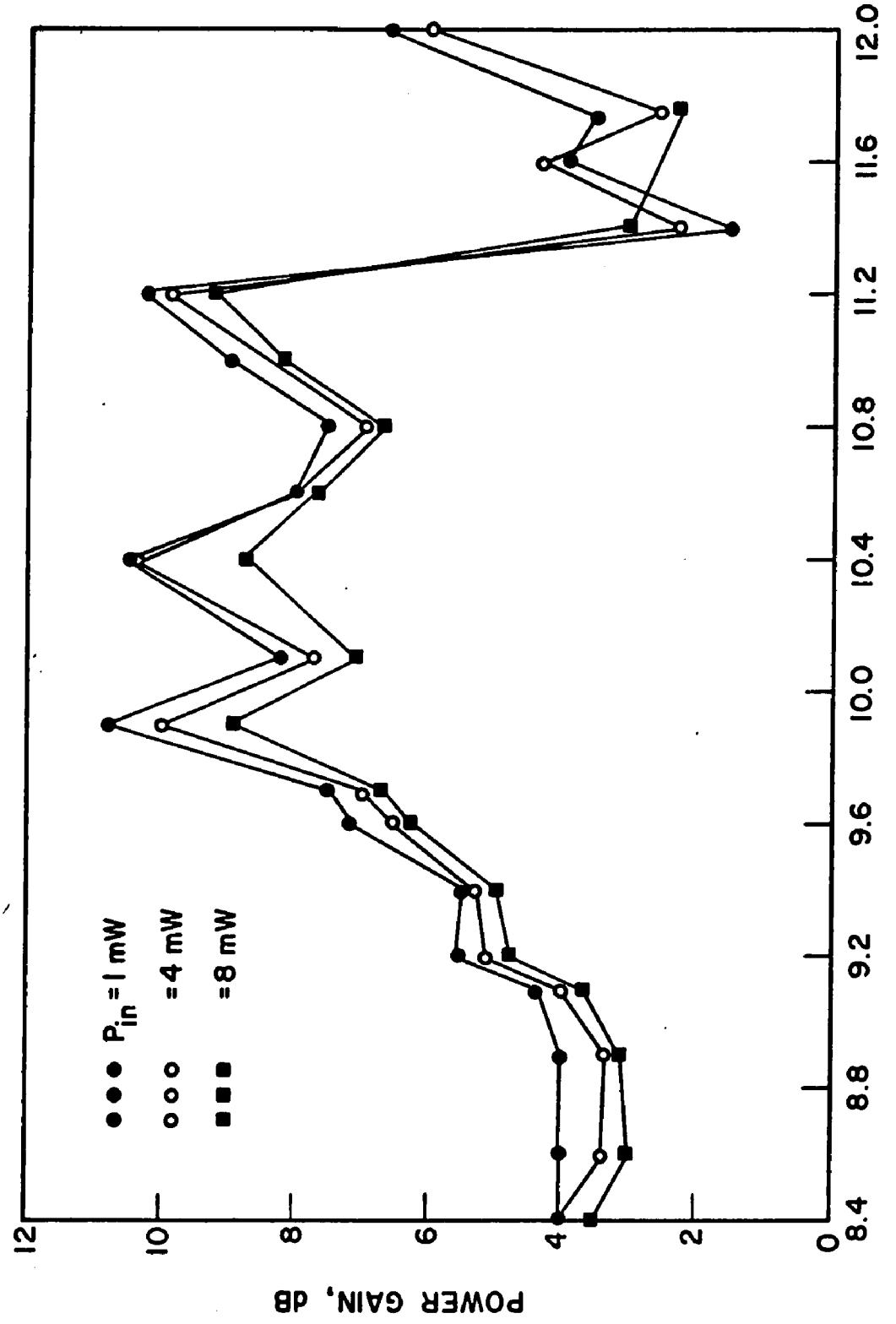


FIG. 8.6 POWER GAIN VS. FREQUENCY CORRESPONDING TO THE DATA OF FIG. 8.5.

Swept frequency measurements of output power as a function of frequency for an input power of approximately 3 mW are shown in Fig. 8.7 for diode No. 3. The 10-Ω impedance transformer was used to obtain gain around 10 dB at the bias levels between 8 and 9.5 V. The maximum gain is seen to increase with bias voltage. This is because at relatively low bias levels the negative resistance of the diode increases with bias voltage as shown in the theoretical results of Fig. 5.16a. When it is considered that the length of the crystal of diode No. 3 is 14 μm, gain occurs at somewhat high frequencies in Fig. 8.7. The transit-time frequency for a 14-μm device is approximately 7 GHz. However, theoretical calculations show that gain is expected at 10 GHz for relatively low bias voltages.

Figures 5.4a and 5.4b show that the frequencies of negative resistance decrease as the bias is increased. Such a dependence can be discerned in Fig. 8.7 but is more clearly seen by a comparison of Figs. 8.8 and 8.9 where output power is given as a function of frequency for a constant input power of 0.2 mW and at different bias voltages. The diode (No. 5) is of the same length and donor density as that of Fig. 8.7 (No. 3). The 10-Ω impedance transformer was used for the data of Fig. 8.8. At lower biases, the gain in the circuit was relatively low and a different circuit configuration (as indicated in Fig. 8.9) was used to obtain higher gain at bias voltages around 9 V. It may be recalled that the bandwidth of the 10-Ω impedance transformer is 5 GHz (i.e., 7.5 GHz to 12.5 GHz). Therefore the bandwidth of the amplifier of Fig. 8.8 is limited at the lower end by the circuit.

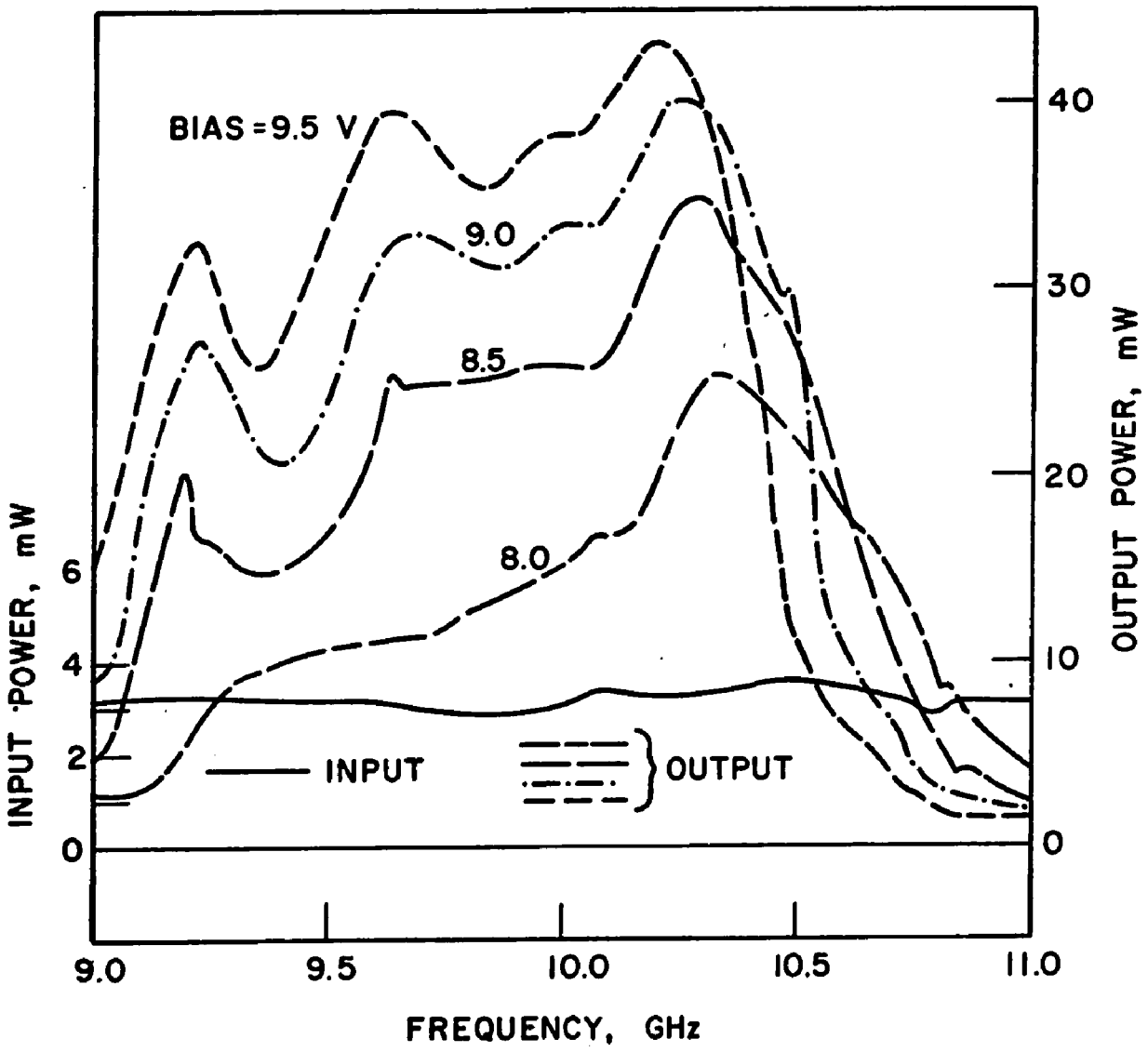


FIG. 8.7 SWEPT FREQUENCY MEASUREMENT OF OUTPUT POWER VS. FREQUENCY FOR DIFFERENT BIAS VOLTAGES. DIODE NO. 3 WITH THE 10-Ω IMPEDANCE TRANSFORMER PLACED AT THE DIODE END WAS USED.

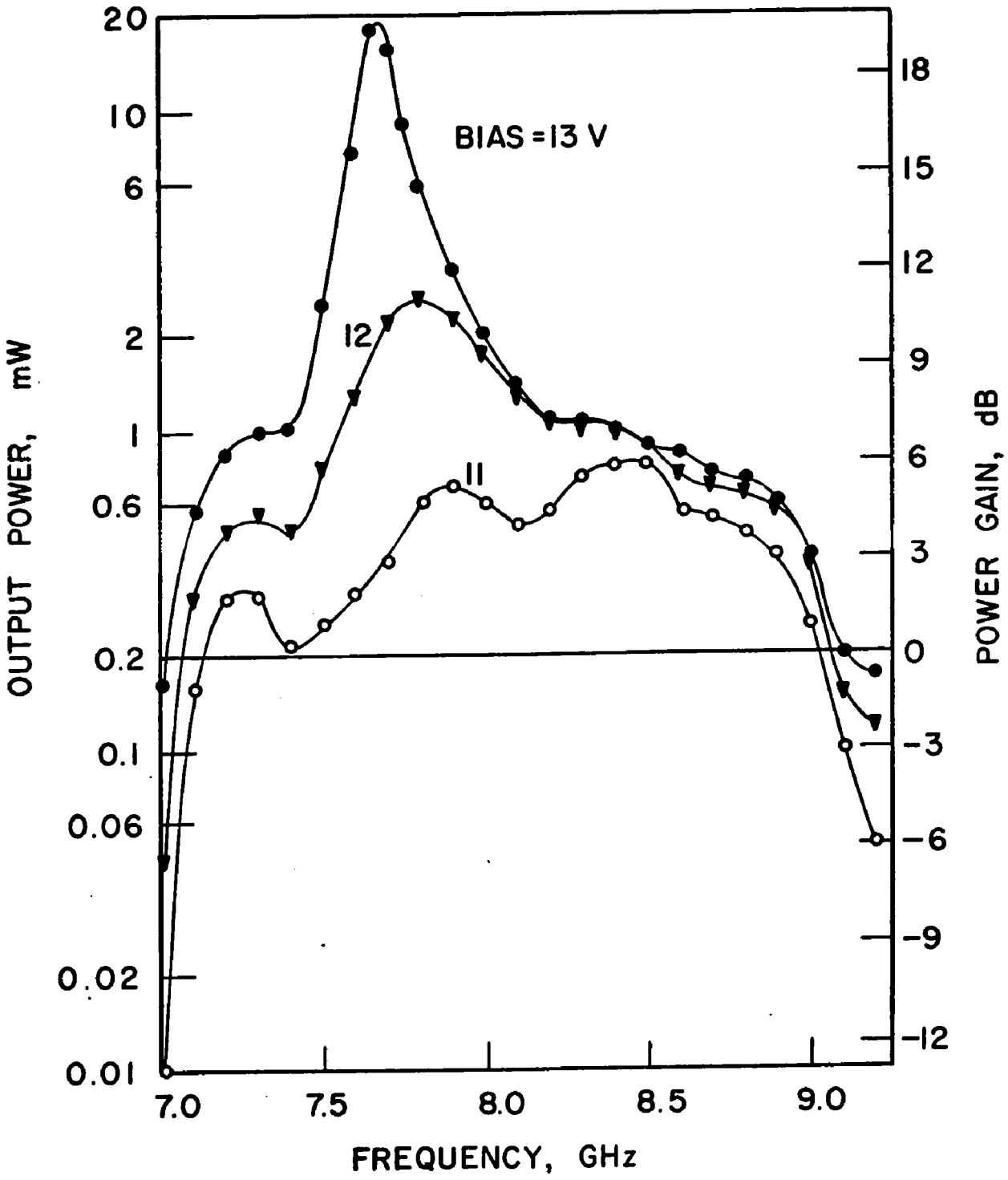


FIG. 8.8 OUTPUT POWER AND POWER GAIN VS. FREQUENCY FOR DIFFERENT BIAS VOLTAGES. DIODE NO. 5 WITH THE 10-Ω IMPEDANCE TRANSFORMER PLACED AT THE DIODE END WAS USED. (INPUT POWER = 0.2 mW)

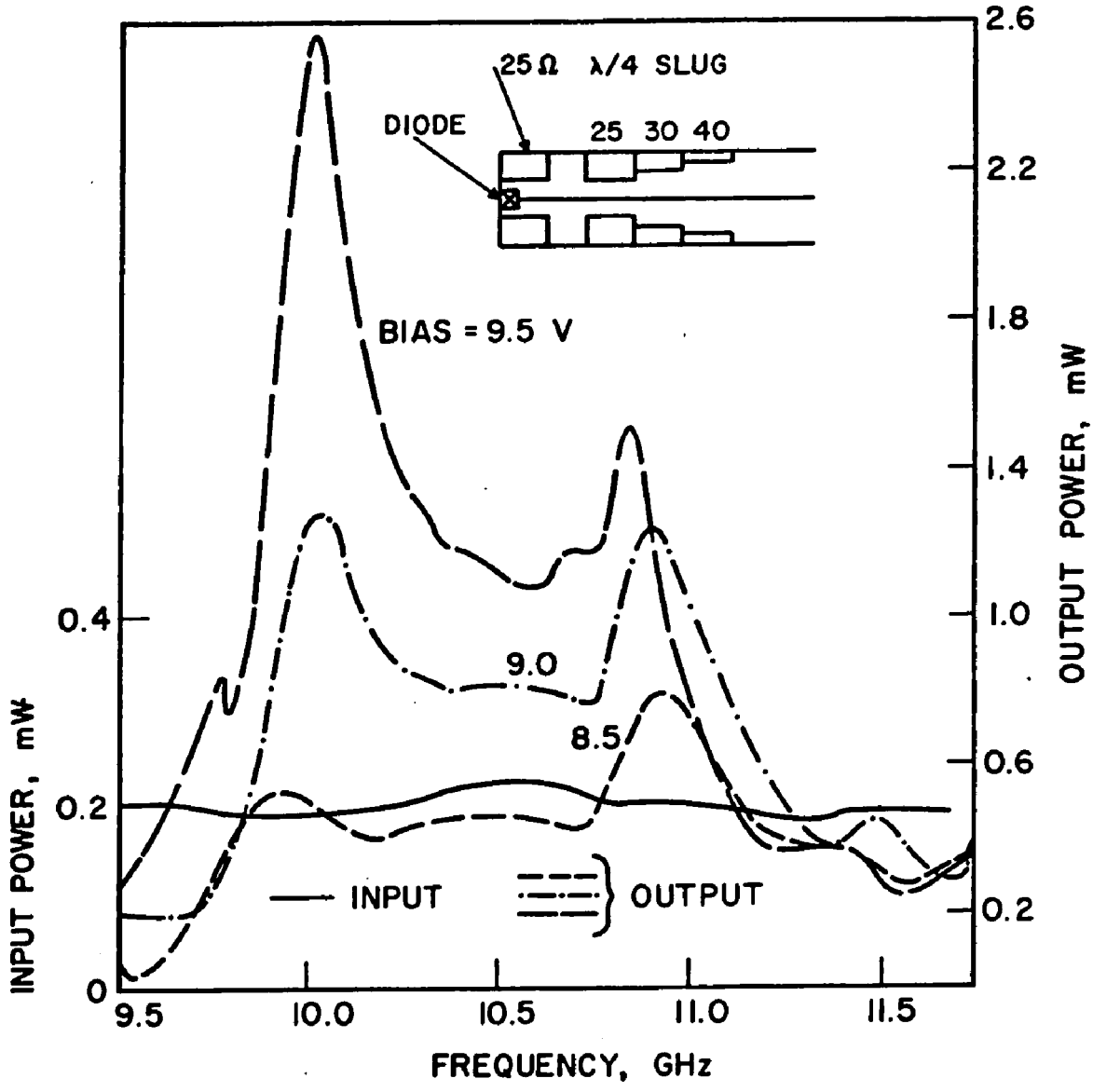


FIG. 8.9 SWEPT FREQUENCY MEASUREMENT OF OUTPUT POWER VS. FREQUENCY FOR DIODE NO. 5.

In addition to the circuit, the diode lead inductance and the package capacitance also affect the bandwidth of the amplifier. The magnitude of the reactance of these elements is of the same order as the diode negative resistance and reactance. Thus the elements can introduce resonances within the frequency range of interest. For example, the lead inductance resonates in series with the device capacitance. At a higher frequency, the package capacitance resonates in parallel with the net inductance of the series combination of the crystal and the lead. At this frequency the diode acts as a pure negative resistance and the gain is maximum near this frequency. In general these resonances decrease the $G^{1/2}$ B product (G = maximum power gain, B = 3 dB bandwidth) of these amplifiers. These effects are illustrated in Fig. 8.10 where small-signal power gain is shown as a function of frequency for the diode and operating conditions of Fig. 5.3 and assuming a series load resistance of 50 Ω. Curve I was calculated by neglecting the lead inductance and package capacitance. Curve II was obtained by including the effect of typical values of these elements. The packaged diode acts as a pure negative resistance at a frequency slightly above 12 GHz. As stated previously, the maximum gain occurs near this frequency. The $G^{1/2}$ B product for curve I is 9.5 GHz and for curve II it is 7.75 GHz. In practice, additional circuit capacitance may exist at the end of the coaxial line where the diode is mounted and the $G^{1/2}$ B product may be reduced further.

The $G^{1/2}$ B product for the data of Fig. 8.6 is approximately 5.4 GHz. In Fig. 8.7 it is approximately 5.2 GHz. It was much less when a

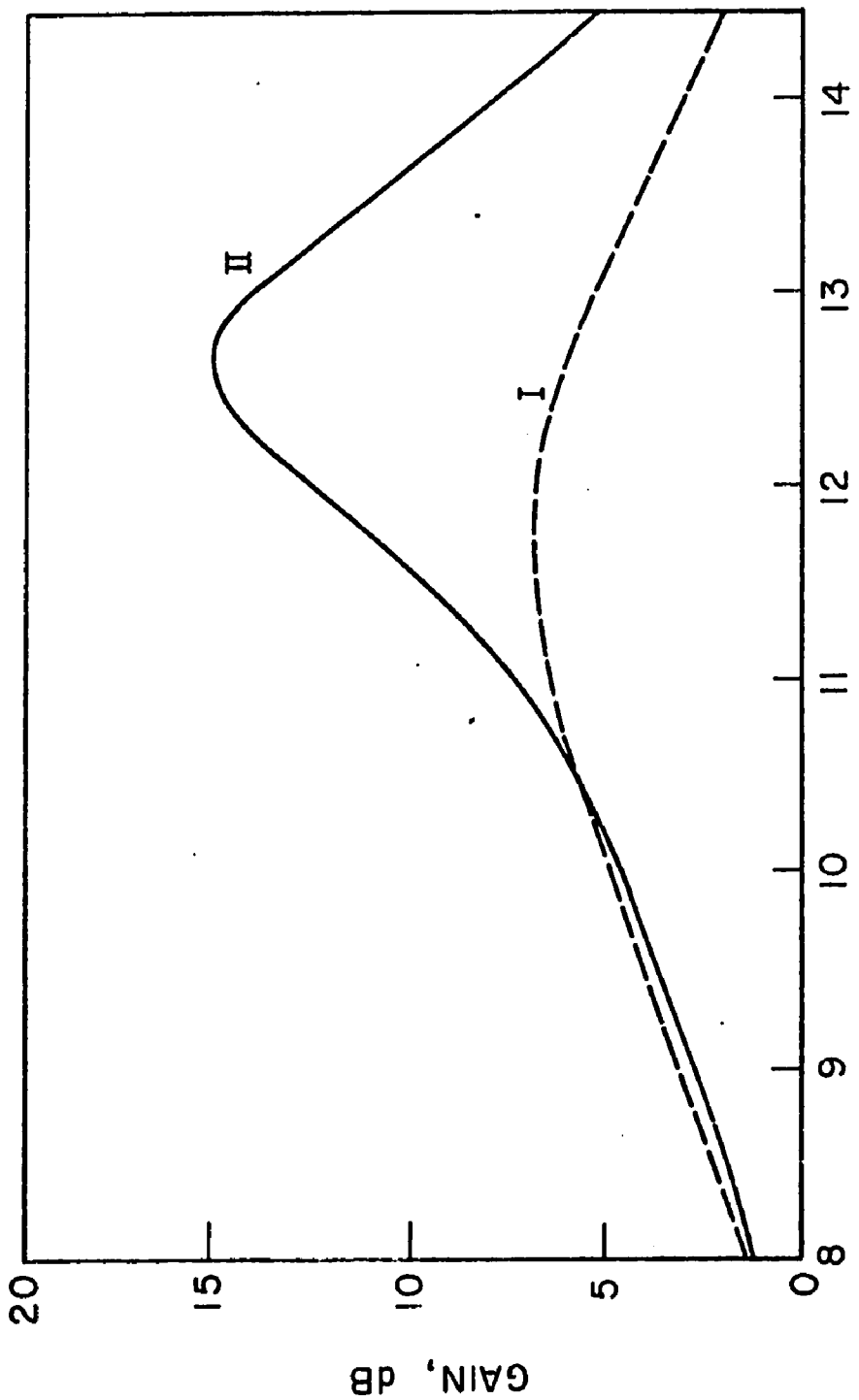


FIG. 8.10 SMALL-SIGNAL POWER GAIN FOR THE DIODE AND OPERATING CONDITIONS OF FIG. 5.3. A SERIES LOAD RESISTANCE OF 50 Ω WAS ASSUMED. CURVE II INCLUDES PACKAGING PARAMETERS (LEAD INDUCTANCE = 0.46 nH, PACKAGE CAPACITANCE = 0.26 pF). CURVE I OMITS THEM.

single slug was used for tuning. Figure 8.11 shows gain vs. frequency at two different input power levels for diode No. 5. A single slug of characteristic impedance 16.3 Ω was used and its position adjusted to obtain large gain near 7.3 GHz as shown in the figure. The bias was 14.7 V and the dc current was 0.39 A. The $G^{1/2}$ B product for both of the curves is approximately 1.4 GHz. Similar observations for diode No. 3 using a 30-Ω slug gave a $G^{1/2}$ B product of 2.37 GHz as shown in Fig. 8.12. The bias voltage and current were 9.5 V and 0.71 A, respectively. Perlman et al.[46] have obtained $G^{1/2}$ B products of 8 GHz and above by the use of microstrip circuits and equalizing networks.

The shift in the center frequency of negative resistance when the bias is changed from 11 V (Fig. 8.8) to 9 V (Fig. 8.9) is approximately 2 GHz. In Fig. 8.9 the frequency of maximum gain decreases by approximately 1 GHz when the bias is increased from 8.5 to 9.5 V. These changes are large compared to those of Fig. 5.4a where an increase of bias from 11 V to 13 V decreases the frequency of maximum negative resistance by approximately 1 GHz (i.e., approximately 0.5 GHz/V). However, Fig. 5.4a is for a constant lattice temperature whereas the lattice temperature increases with bias in the CW experiments of Figs. 8.8 and 8.9. Thus the relatively large change in frequency of operation in Figs. 8.8 and 8.9 must be attributed to a rise in lattice temperature apart from the effect of bias under constant temperature conditions. The effect of lattice temperature on frequency of operation was discussed theoretically in Section 6.4.

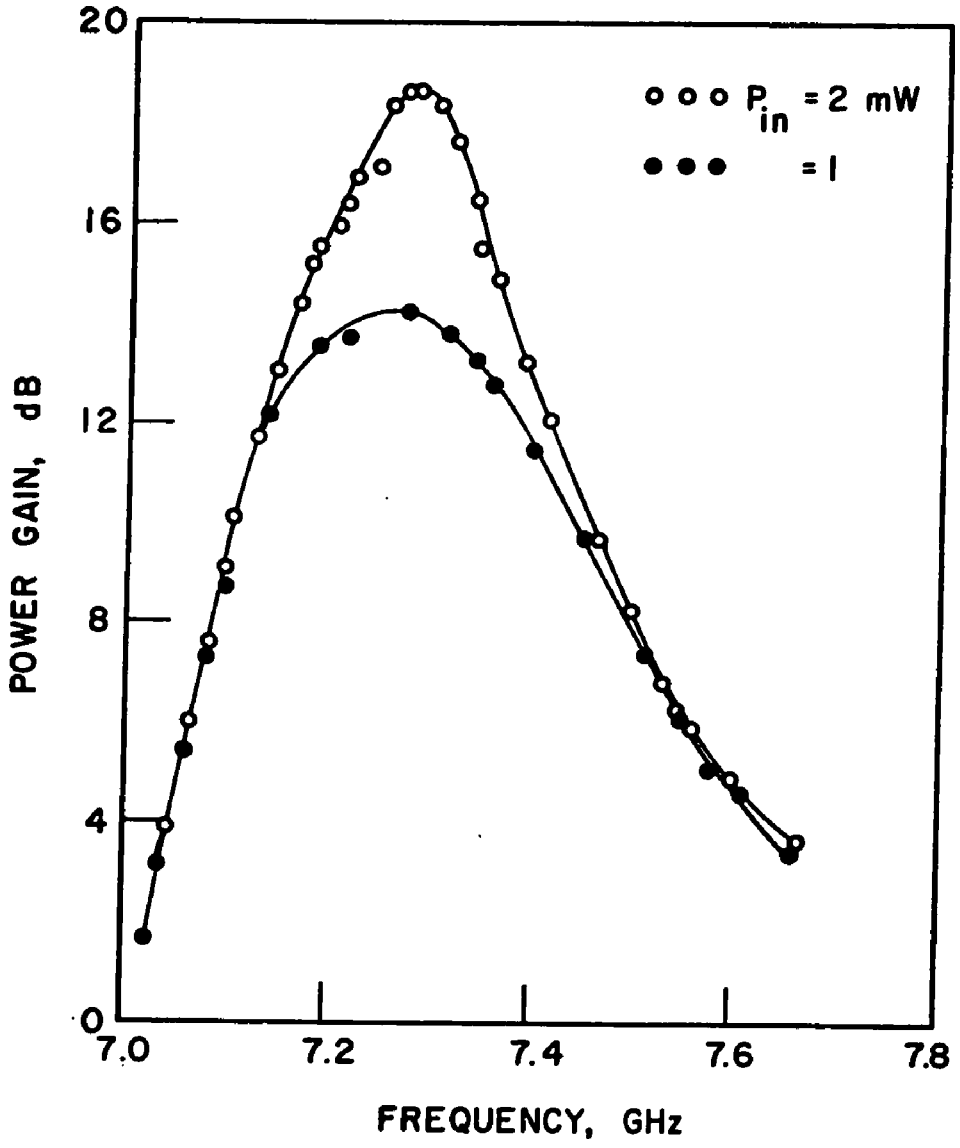


FIG. 8.11 POWER GAIN VS. FREQUENCY FOR DIODE NO. 5 WITH A $\lambda/4$ SLUG OF CHARACTERISTIC IMPEDANCE 16.3 Ω PLACED AWAY FROM IT. (BIAS VOLTAGE = 14.7 V)

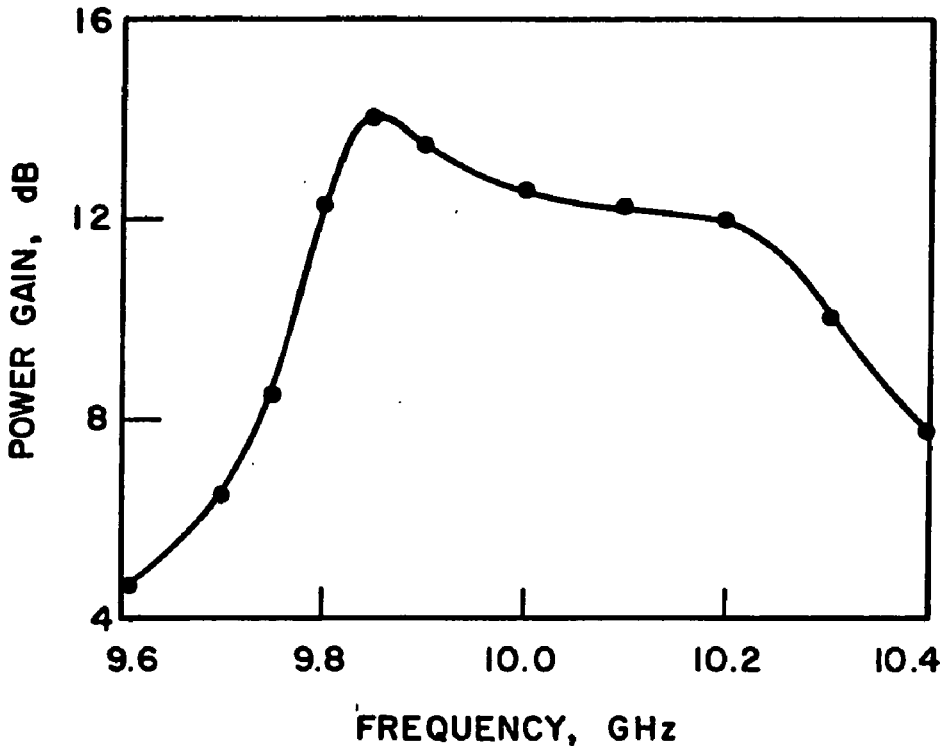


FIG. 8.12 POWER GAIN VS. FREQUENCY FOR DIODE NO. 3 WITH A $\lambda/4$ SLUG OF CHARACTERISTIC IMPEDANCE 30 Ω PLACED AWAY FROM IT. (INPUT POWER = 1 mW, BIAS VOLTAGE = 9.5 V)

It was shown in Chapters V and VI (e.g., Figs. 5.16a and 6.13) that for a constant RF current, the magnitude of the negative resistance at first increases and then decreases as the bias is increased above the threshold value. Similar experimental results are shown for diode Nos. 2 and 1 in Figs. 8.13 and 8.14, respectively, where power gain is plotted as a function of bias voltage for constant RF input power levels. In Fig. 8.13 the signal frequency is 9.23 GHz. A 10-Ω slug was placed at the diode end of the coaxial line. In Fig. 8.14 the signal frequency was 9.75 GHz and the 25-Ω impedance transformer was used at the diode end of the line. As expected from the theoretical curves of Figs. 5.16a and 6.13, the minimum bias voltage at which gain is observed increases with signal strength. Also, in accordance with the theoretical results, the higher the signal power, the greater is the bias voltage at which maximum gain occurs.

The values of dc to RF conversion efficiency corresponding to the data of Fig. 8.13 are shown in Fig. 8.15. The maximum efficiency of approximately 2 percent is observed for an input power of 50 mW when the gain is approximately 3 dB. This value is of the same order as that calculated in Figs. 6.12 and 6.14.

It was shown in Figs. 3.8 and 5.18a that negative resistance increases as the RF signal is increased from a small value, reaches a maximum, and then decreases at large signals. This can also be observed in the experimental data of Fig. 8.14 at bias voltages above 8 V. The gain expansion occurs at higher RF power input for larger values of bias voltage. This is shown more clearly in Fig. 8.16 for diode No. 1, where

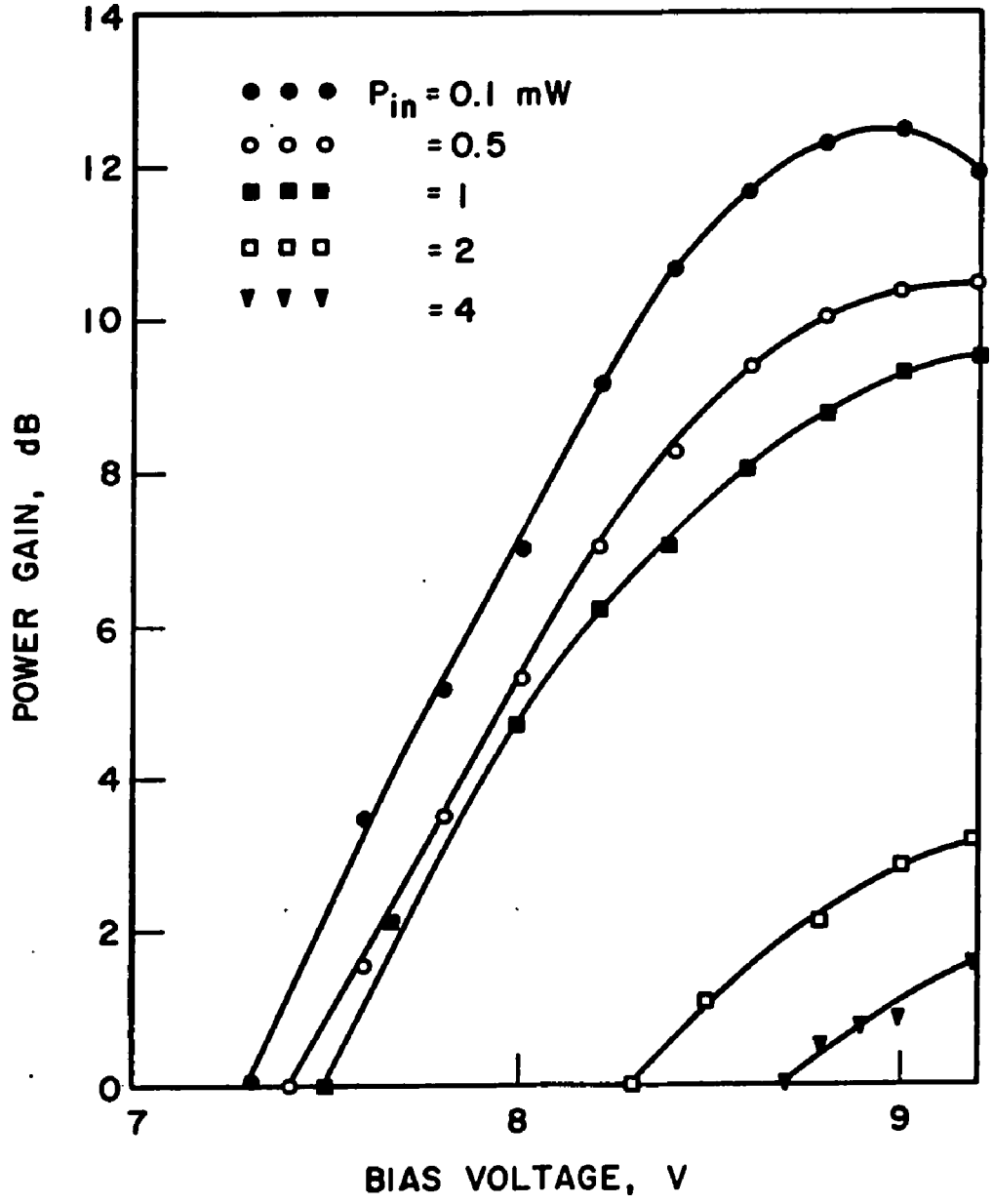


FIG. 8.13 POWER GAIN VS. BIAS VOLTAGE FOR DIODE NO. 2 WITH A $\lambda/4$ SLUG OF CHARACTERISTIC IMPEDANCE 10 Ω PLACED AT THE DIODE END OF THE 50-Ω TRANSMISSION LINE. (FREQUENCY = 9.23 GHz)

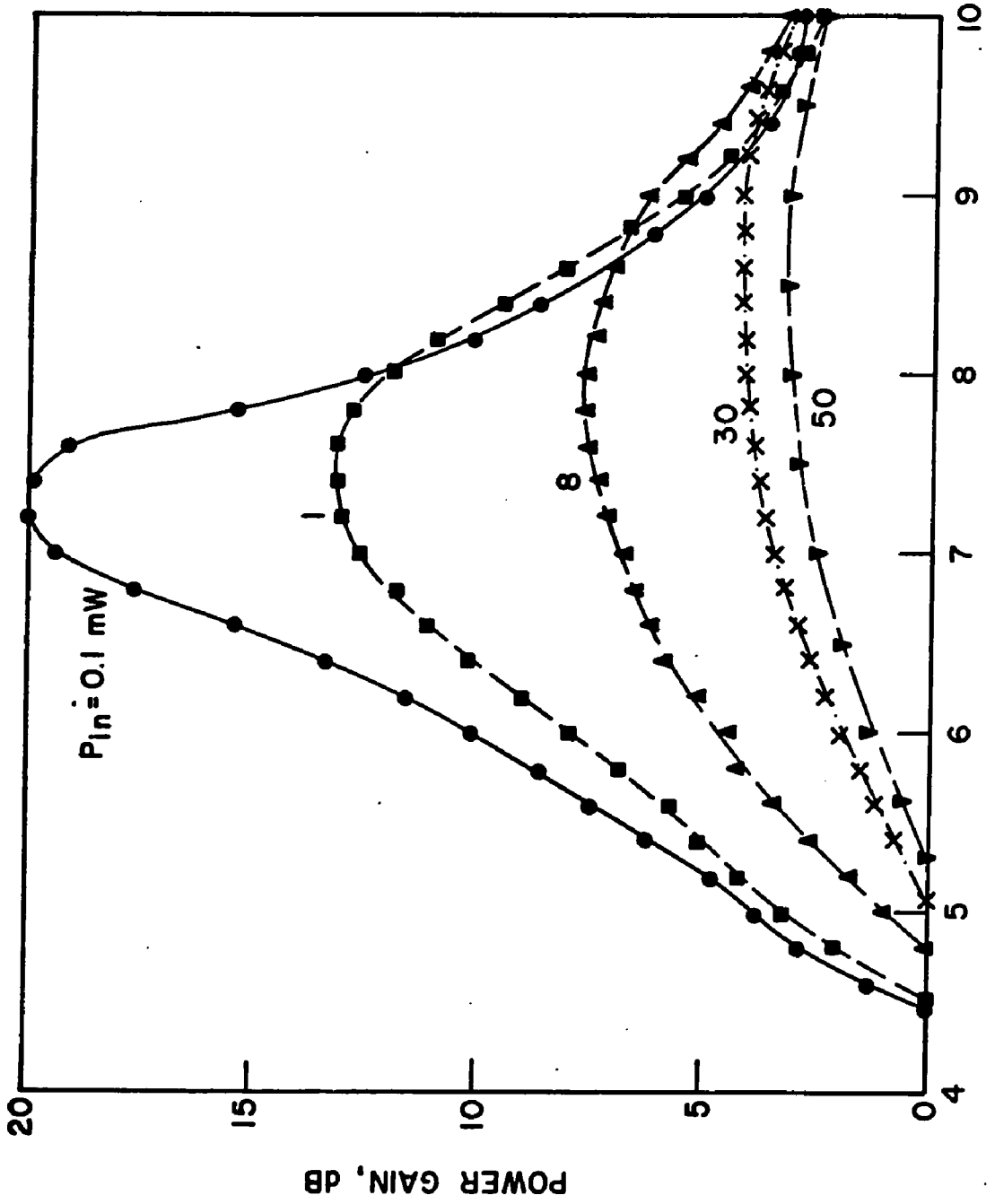


FIG. 8.14 POWER GAIN VS. BIAS VOLTAGE FOR DIODE NO. 1. THE 25-Ω IMPEDANCE TRANSFORMER WAS USED. (FREQUENCY = 9.75 GHz)

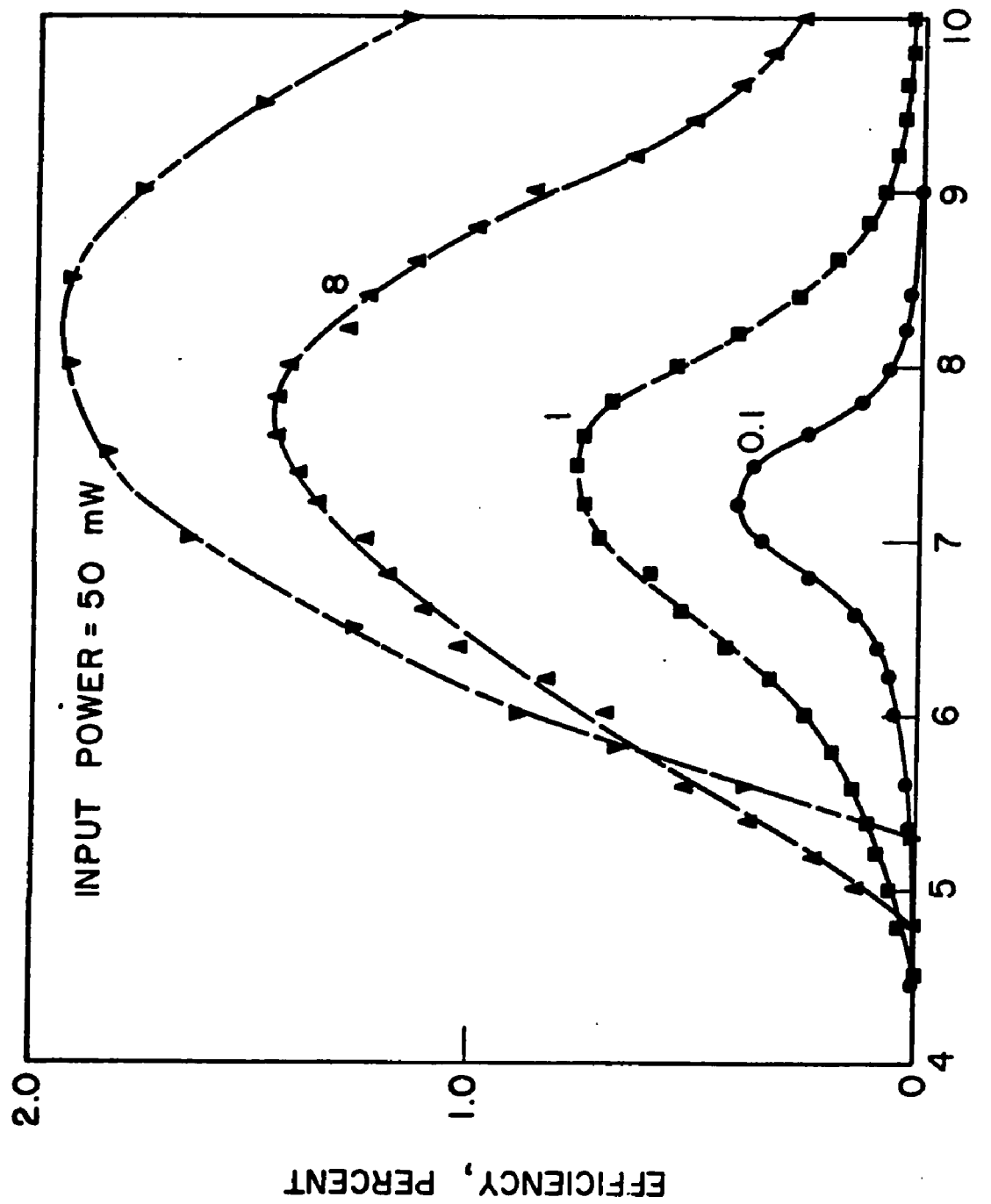


FIG. 8.15 Dc TO RF CONVERSION EFFICIENCY CORRESPONDING TO THE DATA OF FIG. 8.13.

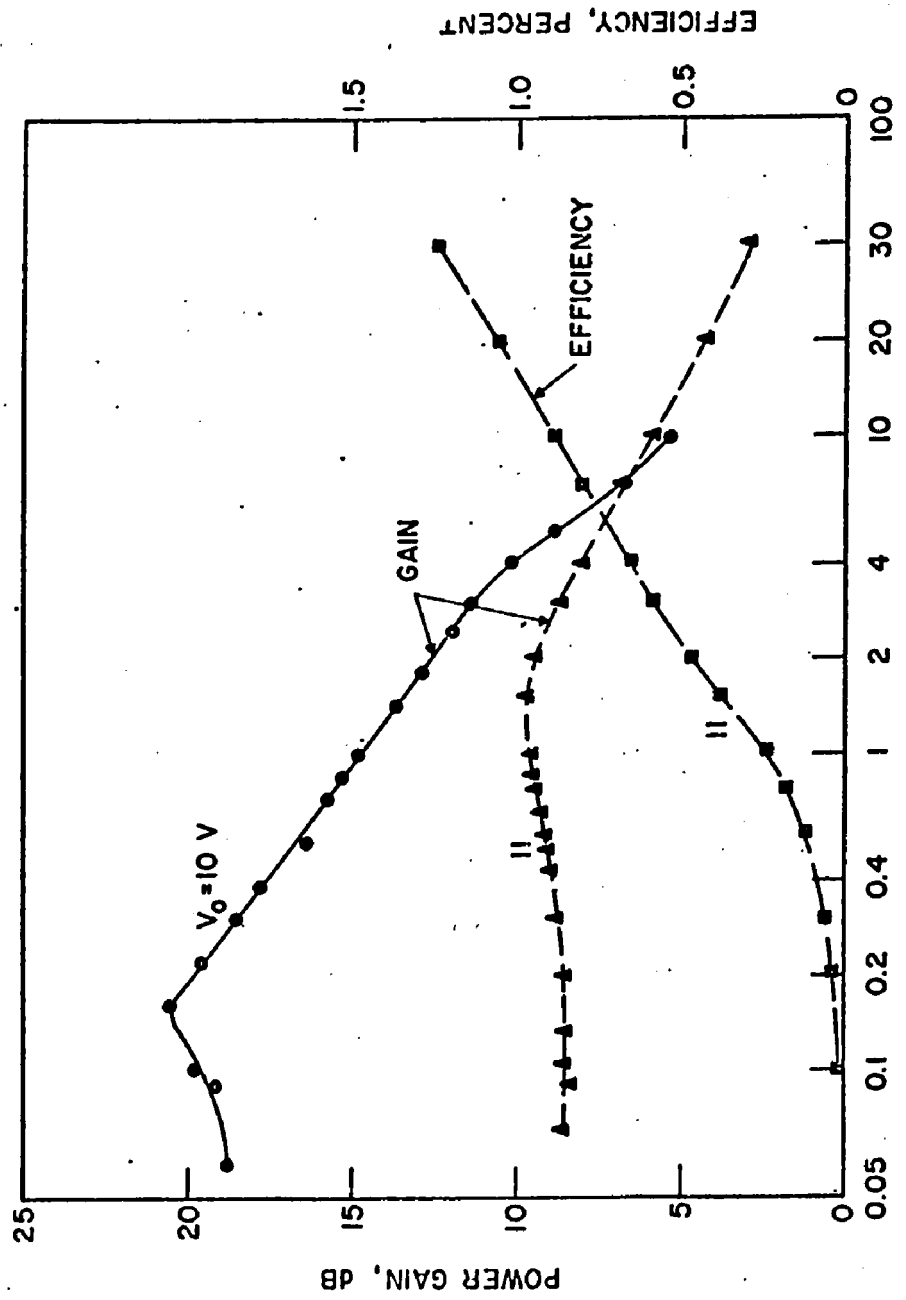


FIG. 8.16 POWER GAIN AND EFFICIENCY VS. INPUT POWER FOR DIODE NO. 1 WITH A $\lambda/4$ SLUG OF CHARACTERISTIC IMPEDANCE 25 Ω PLACED AWAY FROM IT. (FREQUENCY = 9.75 GHz)

power gain is plotted as a function of input RF power for different bias voltage values. A single slug having a characteristic impedance of 25 Ω was used to obtain a maximum gain of approximately 20 dB at 10 V bias. The gain decreases at a higher bias of 11 V but gain expansion occurs at a higher RF power level as expected from the theoretical results of Fig. 5.18a. The dc to RF conversion efficiency is also shown for the 11 V bias case. The results of this figure are qualitatively similar to those of Fig. 3.8.

Figure 8.17 shows similar data for diode No. 4. Here gain is plotted on a linear scale so that gain expansion can be more easily observed. The signal frequency is 9.42 GHz. A single slug of 40-Ω characteristic impedance was used. As expected, the gain increases with bias voltage for relatively low biases and decreases when the bias is high. It was stated in Section 5.3 that when the bias voltage is small and the difference between the magnitude of diode negative resistance and circuit resistance is large (so that gain is small) gain expansion may not be easily observable. This is the case at a bias of 8 V in Fig. 8.17. At higher bias voltages gain expansion can be clearly seen. When the difference between the magnitude of diode negative resistance and circuit resistance is small, the gain is large and is sensitive to change in the value of negative resistance. Such a situation occurs at a bias of 10 V where gain expansion is substantial. Again, as predicted in Fig. 5.18a, gain expansion occurs at higher RF input power levels for higher bias voltages.

In general, the nonlinearity of the amplifier is higher at higher gains. Another example of such behavior is shown in Fig. 8.18 where

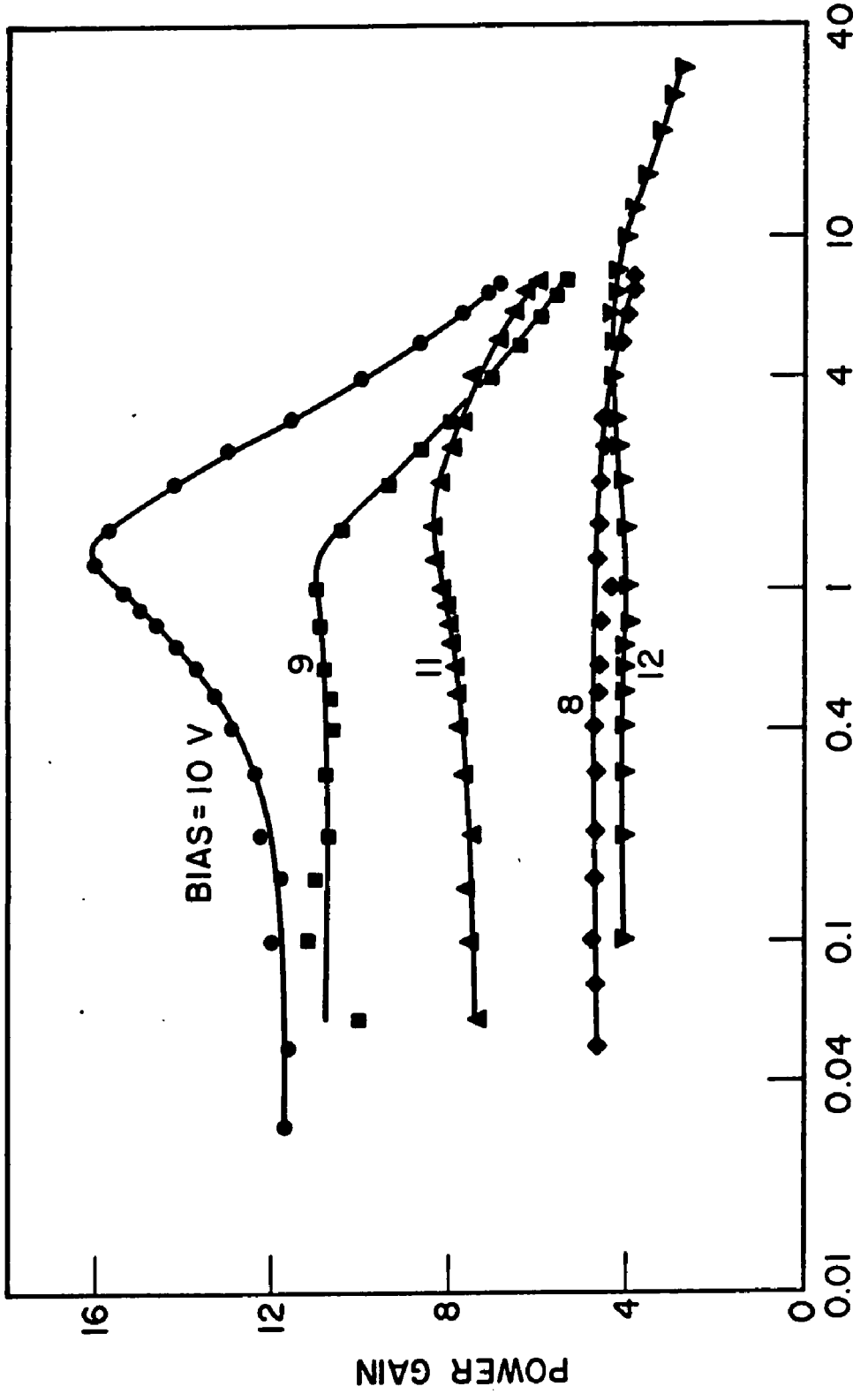


FIG. 8.17 POWER GAIN VS. INPUT POWER FOR DIFFERENT BIAS VOLTAGES. DIODE NO. 4 WITH A $\lambda/4$ SLUG OF CHARACTERISTIC IMPEDANCE 40 Ω PLACED AWAY FROM IT WAS USED. (FREQUENCY = 9.42 GHz)

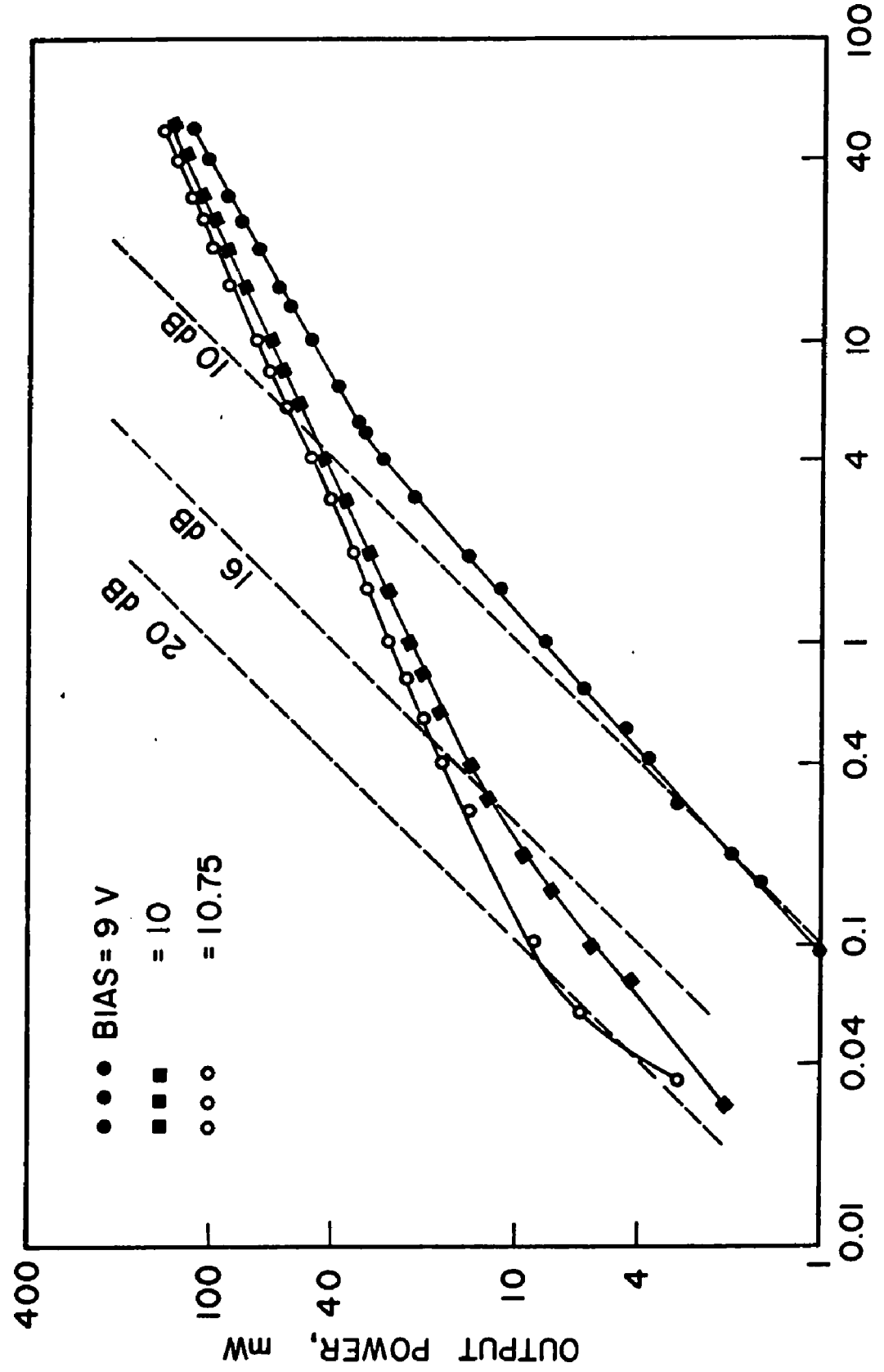


FIG. 8.18 OUTPUT POWER VS. INPUT POWER FOR DIODE NO. 3. THE 25-Ω IMPEDANCE TRANSFORMER WAS USED. (FREQUENCY = 8.8 GHz)

RF power output is shown as a function of input power for diode No. 3. The 25-Ω impedance transformer was used. The signal frequency was 8.8 GHz. Gain as well as nonlinearity increase with bias voltage.

When the bias voltage is constant, the linearity of the amplifier depends on the circuit impedance at the signal frequency. For example in Fig. 8.11, the gain is the same for both input power levels of 0.2 mW and 1 mW at frequencies below 7.14 GHz. But at the frequency of maximum gain strong gain compression occurs. The same diode operated in a different circuit showed fairly linear behavior at 7.8 GHz (Fig. 8.19). The 10-Ω impedance transformer was used.

8.5 Summary

A comparison of some of the important theoretical results of the large-signal analysis of Chapter II with experimental observations has been presented. Good qualitative agreement has been found between the theory and experiment. In particular the following results have been shown:

1. The bias current decreases as a result of lattice heating. The current also decreases when a large signal is injected into a stabilized TE device biased with a constant voltage supply.

2. Gain (or negative conductance) over frequency bandwidths greater than 3.6 GHz at X-band is observed. $G^{1/2}$ B products of greater than 5 GHz can be obtained when the diode is mounted in a wideband circuit with constant resistance.

3. The frequency at which maximum gain is obtained decreases when the bias is increased (for a fixed circuit) as well as when the lattice temperature increases.

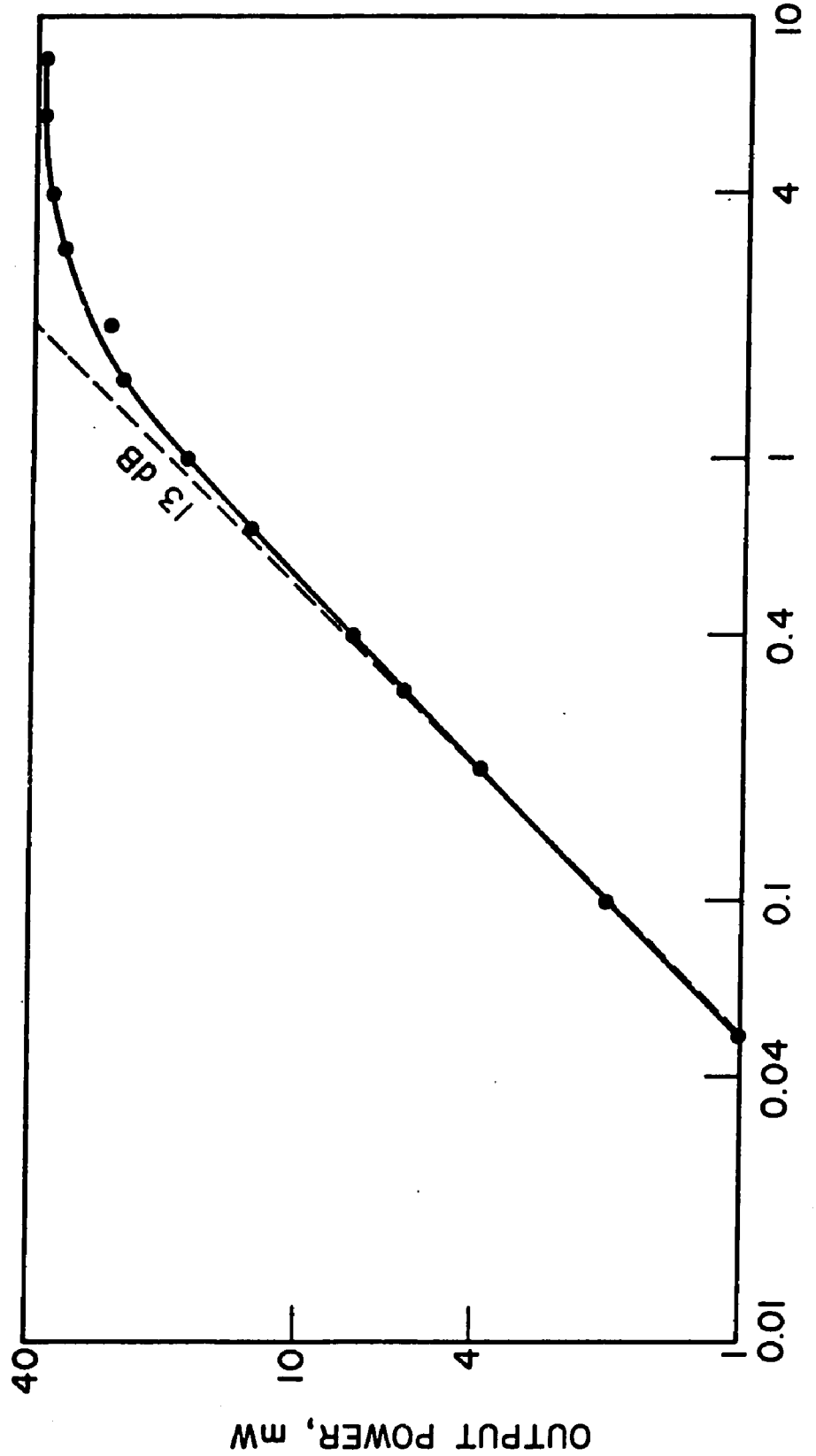


FIG. 8.19 OUTPUT POWER VS. INPUT POWER FOR DIODE NO. 5. THE 10-Ω IMPEDANCE TRANSFORMER WAS USED. (FREQUENCY = 7.8 GHz, BIAS = 12.5 V)

4. Gain increases with the bias voltage at relatively low bias values; it decreases when the bias is high, and it has a maximum value for a certain bias voltage. The higher the RF input power, the higher is the voltage at which the maximum gain occurs.

5. The minimum bias voltage at which the device exhibits gain increases with the input signal power.

6. The amplifier gain at first increases (gain expansion) and then decreases (gain compression) as the RF signal power is increased from a small value. The higher the bias voltage, the higher is the RF power at which the maximum in gain occurs.

CHAPTER IX. A MODEL FOR THE DELAYED-DOMAIN MODE OF TRANSFERRED-ELECTRON DEVICES

9.1 Introduction

Hines and Buntschuh[20] have discussed microwave amplification by injection locking. In order to understand and assess the potential of the delayed-domain mode for large-signal amplification by injection locking, an analytical model for the mode was developed. The model, and some numerical calculations based on it, are presented in this chapter. A brief description of the delayed-domain mode is given in Section 9.2.

Detailed knowledge of the domain collection process is essential for quantitative study of the delayed-domain mode. An analysis of this process is presented in Section 9.3. Previously, McCumber and Chynoweth[26] calculated the current through a GaAs device during domain collection by solving the basic transport equations on a computer. However, this gives little physical insight into the domain collection process. Heinle[86] simplified the starting equations by neglecting diffusion and relaxation effects and obtained general equations for domain dynamics. Robrock[87] treated the problem of domain collection by postulating the existence of an "apparent" domain which maintains the stable-domain shape while passing across an ideal anode boundary. In the study given here, equations for the domain collection process were written directly from physical considerations and the electric field configuration within the crystal was calculated as a function of time. From this, the current waveform during domain collection can be obtained for a given voltage across the diode.

The analysis of the domain collection process was combined with the model for the quenched-domain mode given by Khandelwal[83] in order to study the delayed-domain mode. This is presented in Section 9.4. Current waveforms for a diode biased with a dc and an RF voltage across it were determined. These current waveforms were then Fourier analyzed to obtain the dc and fundamental components. From these the dc to RF conversion efficiency was determined. Calculations were also made for a voltage waveform with a second harmonic as suggested by Kino and Kuru[88] for high-efficiency operation. The results of these calculations are also presented in Section 9.4 along with the effects of variation of dc bias, first- and second-harmonic voltage magnitudes and their relative phases.

9.2 A Description of the Delayed-Domain Mode

Consider a GaAs diode with a dc bias greater than the threshold value across it and an RF voltage such that the total voltage across the diode goes below the threshold voltage during part of the cycle. As the instantaneous voltage reaches the threshold, a domain nucleates near the cathode. This domain grows and travels toward the anode. If the voltage across the diode stays above the sustaining voltage until the domain has been collected at the anode and if it is below the threshold voltage at the moment the domain has been fully collected, no new domain is nucleated at the cathode until the voltage comes up to the threshold value. Thus there is a time lag between the collection of one domain and the nucleation of a new domain. Such an operation corresponds to frequencies below the transit-time frequency and is called the delayed-domain mode of operation.

If the voltage falls below the sustaining voltage during domain collection then the domain is quenched, since the quenching process is faster than the process of collection. The time constant for quenching being of the order of a few picoseconds[83] while the time for collection of a domain is of the order of a few tens of picoseconds. After the quenching, the formation of a new domain may be delayed because the frequency is below the transit-time frequency. If however, the voltage goes below the sustaining voltage after the domain has been collected, then the mode may be called a delayed-domain mode.

9.3 The Domain Collection Process

Initially, diffusion effects are neglected for simplicity. When this is done, the depletion layer of the domain is fully depleted of the charge carriers and the accumulation layer is of negligible width.[89] The electric field configuration of a domain in transit is then a right-angled triangle. Consider such a domain in the process of being collected. Let E_1 be the field outside the domain, E_2 the peak field in the domain and E_3 the field near the anode as indicated in Fig. 9.1 (which is not drawn to scale). Since the cathode and anode contacts are usually good conductors, the electric field at the cathode and anode boundaries falls to zero, requiring overall charge neutrality.

Because the thickness of the accumulation layer is negligible when carrier diffusion and thermal currents are neglected,[89] the time for collection of the accumulation layer is very small and the analysis will be confined initially to the period during which the depletion region is

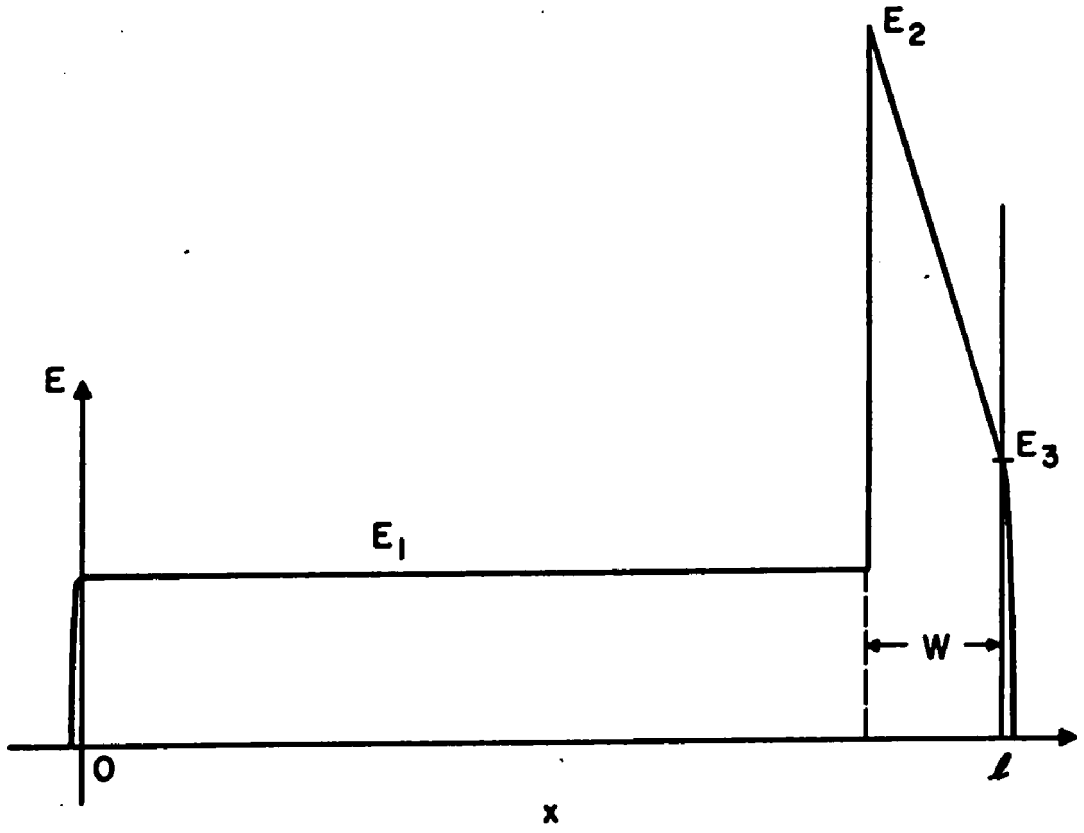


FIG. 9.1 ELECTRIC FIELD CONFIGURATION IN A GUNN DIODE DURING DOMAIN COLLECTION. THE FIGURE IS NOT DRAWN TO SCALE.

collected. Since the depletion region of the domain is fully depleted, there is no conduction current at the anode during the time that the depletion layer is collected. The current at the anode during this period consists of displacement current only.

The current near the cathode has both conduction and displacement components. As the domain is collected E_1 must approach E_{th}. As E_1 reaches E_{th} a new domain starts being nucleated in the case of the transit-time mode. In the case of the delayed-domain mode E_1 does not reach E_{th} until shortly after the domain has been fully collected. The analysis given in this section is confined to the period when E_1 is less than E_{th}.

A velocity-field characteristic of the following form is assumed:

$$v = \mu_o E \quad ; \quad E \leq E_{th}$$

$$v = B_a + \frac{B_b}{E} + B_c E + \frac{B_d}{E^2} \quad ; \quad E_{th} < E \leq 50 \text{ kV/cm}$$

$$v = 1.1 \times 10^7 \text{ cm/s} \quad ; \quad E > 50 \text{ kV/cm} \quad . \qquad (9.1)$$

Here v is the average carrier (electron) velocity, E is the electric field and μ_o is the mobility of the GaAs material at low electric fields. With proper values of the constants B_a, B_b, B_c and B_d, the characteristic can be shown[90] to be in close agreement with that given by Butcher and Fawcett.[76]

By the condition of continuity of current, the currents at $x = 0$ and $x = \ell$ must be equal, i.e.,

$$\epsilon \frac{dE_1}{dt} + n_o e \mu_o E_1 = \epsilon \frac{dE_3}{dt} , \qquad (9.2)$$

where ϵ = the permittivity of GaAs,

n_o = the ionized donor density of the GaAs material and

e = the magnitude of electronic charge.

If W_D is the width of the depletion layer, then by Poisson's equation,

$$\frac{E_2 - E_3}{W_D} = \frac{n_o e}{\epsilon} , \qquad (9.3)$$

where n_o is the ionized donor density which is considered to be uniform along the length of the diode.

If E_2 were to remain constant during domain collection, then the time rate of change of E_3 would be given by

$$\left.\frac{dE_3}{dt}\right|_{E_2 = \text{constant}} = \frac{E_2 - E_3}{W_D} v_A = \frac{n_o e v_A}{\epsilon} , \qquad (9.4)$$

where v_A is the velocity at which the accumulation layer moves. The value of W_D has been substituted in Eq. 9.4 from Eq. 9.3. If, however, E_2 also changes, the total time rate of change of E_3 can be written as

$$\frac{dE_3}{dt} = \frac{dE_2}{dt} + \frac{n_o e v_A}{\epsilon} . \qquad (9.5)$$

Equation 9.5 may also be obtained from Eq. 9.1 and by considering the amount of charge in the accumulation layer.

The field difference $E_2 - E_1$ changes if the total charge in the accumulation layer changes. This occurs if the velocity of the domain (peak of the domain field configuration) is different from the velocity of carriers outside the domain. The time rate of change of $E_2 - E_1$ can be written in terms of the velocity difference as

$$\epsilon \frac{d(E_2 - E_1)}{dt} = (\mu_o E_1 - v_A)\, n_o e \quad . \tag{9.6}$$

It is noted that one of the equations (Eqs. 9.2, 9.5 and 9.6) is redundant.

The total voltage, V, across the diode is the integral of the electric field over the length of the diode. Thus,

$$V = E_1 \ell + \left(\frac{E_2 + E_3}{2} - E_1 \right) W \quad .$$

Using Eq. 9.3,

$$V = E_1 \ell + \frac{\epsilon}{n_o e} \left(\frac{E_2^2 - E_3^2}{2} - E_1 (E_2 - E_3) \right) \quad . \tag{9.7}$$

Differentiating Eq. 9.7 with respect to time gives

$$\frac{dV}{dt} = \ell \frac{dE_1}{dt} + \frac{\epsilon}{n_o e} \left(\frac{dE_1}{dt} (E_3 - E_2) + \frac{dE_2}{dt} (E_2 - E_1) + \frac{dE_3}{dt} (E_1 - E_3) \right) \quad . \tag{9.8}$$

Substituting for dE_3/dt from Eq. 9.5 and for dE_2/dt from Eq. 9.6 and simplifying yields

$$\frac{dE_1}{dt} = \frac{1}{\ell} \left(v(E_1)(E_3 - E_2) + v_A (E_2 - E_1) \right) + \frac{1}{\ell} \frac{dV}{dt} \quad . \tag{9.9}$$

The velocity of the accumulation layer may be obtained from the relation,[86]

$$v_A = \frac{\int_{E_1}^{E_2} v(E)\, dE}{E_2 - E_1} \quad . \tag{9.10}$$

This equation assumes that the electric field rises uniformly in the accumulation layer or that the charge density in the accumulation layer is uniform. This will be true for triangular domains. If conditions at the time the domain starts being collected are known, Eqs. 9.9, 9.6 and 9.5 may be solved by the Runge-Kutta[74] technique.

In the preceding equations the effects of diffusion have been neglected. In practice, the depletion layer is not fully depleted because of diffusion.[77] In addition the accumulation layer width is not negligible although it is still small compared with the width of the depletion layer.[77] The preceding equations were modified to approximate the effects of diffusion in the following manner.

Let R_d be the depletion ratio defined as $R_d = n/n_o$ where n is the carrier concentration in the depletion region. Butcher et al.[77] have shown that n is nearly uniform in the depletion region. Therefore R_d is assumed to be constant along the length of this region.

The dielectric relaxation time for 1 Ω-cm GaAs is approximately 10^{-12} s. Preliminary calculations showed that typically the domain collection time is much larger than this. It is then likely that R_d will not be constant during domain collection. However, in the absence of knowledge of the exact nature of this variation, it was assumed to be constant.

As a result of R_d being nonzero, Eq. 9.2 changes to

$$\epsilon \frac{dE_1}{dt} + n_o ev(E_1) = \epsilon \frac{dE_3}{dt} + n_o R_d ev(E_3) \tag{9.11}$$

and Eq. 9.3 is replaced by

$$\frac{E_2 - E_3}{W_D} = \frac{(n_o - n)e}{\epsilon} \quad . \tag{9.12}$$

The rest of the treatment is similar to that given previously. The resultant equations were solved numerically for a diode with $n_o = 1 \times 10^{15}/cm^3$, a length of approximately 42.4 μm and a constant bias voltage ($dV/dt = 0$) of 14.8 V giving an average bias field of 3.5 kV/cm. The other parameters were chosen as follows:

μ_o = 5350 $cm^2/V\text{-}s$,

B_a = -2.6×10^6 cm/s,

B_b = 1.047×10^{11} $V(s)^{-1}$,

B_c = 228.8 $cm^2/V\text{-}s$, the high-field mobility,

B_d = 0.132×10^{15} $(V)^2$ $(cm\text{-}s)^{-1}$ and

E_{th} = 3.33 kV/cm.

Conditions at the start of domain collection were obtained from the calculations of Butcher et al.[77] as follows:

E_1 = 1.75 kV/cm,

E_2 = 46.7 kV/cm,

R_d = 0.142.

The results are shown in Figs. 9.2 through 9.4.

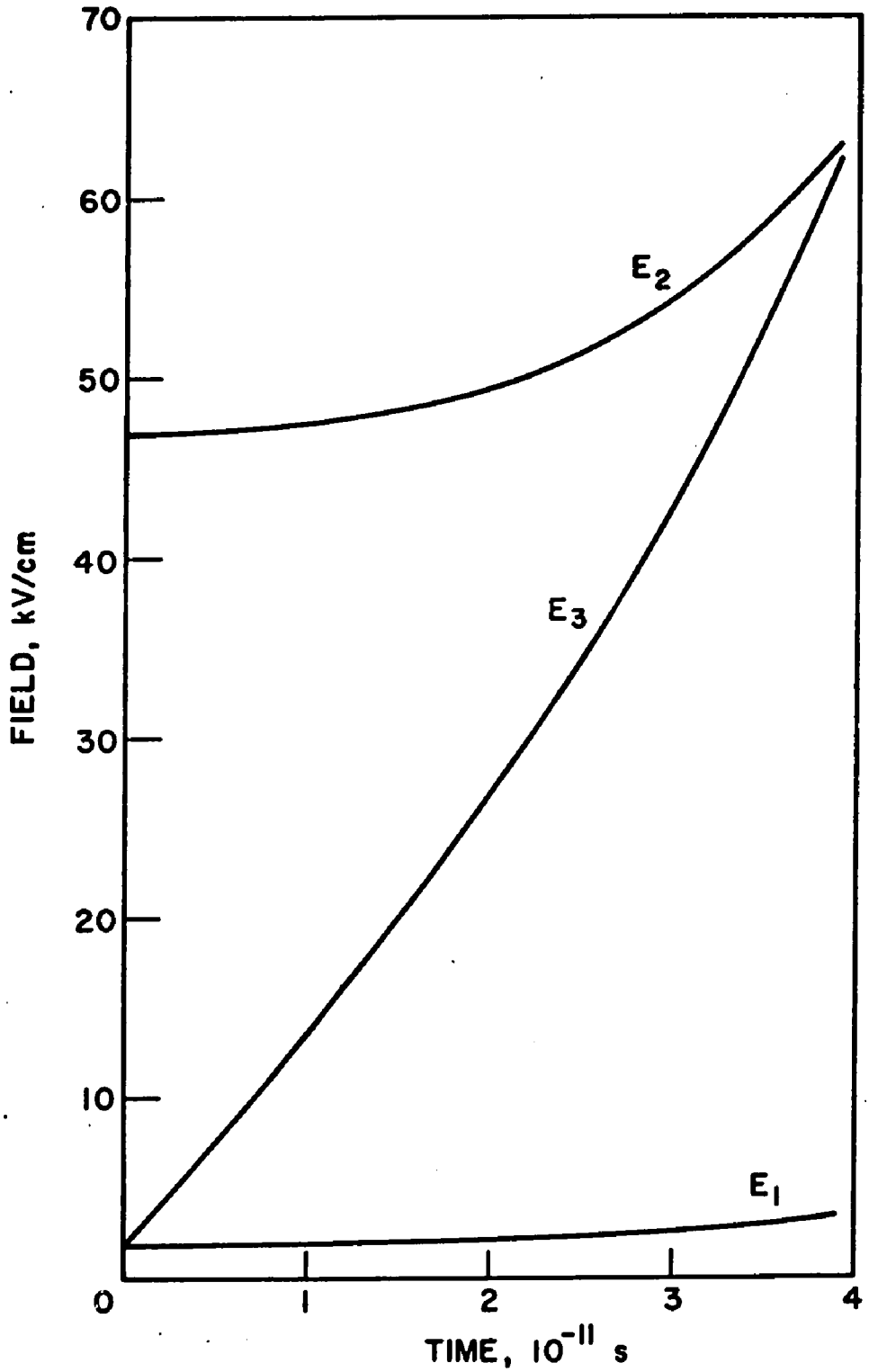


FIG. 9.2 CALCULATED VALUES OF E_1, THE FIELD NEAR THE CATHODE; E_2, THE PEAK FIELD IN THE DOMAIN AND E_3, THE FIELD NEAR THE ANODE VS. TIME. (THE DIODE IS 42.4-μm LONG WITH A DOPING DENSITY OF $10^{15}/cm^3$ AND A BIAS VOLTAGE OF 14.8 V.)

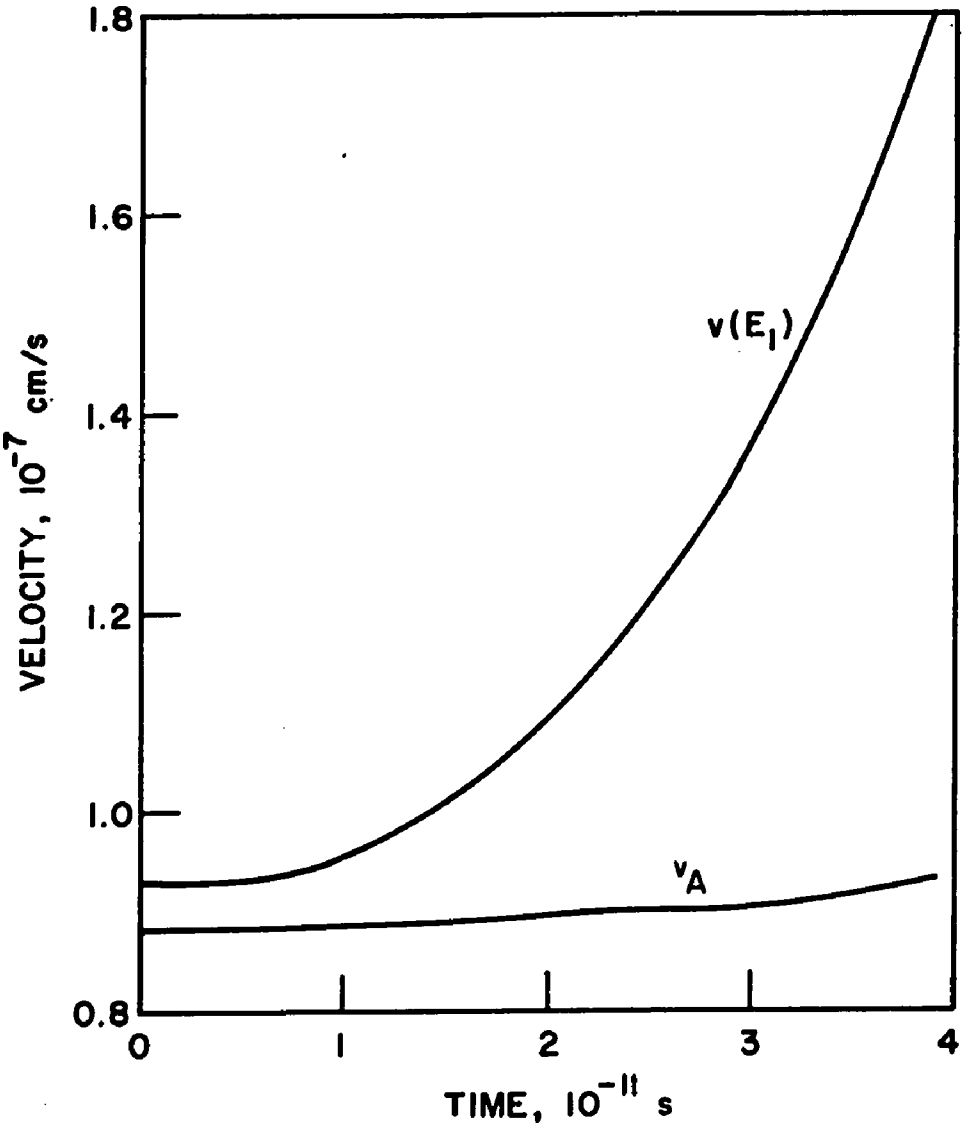


FIG. 9.3 CALCULATED DOMAIN VELOCITY AND VELOCITY OF CARRIERS OUTSIDE THE DOMAIN VS. TIME FOR A GaAs DIODE. (THE DIODE IS 42.4-μm LONG WITH A DOPING DENSITY OF $10^{15}/cm^3$ AND A BIAS VOLTAGE OF 14.8 V.)

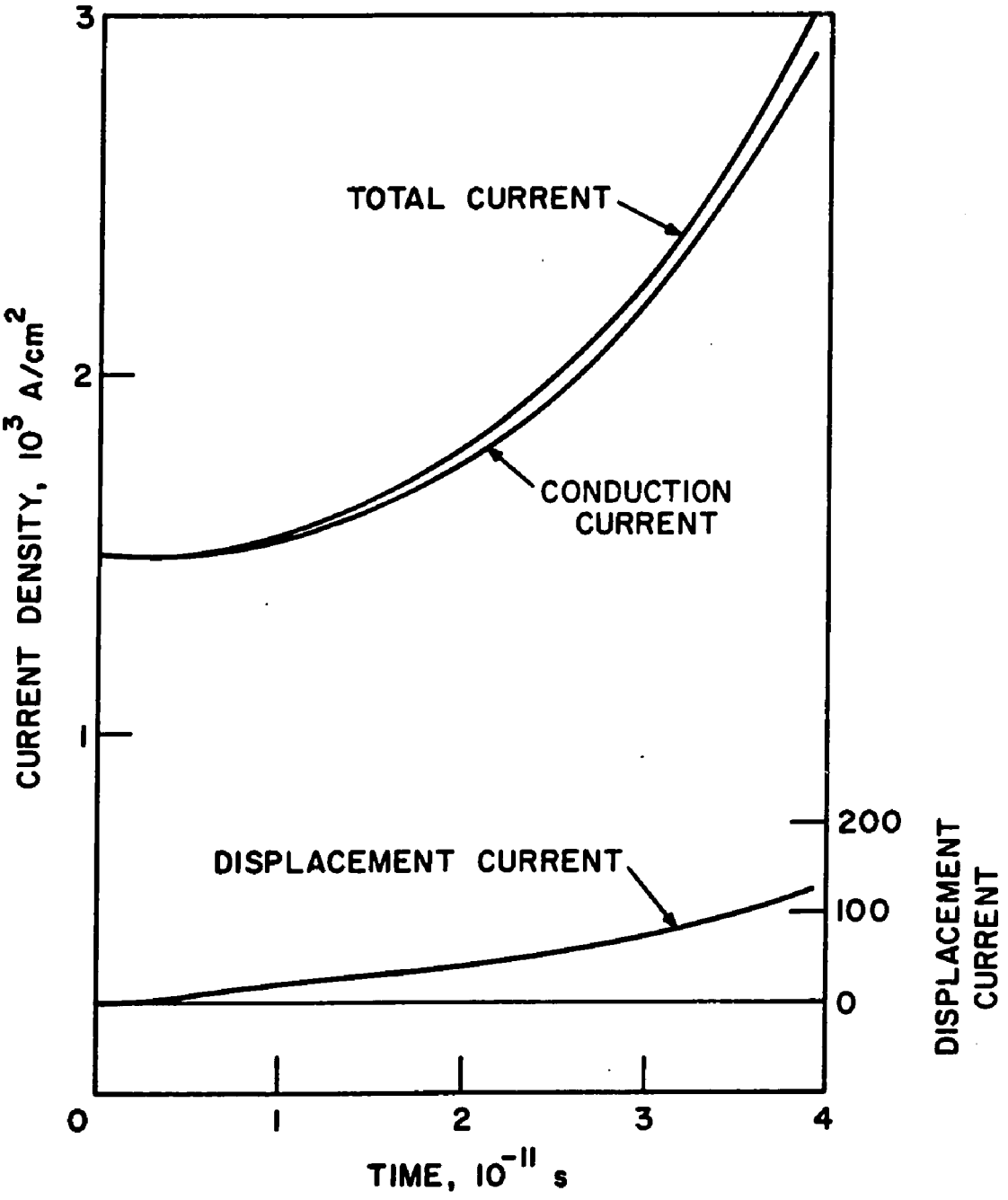


FIG. 9.4 CALCULATED CONDUCTION, DISPLACEMENT AND TOTAL CURRENT DENSITIES NEAR THE CATHODE FOR A GaAs DIODE. (THE DIODE IS 42.4-μm LONG WITH A DOPING DENSITY OF $10^{15}/cm^3$ AND A BIAS VOLTAGE OF 14.8 V.)

It is seen in Fig. 9.2 that all the electric fields E_1, E_2 and E_3 increase during collection of the domain. At the start of the domain collection E_1 and E_3 are equal and at the end, E_2 and E_3 are equal. Figure 9.3 shows that $v(E_1)$ increases considerably, whereas v_A remains almost constant during this time. This increasing difference in velocities causes a growth in the accumulation layer and a consequent rise in the electric field E_2.

Figure 9.4 shows the conduction, displacement and total current densities near the cathode. The displacement current is quite small and as a result the total current nearly follows the electric field near the cathode. The displacement current near the anode, on the other hand, will form a substantial part of the total current since E_3 increases rapidly and the carrier concentration is small.

The calculations reported here were done only up to the point where the field outside the domain reaches threshold. After this a new domain is expected to be nucleated near the cathode. In the delayed-domain mode, however, the field outside the domain reaches threshold only after the domain has been collected.

A straight-line representation (Eq. 9.1) has been assumed for the low-field velocity-electric field relationship. This corresponds to a constant value of the device dc resistance below the threshold voltage. However in a more realistic situation, this resistance is a function of the voltage across the device and can be treated by using a cubic current-voltage relationship such as

$$I_{cond} = A_a V + A_b V^2 + A_c V^3 \quad , \tag{9.13}$$

where I_{cond} stands for the conduction current at the cathode. The constants A_a, A_b and A_c for a given device can be evaluated from measurements on the device to be studied.

As stated before, the accumulation layer has a finite width as a result of diffusion effects. Therefore the time for the extinction of the accumulation layer must be taken into account. For the purpose of calculating the current during extinction of the accumulation layer, it was assumed that the charge in the layer dissipates according to a positive time constant

$$\tau_p = \frac{\epsilon}{\sigma} , \tag{9.14}$$

where σ is the low-field conductivity of the GaAs material. This time constant is the same as that used by Khandelwal[63] for the quenching of the domain. Thus, if V_{Do} is the "domain" voltage at the end of the depletion-layer collection, then the remaining domain voltage at a later time is given by

$$V_D = V_{Do} e^{-t/\tau_p} . \tag{9.15}$$

The value of V_{Do} can be obtained by subtracting $E_1 \ell$ from V at the end of the depletion-layer collection. The field outside the domain is then

$$E_1 = \frac{1}{\ell} \left(V - V_{Do} e^{-t/\tau_p} \right) . \tag{9.16}$$

The conduction current at the cathode is again found by substituting $E_1 \ell$ for V in Eq. 9.15. To find the displacement current Eq. 9.11 is differentiated with respect to time and is multiplied by ϵA giving

$$I_{dis} = \epsilon \frac{A}{\ell} \left(\frac{dV}{dt} + \frac{V_{Do}}{\tau_p} e^{-t/\tau_p} \right) . \tag{9.17}$$

After the domain has been fully collected, the diode voltage must be below threshold in order for the formation of a new domain to be delayed. The conduction current is then given by Eq. 9.13 and the displacement current by $C_o(dV/dt)$ where C_o is the low-field capacitance of the diode. The formation of a new domain starts when the voltage reaches the threshold voltage again.

9.4 The Delayed-Domain Mode

A complete cycle in this mode of operation consists of domain formation, domain propagation, domain collection and the delay between domain collection and the nucleation of a new domain. The complete current waveform for a given voltage across the device can be constructed if the current during each part of the cycle is known.

The equations of Khandelwal[63] can be used for calculating the device current during domain formation and during its propagation before it starts being collected at the anode. The equations also provide the initial conditions for domain collection. To determine these, the time at which domain collection starts must be known. Domain collection starts when the leading edge of the domain reaches the anode. The time t at which this occurs is given by

$$l = \int_0^t v_A \, dt + W_D \quad , \tag{9.18}$$

where v_A is the velocity of the accumulation layer and W_D is the width of the depletion layer. Butcher and Fawcett[91] have calculated the widths of

accumulation layers and depletion layers of domains. Their results show that the width of the accumulation layer is nearly constant for a particular resistivity. An approximate value of the accumulation layer width can thus be obtained from their data.

Considering the nature of the relation between total domain width and domain voltage,[63] an expression of the following form was used to estimate the width

$$W = P + QV_D + SV_D^2 \quad , \tag{9.19}$$

where W is the width of the domain; V_D is the domain voltage; and P, Q and S are constants. The value of V_D is available from the terminal voltage and the stable-domain characteristic. The width W_D of the depletion layer may then be obtained by subtracting the accumulation-layer width from W. The values of E_1 and E_2 at the start of domain collection can be obtained from

$$E_1 = \frac{V - V_D}{\ell} \tag{9.20}$$

and assuming triangular domains,

$$E_2 = E_1 + \frac{2V_D}{W} \quad . \tag{9.21}$$

The current during domain collection can now be calculated as explained in the last section.

Current waveforms for a diode voltage of the type

$$V = V_B + V_1 \sin \omega t$$

have been calculated. The various parameters were chosen as follows:

ℓ = 16 μm,

A = 0.13×10^{-3} cm^2,

μ_o = 5500 $cm^2/V\text{-}s$,

n_o = $10^{15}/cm^3$,

V_{TH} = 5.2 V (threshold field = 3.25 kV/cm) and

V_S = 4.47 V (the domain sustaining voltage).

The following velocity-field characteristic was assumed for the purpose of calculating the velocity of the accumulation layer:

$$v = \mu_o E \quad \text{for} \quad E \leq E_{th} ,$$

$$v = B_a + B_b/E + B_c E + B_d/E^2 \quad \text{for} \quad E_{th} < E \leq 12 \text{ kV/cm} ,$$

$$v = 0.8 \times 10^7 \text{ cm/s} \quad \text{for} \quad E > 12 \text{ kV/cm} ,$$

where B_a = -2.6×10^6 cm/s,

B_b = 1.047×10^{11} $V(s)^{-1}$,

B_c = 228.8 $cm^2/V\text{-}s$ and

B_d = -0.132×10^{15} $(V)^2$ $(cm/s)^{-1}$.

The depletion layer was assumed to be fully depleted. Figure 9.5 shows the voltage and current waveforms for a dc bias of 8 V and an RF voltage amplitude of 3.5 V. The plots are made for frequencies below the transit-time frequency which was estimated to be slightly higher

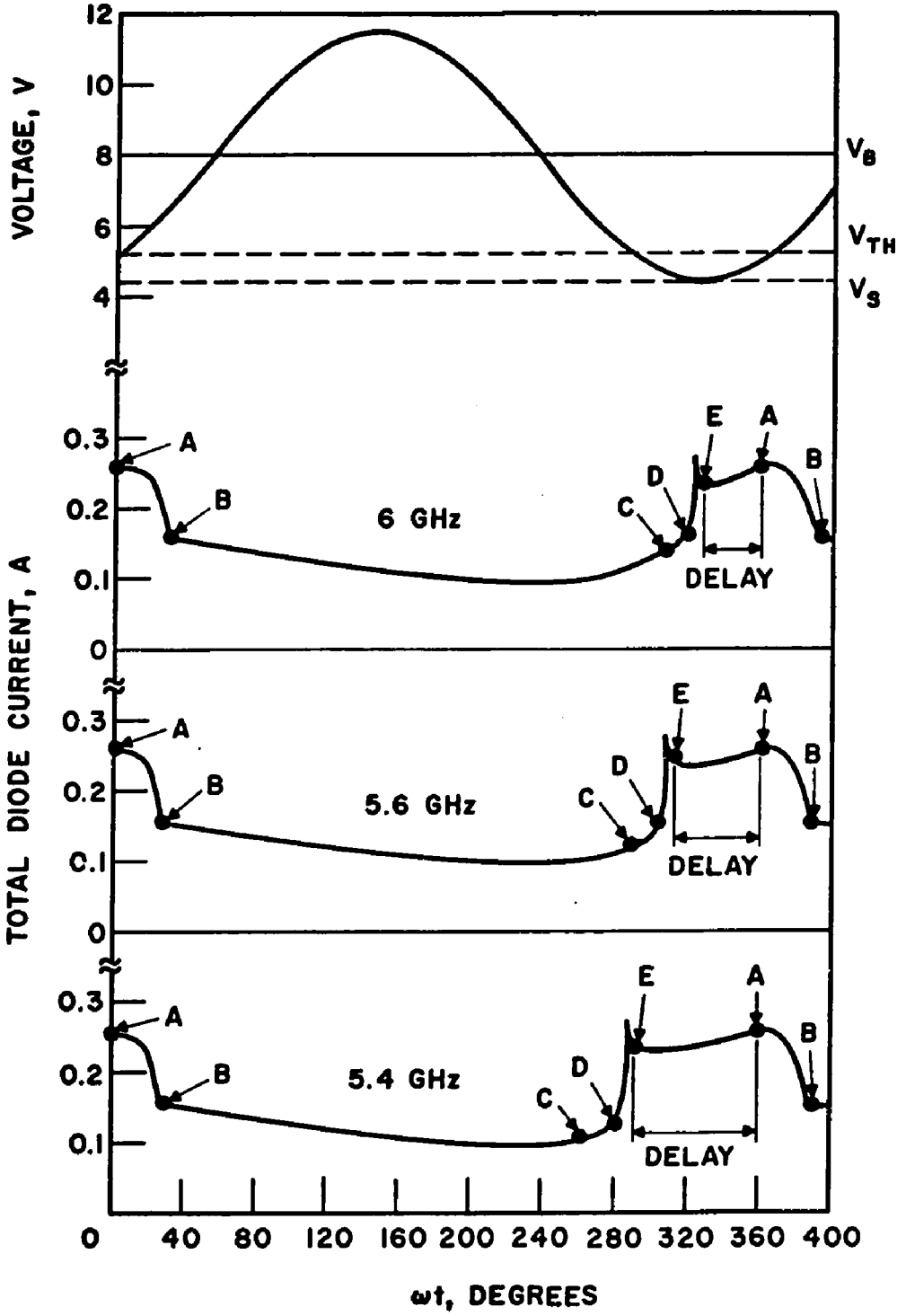


FIG. 9.5 VOLTAGE AND CURRENT WAVEFORMS FOR A DIODE OPERATING IN THE DELAYED-DOMAIN MODE WITH ℓ = 16 μm, A = 0.13 x 10^{-3} cm^2, μ_o = 5500 $cm^2/V\text{-}s$, n_o = $10^{15}/cm^3$, V_{TH} = 5.2 V, V_S = 4.47 V, BIAS VOLTAGE = 8 V AND RF VOLTAGE AMPLITUDE = 3.5 V. (A) DOMAIN FORMATION STARTS, (B) DOMAIN FORMATION ENDS, (C) DEPLETION LAYER COLLECTION STARTS, (D) ACCUMULATION LAYER COLLECTION STARTS AND (E) DOMAIN COLLECTION IS COMPLETED.

than 6 GHz. As expected, the current decreases during domain formation and increases during its extinction. The bulk of the current increase during domain collection is at the start of the dissipation of the accumulation layer. Since the voltage is below the threshold voltage after the domain has been fully collected, there is a delay in the nucleation of a new domain. This delay is indicated in the figure (points E to A) and is seen to be higher at lower frequencies leading to a greater fundamental component of current 180 degrees out of phase with the RF voltage.

The current waveforms were Fourier analyzed to find the efficiency of dc to RF conversion. Figure 9.6 shows a plot of efficiency vs. frequency for constant dc and RF voltage levels. As expected, the efficiency is higher at lower frequencies, being 9 percent at 5.4 GHz. The figure also shows a plot of the delay (points E to A in Fig. 9.5) in domain formation vs. frequency.

Calculations showed that at a higher bias level of 8.8 V and with an RF voltage amplitude of 5 V, an efficiency of 10.4 percent was obtained at 5.4 GHz. Further calculations of efficiency for different cases are shown in Fig. 9.7. The device parameters were chosen to approximate those of Reynolds et al.,[92] who have obtained high-efficiency operation in what appears to be the delayed-domain mode. The parameters are:

$\ell = 80\ \mu m$,

$A = 0.105 \times 10^{-2}\ cm^2$,

$n_o = 10^{15}/cm^3$ (full ionization of donors assumed),

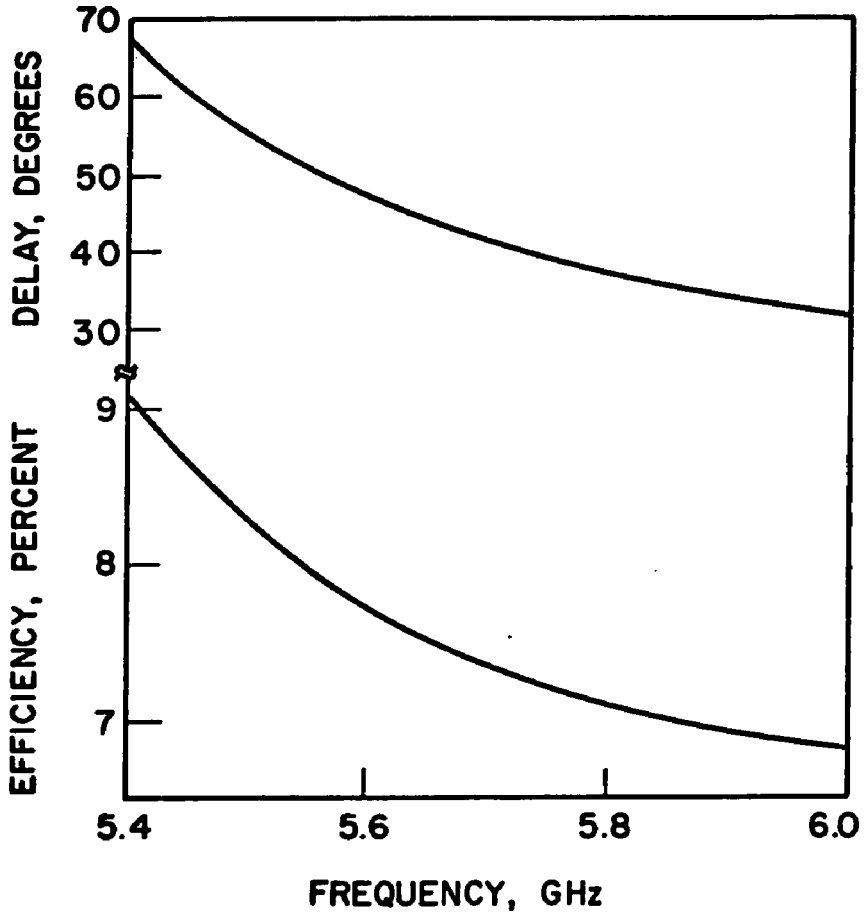


FIG. 9.6 THE DELAY IN DOMAIN FORMATION (POINTS E TO A IN FIG. 9.5) AND EFFICIENCY VS. FREQUENCY FOR A DIODE OPERATING IN THE DELAYED-DOMAIN MODE. (ℓ = 16 μm, A = 0.13 x 10^{-3} cm^2, μ_o = 5500 cm^2/V-s, n_o = $10^{15}/cm^3$, V_{TH} = 5.2 V, V_S = 4.47 V, BIAS VOLTAGE = 8 V, RF VOLTAGE AMPLITUDE = 3.5 V)

V_{TH} = 26 V (threshold field = 3.25 kV/cm),

V_S = 16.7 V (calculated from domain voltage vs. outside electric field data).

Curve I shows efficiency vs. frequency for a voltage bias of three times the threshold. The RF voltage is a sinusoid of an amplitude of 61.2 V, such that the instantaneous voltage across the device does not go below the domain-sustaining voltage thus preventing any possibility of domain quenching. The maximum frequency shown on the curve is the transit-time frequency, i.e., a new domain nucleates as soon as the previous one is collected for this case. The rest of the curve represents the delayed-domain mode. The efficiency is seen to increase from 7 percent at the transit-time frequency to 12 percent at 0.82 GHz. It is not possible to obtain the delayed-domain mode at frequencies lower than 0.82 GHz as the instantaneous voltage across the device is not below the threshold after the domain is collected.

The RF voltage amplitude was increased to 68 V to enable domain quenching at certain frequencies, and Curve II of Fig. 9.7 was obtained for efficiency as a function of frequency. The frequencies above that at point B on the curve are such that quenching of the domain occurs before it reaches the anode. For frequencies between points A and B, quenching of the domain occurs during its collection at the anode. The part of the curve below point A represents the pure delayed-domain mode. Because of the larger RF voltage amplitude compared to the case of Curve I, the device terminal voltage reaches the threshold value at a lower transit angle making operation possible at lower frequencies as seen on the curve.

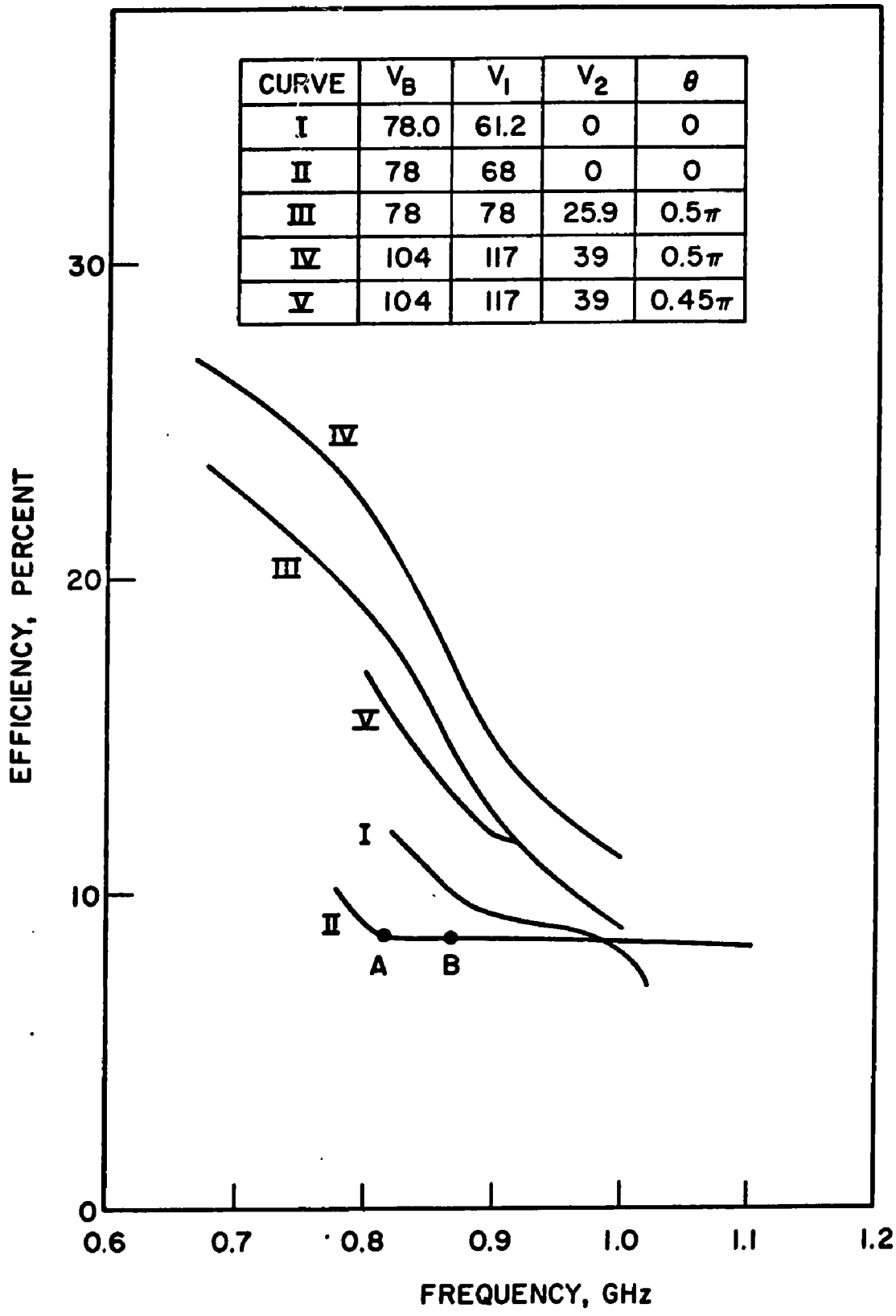


FIG. 9.7 EFFICIENCY VS. FREQUENCY FOR A GaAs DIODE FOR DIFFERENT VALUES OF SECOND-HARMONIC VOLTAGE. (ℓ = 80 μm, A = 0.105 x 10^{-2} cm^2, n_o = $10^{15}/cm^3$, V_{TH} = 26 V, V_S = 16.7 V)

However, the efficiencies are lower because now the amplitude of the current is reduced for most of the period during the high current state of the device (state between domain collection and renucleation) because of the lower device terminal voltage.

Figure 9.7 also shows calculations made for voltage waveforms of the type

$$V = V_B + V_1 \sin \omega t + V_2 \sin(2\omega t - \theta) \quad . \tag{9.22}$$

Kino and Kuru[88] have suggested $V_2 = (1/3)V_1$ and $\theta = \pi/2$ for high-efficiency operation. Such a waveform is shown in Fig. 9.8 where $V_B = 104$ V, $V_1 = 117$ V, $V_2 = 39$ V. The values of V_B and V_1 have been chosen such that the voltage across the device stays below the threshold value and above the domain-sustaining voltage for a substantial part of the cycle. If the domain is collected at the start of the period, the device stays in a high current state for a considerable part of the cycle, resulting in a high dc to RF conversion efficiency. Figure 9.8 also shows the current waveforms for three different frequencies. The large dip near a transit angle of 160 degrees is because of the large displacement current resulting from the rapid fall in device terminal voltage.

Curve IV in Fig. 9.7 shows efficiency as a function of frequency for the voltage waveform of Fig. 9.8. A maximum efficiency of 27 percent is seen. For a lower bias of 78 V but retaining the above voltage waveshape, the efficiencies are lower as shown in Curve III. The value of θ was changed from 0.5π to 0.45π while retaining the other conditions

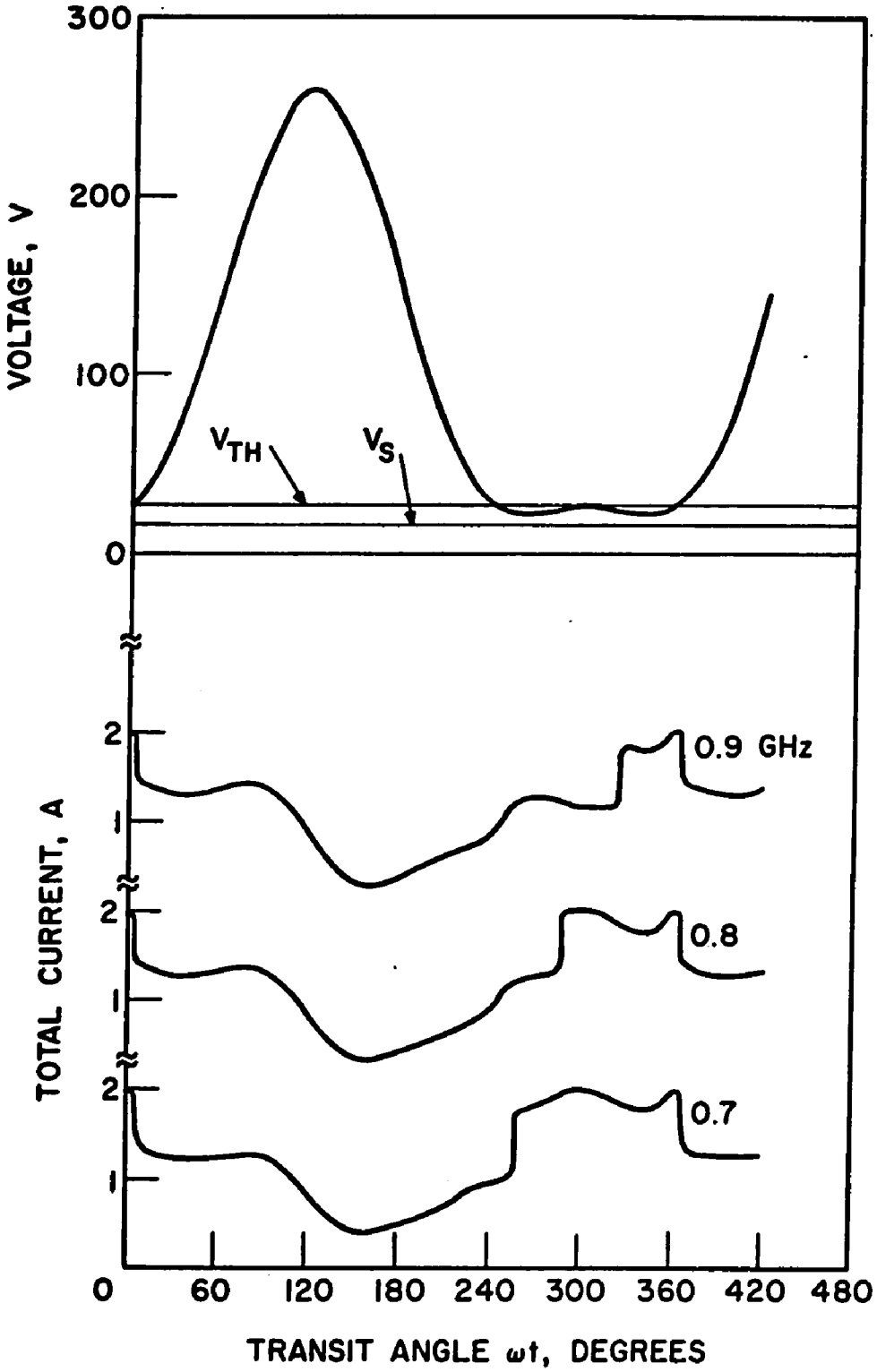


FIG. 9.8 VOLTAGE AND CURRENT WAVEFORMS FOR A GaAs DIODE OPERATING IN THE DELAYED-DOMAIN MODE. (l = 80 μm, A = 0.105 x 10^{-2} cm^2, n_o = $10^{15}/cm^3$, V_{TH} = 26 V, V_S = 16.7 V, V_B = 104 V, V_1 = 117 V, V_2 = 39 V, $\theta = 0.5\pi$)

of Curve IV, and Curve V was obtained which shows a reduction in efficiency and a restricted frequency range of operation in the delayed-domain mode. Changing θ to 0.55π made operation in the delayed-domain mode possible only near 8.5 GHz with efficiency nearly that corresponding to Curve IV. At other frequencies either domain quenching occurred with no gain in efficiency or a domain was nucleated after the collection of a previous one.

Increasing V_1 from 117 V to 123 V and V_2 from 39 V to 40.3 V with $\theta = 0.5\pi$ nearly retains the shape of the voltage wave of Fig. 9.8 but causes a reduction in the maximum efficiency as seen in Curve I of Fig. 9.9. This is because of a lower value of device terminal voltage and consequently a lower current during the high-current state of the device. This result is similar to the single-frequency case described earlier. The lower end of the frequency range of operation is also slightly extended in analogy with the single-frequency case. It is possible to extend the frequency of operation slightly further and increase efficiency on the low-frequency side by making V_2 greater than $1/3\ V_1$ as shown in Curve II of Fig. 9.9.

In order for operation with the second harmonic present to be feasible, the conductance at the second harmonic must be negative or else the second harmonic cannot be sustained. Further, the magnitude of this negative conductance must not continue to increase indefinitely with V_2 in order for the system to stabilize at some value of V_2. In every case with the second harmonic included which is reported here, the conductance at the second harmonic calculated by Fourier analysis of

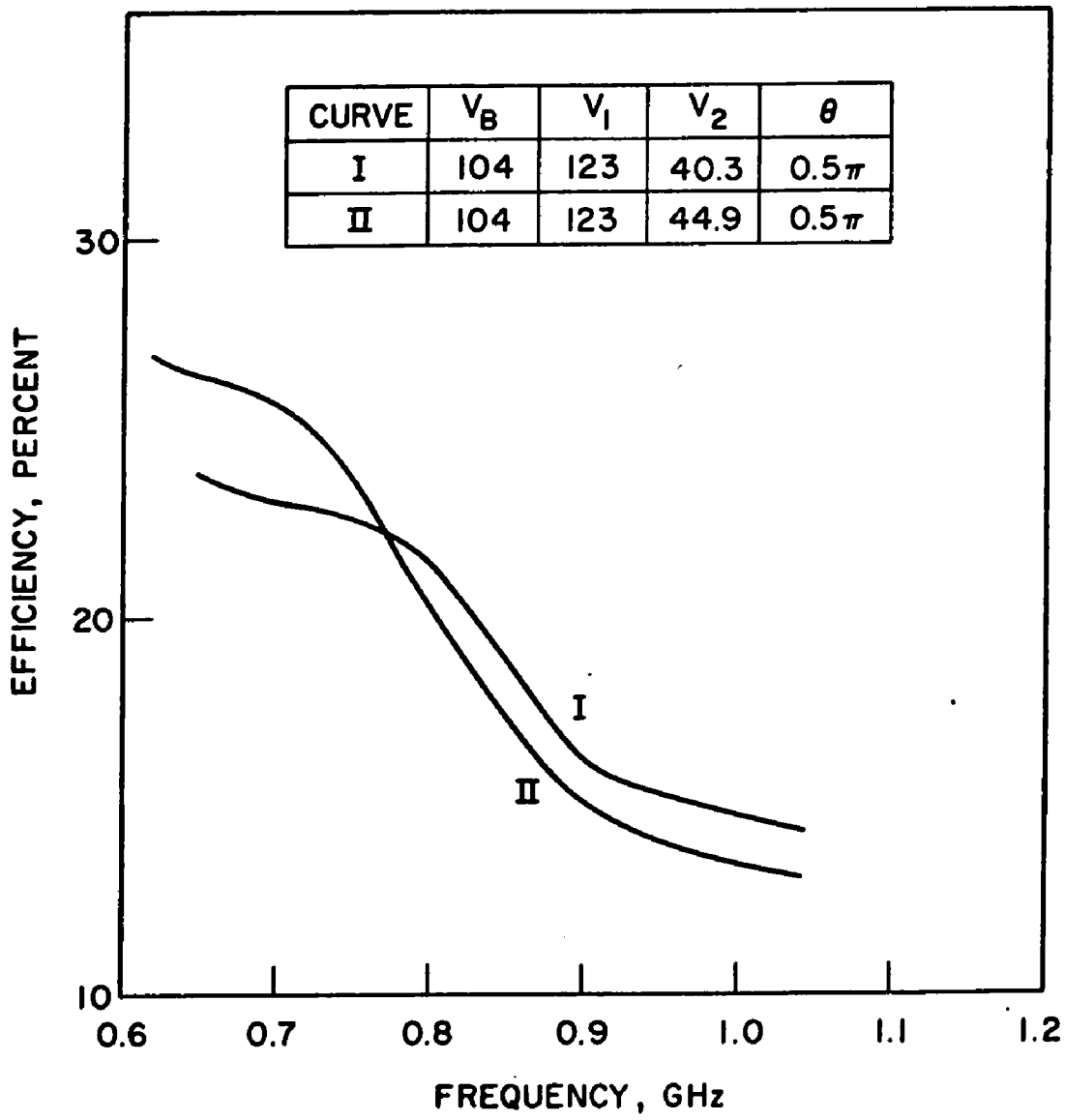


FIG. 9.9 EFFICIENCY VS. FREQUENCY FOR A GaAs DIODE FOR DIFFERENT SECOND-HARMONIC VOLTAGES. (ℓ = 80 μm, A = 0.105 x 10^{-2} cm^2, n_o = $10^{15}/cm^3$, V_{TH} = 26 V, V_S = 16.7 V)

the current waveform was found to be negative. Plots of negative admittance at the second harmonic for V_B = 104 V, V_1 = 123 V and $\theta = \pi/2$ with varying V_2 are shown in Fig. 9.10 at three different frequencies. It is seen that the magnitude of the negative conductance increases as V_2 is increased from 40.3 V to 44.5 V, but decreases as V_2 is increased further.

Figure 9.11 gives the plot of admittance at the fundamental frequency for V_B = 104 V, V_1 = 123 V, V_2 = 40.3 V and $\theta = \pi/2$, showing an increasing negative conductance and decreasing susceptance at low frequencies.

The efficiencies obtained in this study are in good agreement with those reported by Reynolds et al.[92] for the delayed-domain mode. The presence of inductive circuit reactance at the second harmonic in their circuit is also consistent with the positive susceptance of the device at the second harmonic as shown in Fig. 9.10.

9.5 Conclusions

It has been shown that for a diode operated under constant bias voltage conditions, the peak field in the domain increases as the domain is collected at the anode. This result is in agreement with that of Robrock.[87]

Calculations of current waveforms for a diode operated in the delayed-domain mode show that the delay in the formation of a domain, after the previous one has been collected, increases with decreasing frequency. This results in higher efficiencies at the lower frequencies. Efficiency also increases as the bias level is increased from three to four

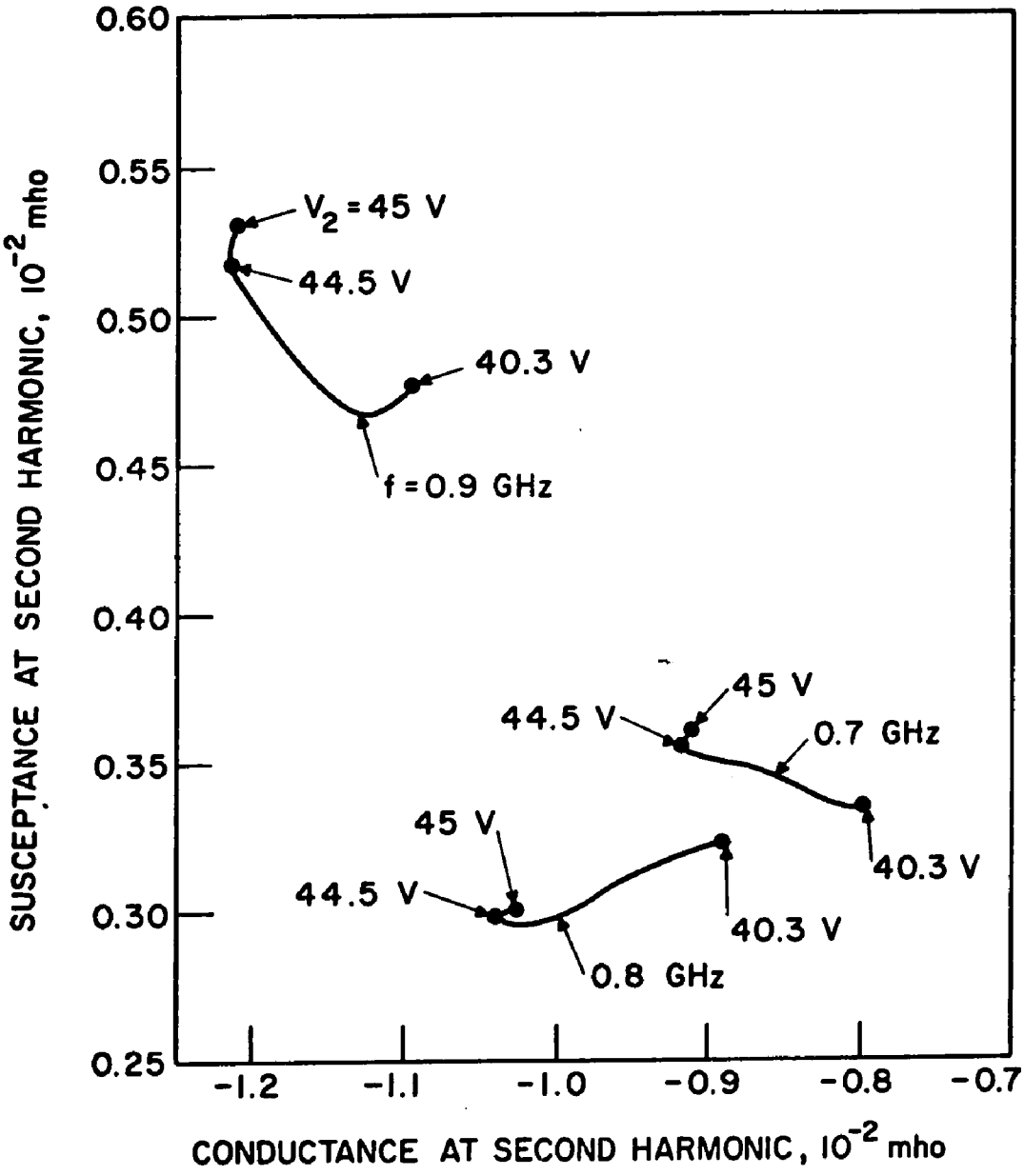


FIG. 9.10 ADMITTANCE AT SECOND HARMONIC FOR A GaAs DIODE. (ℓ = 80 μm, A = 0.105 x 10^{-2} cm^2, n_o = $10^{15}/cm^3$, V_{TH} = 26 V, V_S = 16.7 V, V_B = 104 V, V_1 = 123 V, $\theta = 0.5\pi$)

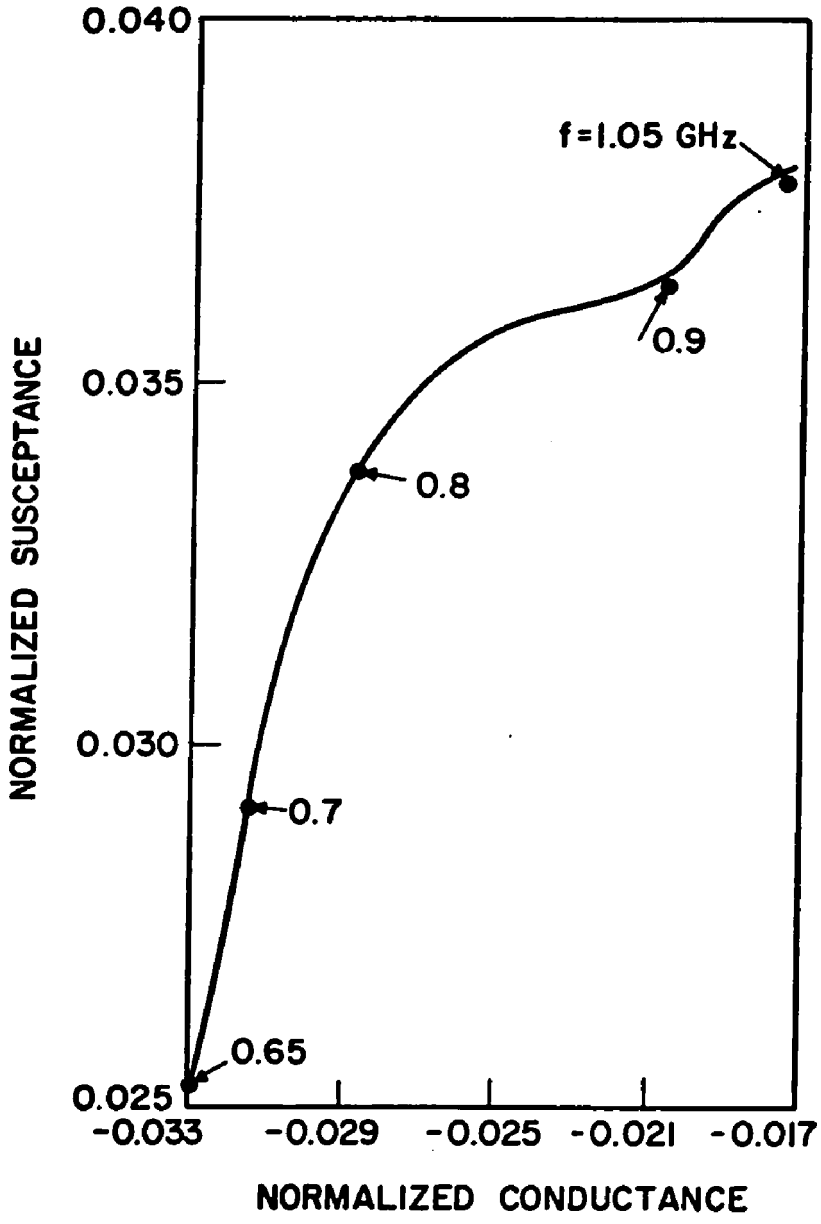


FIG. 9.11 ADMITTANCE AT THE FUNDAMENTAL FREQUENCY NORMALIZED WITH RESPECT TO THE LOW-FIELD CONDUCTANCE FOR A GaAs DIODE. (ℓ = 80 μm, $A = 0.105 \times 10^{-2}$ cm^2, $n_o = 10^{15}$/cm^3, V_{TH} = 26 V, V_S = 16.7 V, V_B = 104 V, V_1 = 123 V, V_2 = 40.3 V, $\theta = 0.5\pi$)

times the threshold voltage. An increase in RF voltage level is not necessarily an advantage for efficiency, but it can extend the frequency of operation slightly on the low-frequency side. A second harmonic in a device can be sustained if it is placed in a proper circuit and such a harmonic can increase the efficiency greatly. The values of efficiencies calculated as functions of frequency are in good agreement with the experimental results of Reynolds et al.[92]

CHAPTER X. CONCLUSIONS AND SUGGESTIONS FOR FURTHER STUDY

10.1 Conclusions

A theoretical and experimental study of stabilized transferred-electron amplifiers has been presented. Large-signal effects and the effects of various operating and material parameters such as bias voltage, lattice temperature and doping density have been investigated.

In the large-signal analysis, the effects of carrier diffusion were included and the dependence of diffusion coefficient upon the electric field was taken into account. It was found that diffusion reduces the dc to RF conversion efficiency by approximately 20 percent. Calculations showed that static-field distortion present in subcritically doped devices significantly increases with increase in RF drive level. This results in a decrease in average current when oscillations occur or large RF signals are injected with fixed bias voltage, despite the absence of space-charge dipole domains. This has been verified experimentally.

Theoretical calculations showed that as the bias voltage is increased above threshold, the magnitude of the device negative resistance first increases, reaches a maximum and then decreases. Thus in some circuits the diode will exhibit stable amplification at a bias voltage just above threshold, oscillate as the bias is increased and become stable again at a higher bias. However, if the magnitude of the maximum (series) negative resistance is less than the positive (series)

resistance of the circuit, no oscillation occurs and stable amplification is observed over a wide range of bias voltages. Experimental data illustrating the last effect was presented. It was shown that the gain goes through a maximum as the bias is varied keeping the input power constant.

One of the attractive features of these amplifiers is the possibility of obtaining linear amplification over a wide dynamic range. However, it was found that linearity of gain can be achieved only under restrictive conditions. Calculations showed that the magnitude of the device negative resistance at first increases and then decreases as the RF signal amplitude is increased from a small value. Thus in the experimental measurements the device showed gain expansion at small signal powers. Gain compression occurred at higher RF powers. If the difference between the magnitude of maximum negative resistance of the device and the circuit resistance is small, gain is high and is sensitive to any variation in device negative resistance. The nonlinearity of gain is quite pronounced under such conditions. It was found in the experimental study that if the gain is not too high, i.e., if it is approximately 10 dB or less, then it may be assumed to be constant up to large input power.

Under CW operation, the dc power dissipation in the crystal causes an increase in the lattice temperature. This reduces the dc to RF conversion efficiency. It was shown theoretically that if the temperature at the anode can be maintained below the temperature at the cathode, the efficiency is considerably better than if the opposite is true or if

the temperature is uniform. Thus it would be advantageous to place the heat sink at the anode rather than at the cathode.

From the theoretical calculations, the best efficiency obtainable with these devices when the donor density is uniform was found to be of the order of 3 percent. This occurs for values of n_o in the vicinity of $0.3 \times 10^{15}/cm^3$ for X-band operation with GaAs crystals approximately 10 μm long. It was shown that the efficiency can be improved if the donor density increases gradually from the cathode to the anode.

Root-gain bandwidth products (i.e., $G^{1/2} B$, where G = power gain, B = bandwidth) of the order of 5.4 GHz were achieved in a coaxial circuit using Chebychev transformers. Root-gain bandwidth values as high as 9.5 GHz were shown to be possible theoretically if the values of lead inductance and package capacitance were neglected. Calculations showed that negative resistance over multiple octaves was possible at relatively low bias voltages and small signals.

An analytical model of the delayed-domain mode was developed in order to assess the potential of this mode for large-signal amplification by injection locking. Dc to RF conversion efficiencies as high as 27 percent have been shown for GaAs diodes when a second-harmonic signal is present in addition to the fundamental.

10.2 Suggestions for Further Study

Perhaps the most significant limitation of stabilized transferred-electron amplifiers is their low dc to RF conversion efficiency. The present study has indicated some of the ways in which this can be improved.

Detailed analytical study should be made as to the nature of the doping profile required for best efficiency. While precise control of the doping profile is not possible at this stage, attempts should be made to achieve the best profile experimentally. Similar effects on efficiency are expected if the area of the cross section of the crystal increases gradually from the cathode to the anode for uniformly doped material. Theoretical and experimental studies should be made of this effect.

It has been shown that the efficiency is highest at low temperatures. This is because of the higher peak-to-valley ratio of the velocity-electric field relationship at lower temperatures. Materials of higher peak-to-valley ratios, such as InP, should be investigated to obtain higher efficiencies.

Lead inductance and package capacitance have been shown to affect the root-gain bandwidth product adversely. Integration of the devices into properly designed circuits should be attempted to achieve the root-gain bandwidth predicted theoretically.

The analytical model of the delayed-domain mode shows that dc to RF conversion efficiencies greater than 25 percent are possible with GaAs diodes when second-harmonic voltage is present in proper phase and magnitude. Circuits should be designed where control of impedance at both the fundamental and the second harmonic is possible to achieve these efficiency values. Materials (such as InP) with peak-to-valley ratios higher than those in GaAs should be used to try to obtain even higher conversion efficiencies.

APPENDIX A. THE EFFECT OF FINITE TRANSVERSE DIMENSIONS

When the transverse dimensions of a diode are small compared with the space-charge wavelength, the phase velocity of the space-charge wave is modified.[93] This effect is small if

$$\left|\frac{\omega r}{v_o}\right| \gg 1 \quad , \tag{A.1}$$

where ω is the frequency in rad/s, r is one half of the smallest transverse dimension and v_o is the drift velocity. If on the other hand r is greater than the skin depth, the RF currents vary along the transverse direction. One-dimensional analyses like those presented in Chapters II and IX are valid only if Eq. A.1 is satisfied and if the transverse dimensions are smaller than the skin depth.

For a GaAs crystal made from material of 1 Ω-cm resistivity (which is typical) and operated at X-band frequencies, Eq. A.1 is satisfied if r is much greater than 1.6 μm. The upper limit on r is imposed by the skin depth which is 500 μm. Most two-terminal TE devices fall well within these two limits.

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